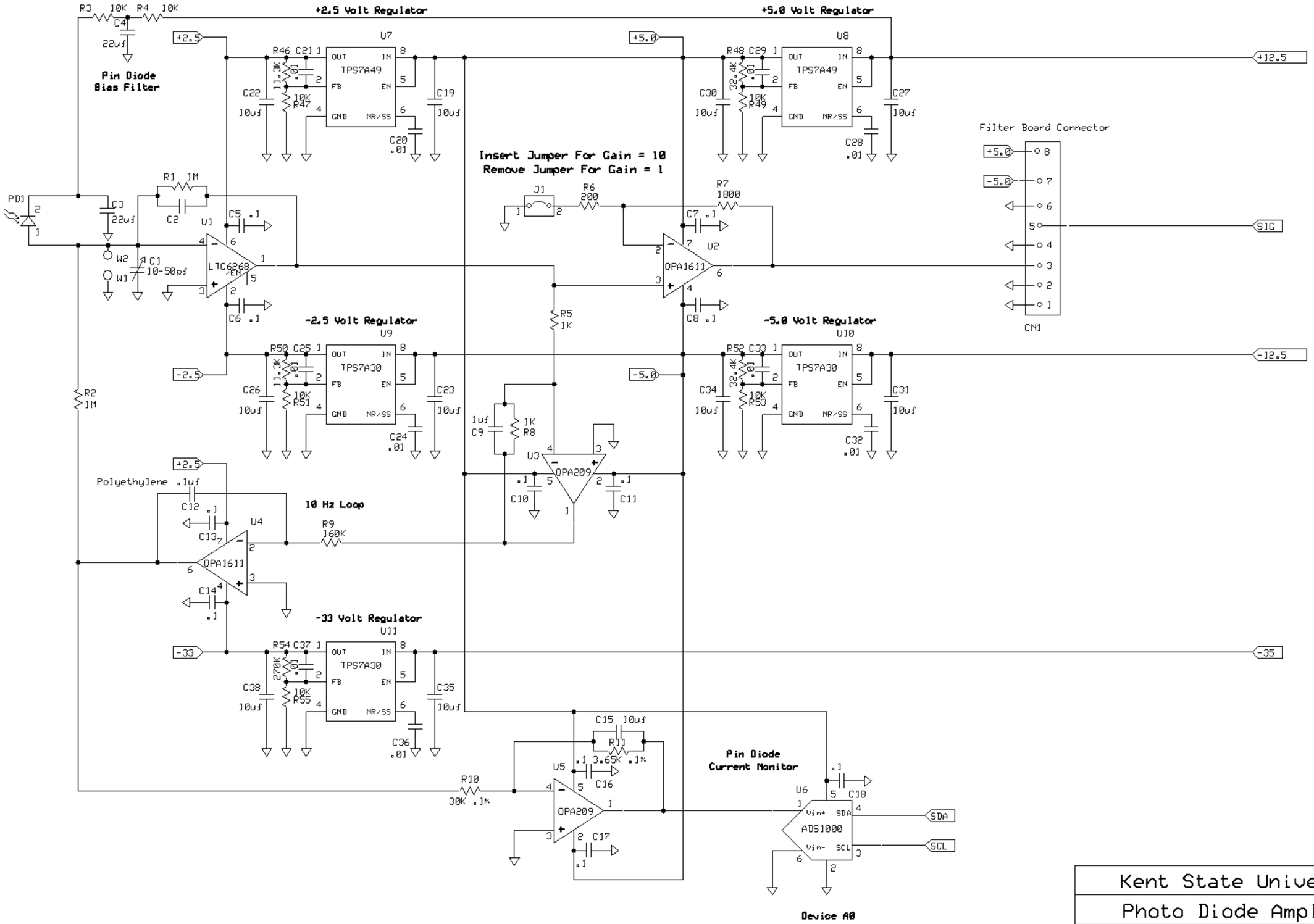


Kent State University		
Photo Diode Amplifier		
Alan R. Baldwin	Rev 1.0 10/25/2018	1 of 2

+12.5 Volt Regulator

U22

TPS7A49

OUT IN FB EN GND NR/SS

+12.5 R42 95.3K C71 60pf R43 10K C70 10uf C72 .01 C73 10uf

Insert Jumper For Gain = 10

Remove Jumper For Gain = 1

J2 R13 200 R14 1800

Board Modification

SIG C39 100Uf R56 1K +2.5 -2.5

Digital Potentiometer

U13 CAT5113

Vcc Control U/D INC CS Gnd RH RW RL

U12 TLC3704 NC C40 .1 C41 .1 C42 .1 C43 .1

R12 10

U14 OPA1611 C44 .1 C45 .1

R20 1K R18 392 .1% R19 3.24K .1% R17 10

U15 THS4131 Vccm C47 1uf C48 1uf C49 1uf

R15 402 .1% R22 1M R16 3.24K .1% C53 .1

DIFF ZERO

U16 OPA209 C50 .1 C51 .1 C46 .47uf

COMM ZERO

U17 OPA209 C54 .1 C55 .1 C52 1uf

10 Hz Loop

R21 1.5K

1 Hz Loop

R25 25 R26 25 R23 10K R24 10K R27 25 R28 25 C56 750pf BNC1 BNC2

-12.5 Volt Regulator

U23

TPS7A30

OUT IN FB EN GND NR/SS

-12.5 R44 95.3K C75 60pf R45 10K C74 10uf C76 .01 C77 10uf

U12 TLC3704 R36 6.8K R37 4.7K C67 100pf

R38 6.8K R39 4.7K C68 100pf

R40 6.8K R41 4.7K C69 100pf

-13.75 +13.75 -35

CN2

NC NC NC

SDA SCL R34 470 R35 470 C65 100pf C66 100pf

Signal+Noise Peak Detector

+5.0 -5.0

U18 LT1812 R29 1K C57 .1 C58 .1

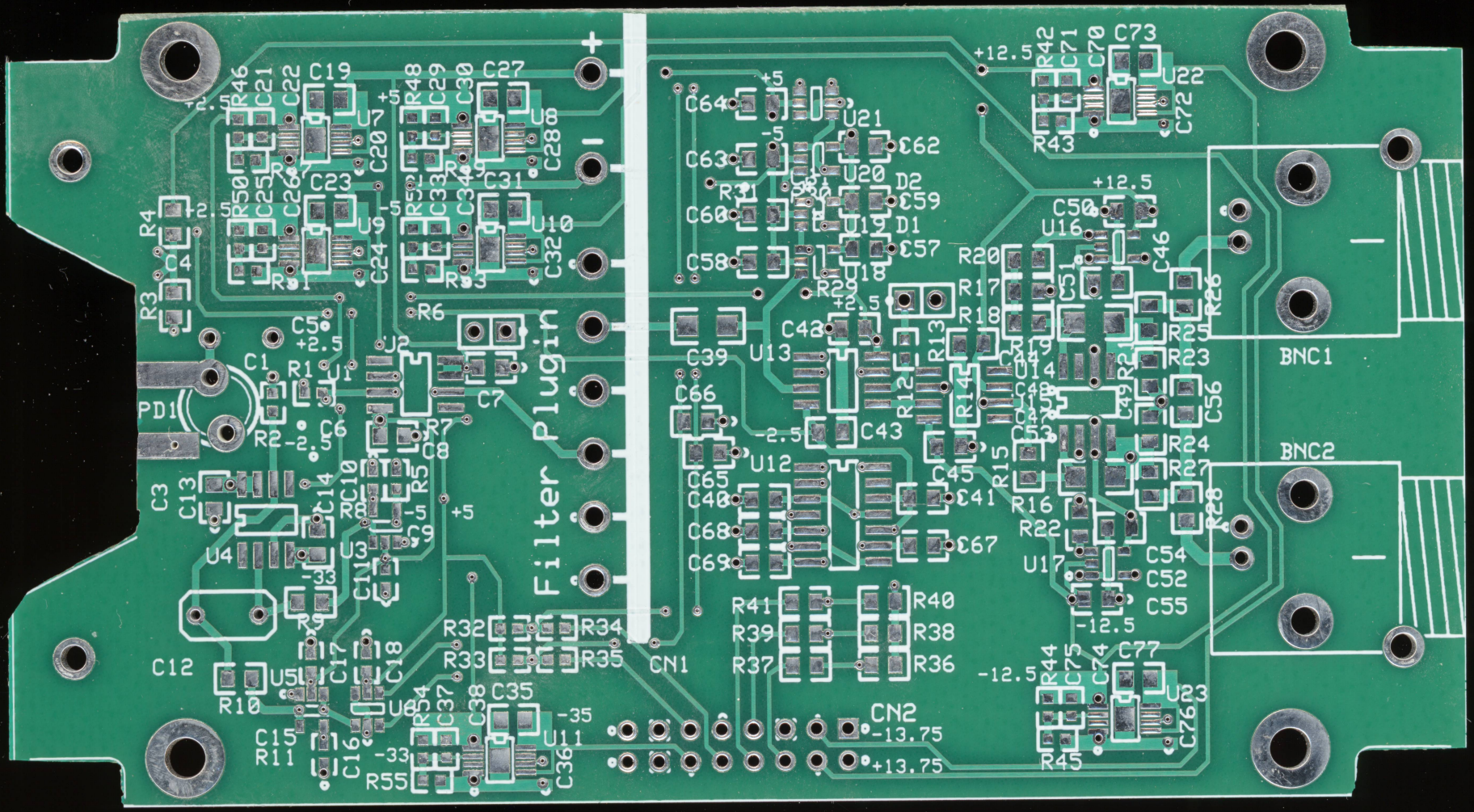
U19 LT1812 C59 .1 C60 .1 D1 DB2S308 D2 DB2S308 R31 1K C61 2.2uf

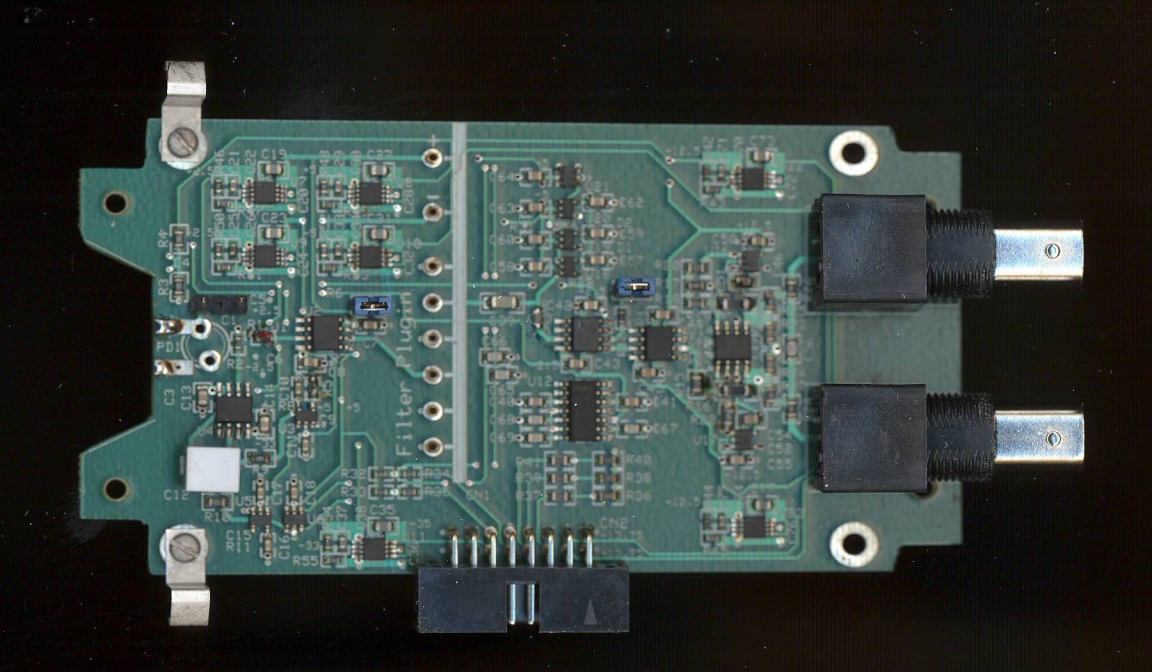
U20 LT1812 C62 .1 R30 100K C63 .1

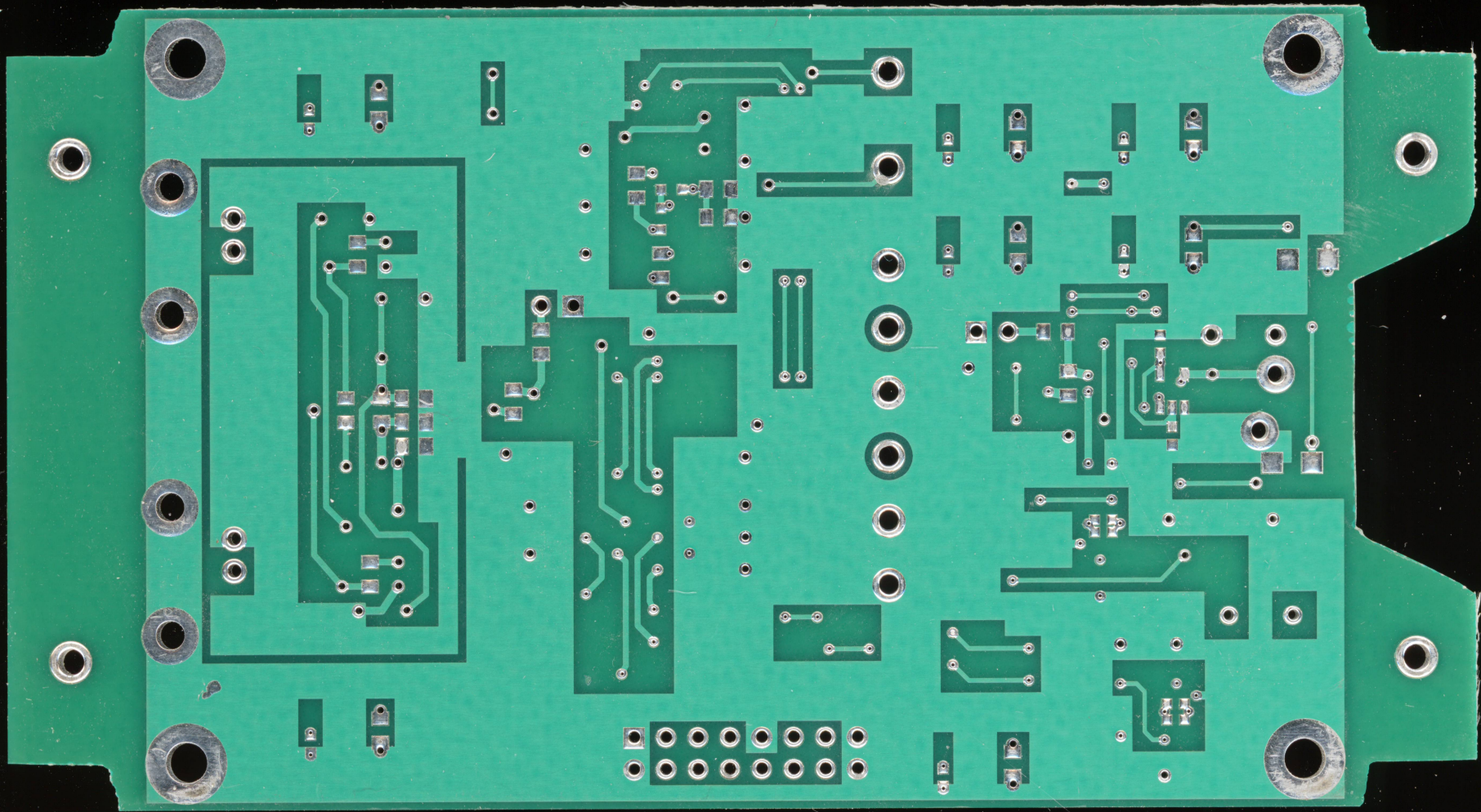
U21 ADS1000 C64 .1 R32 10K R33 10K

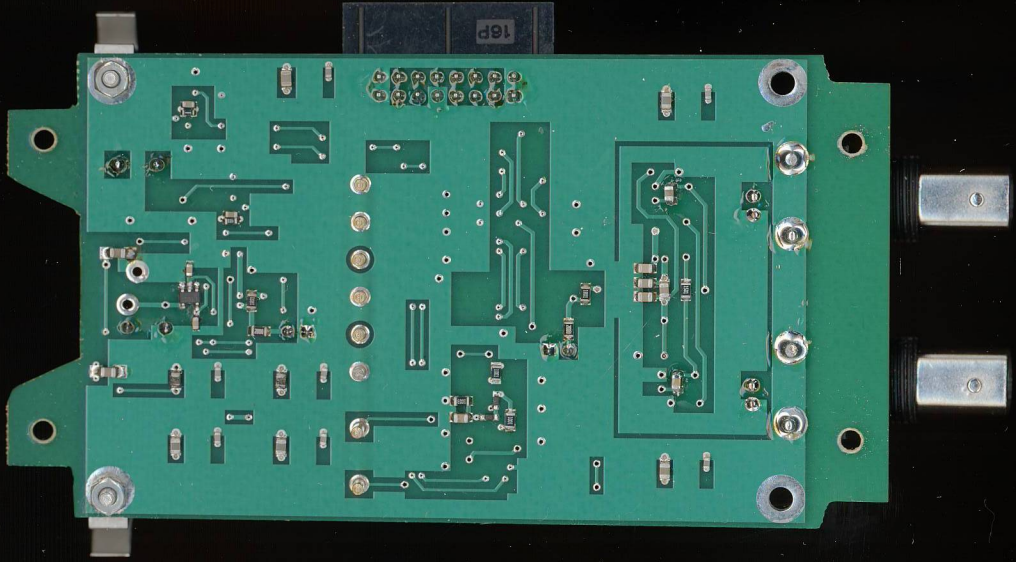
Device A1

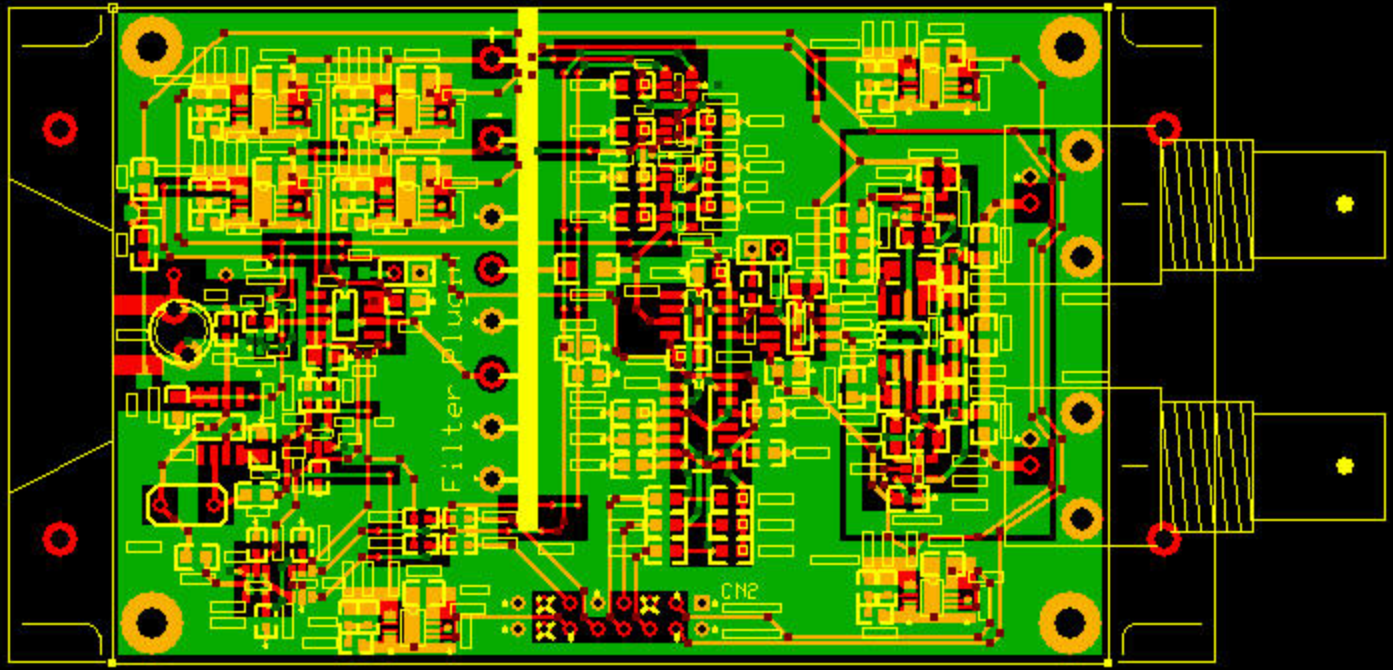
Kent State University		
Photo Diode Amplifier		
Alan R. Baldwin	Rev 1.0 10/25/2018	2 of 2

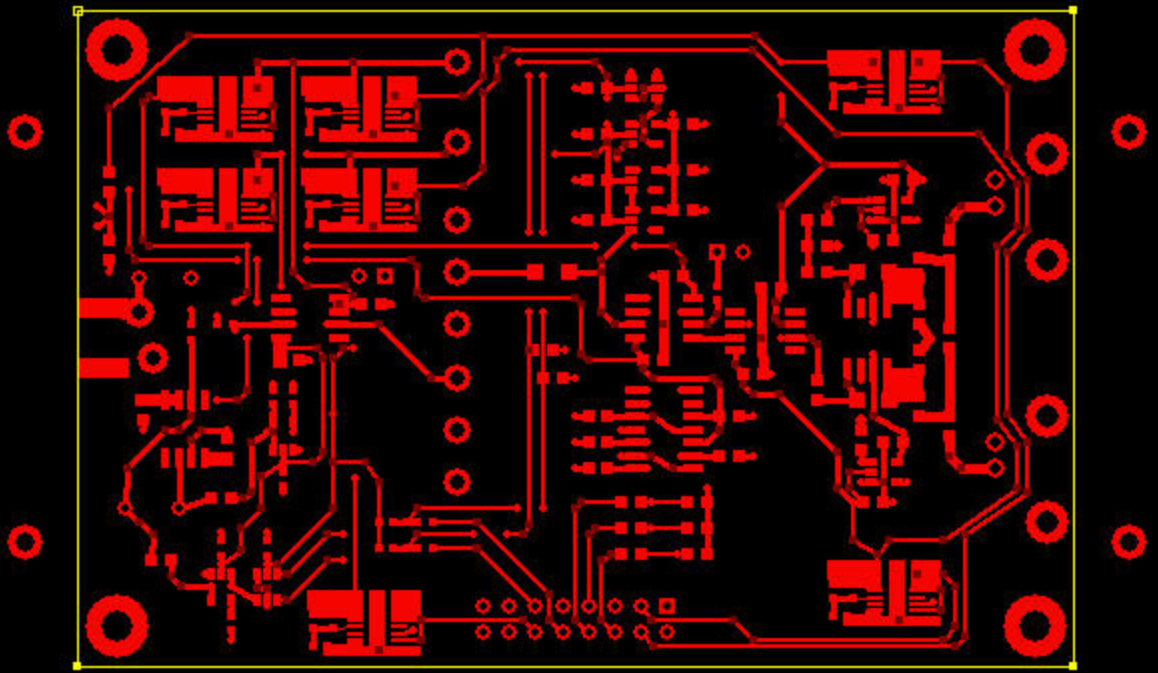

Filter Plugin
PD1
BNC1
BNC2
CN1
CN2
+2.5
-2.5
+5
-5
-33
+35
+12.5
-12.5
-13.75
+13.75

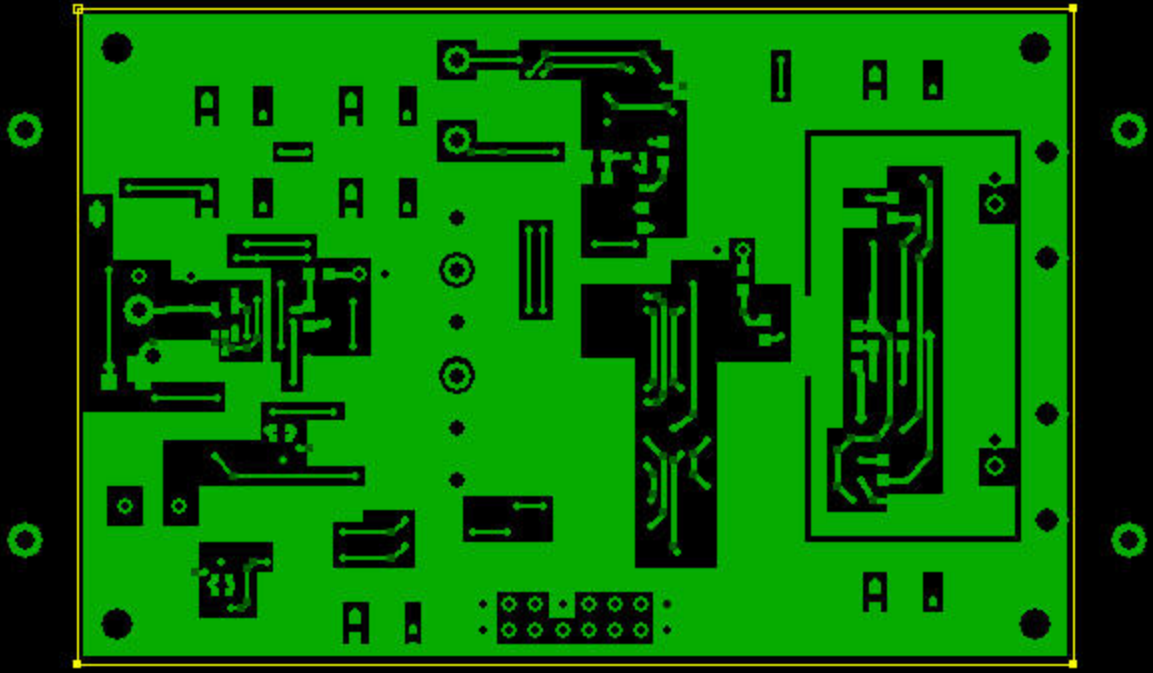

Filter Plugin
PDI

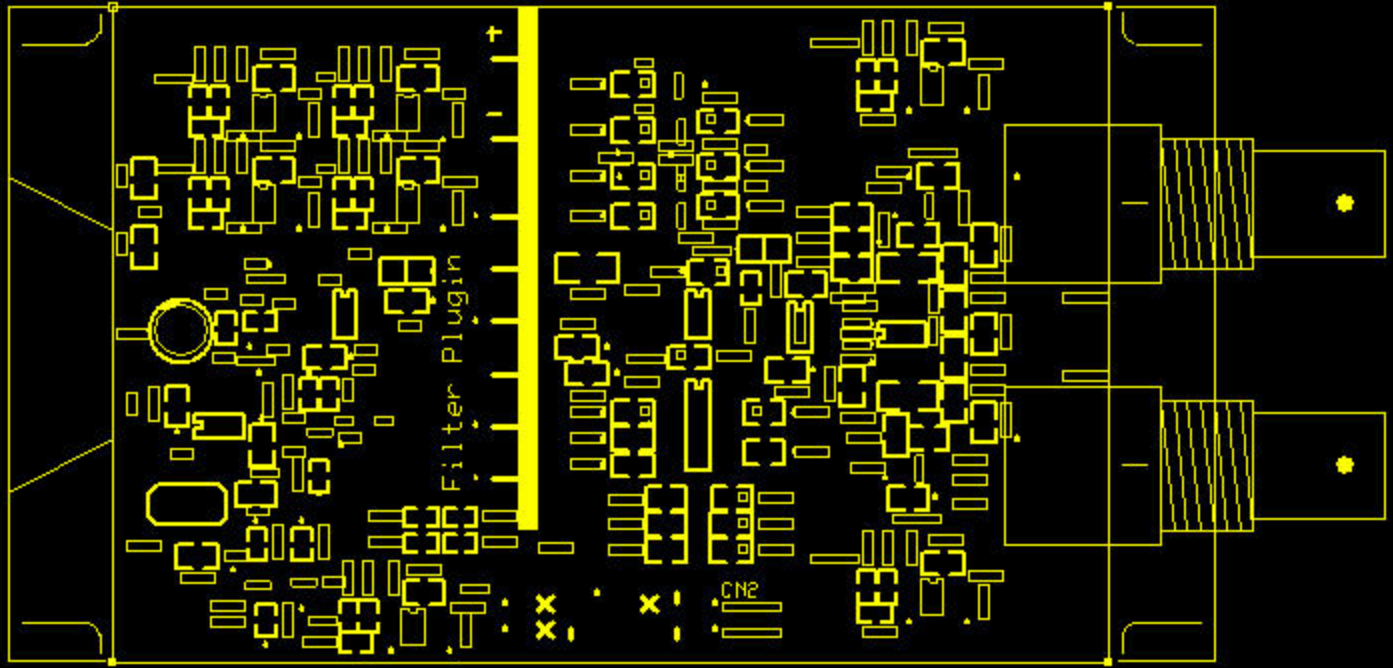


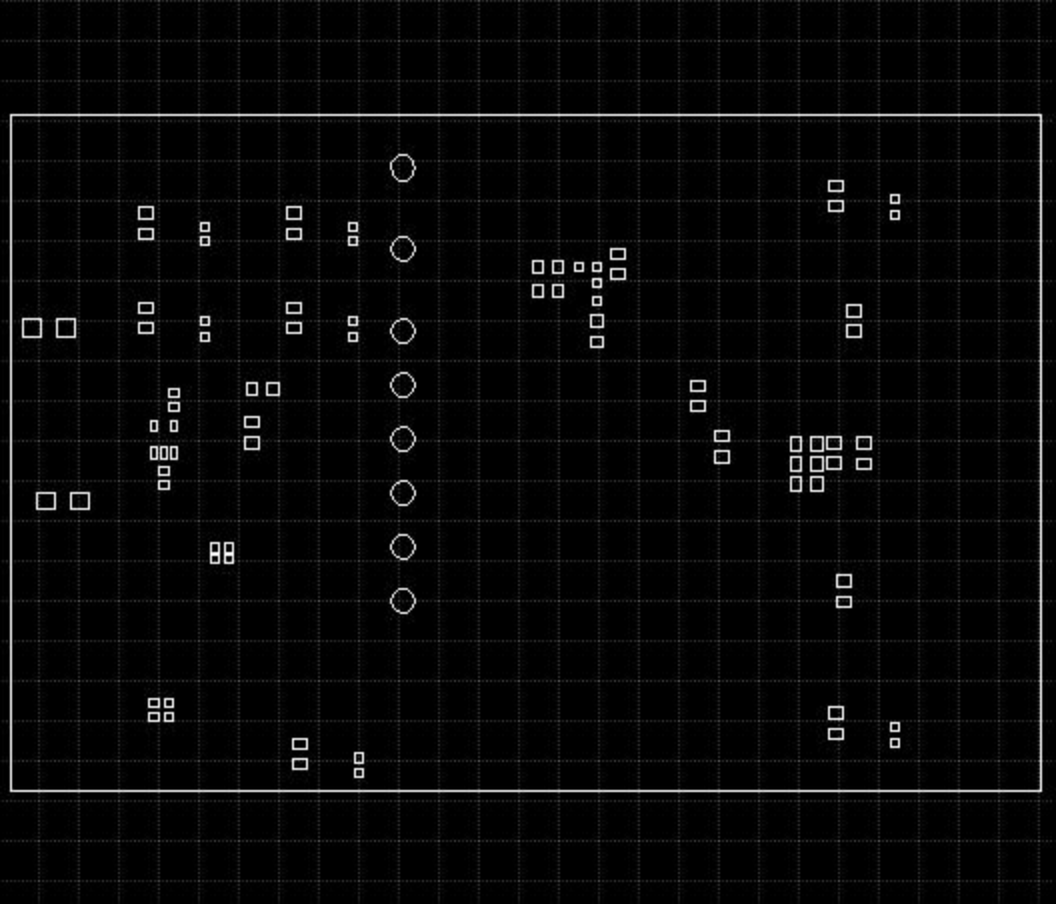

16P


Filter Fluor
CN2






Filter Plugin
CN2



PDIO-01

24V/.5A

T I A

Power & Control

Mini-USB

ARB-2019

TransImpedance Amplifier

PhotoDiode

+

-

Differential Output

Jumpered Gain: 10^6 to 10^9

Adjustable Gain: 0.01 to 1.00

Plugin Bandpass Filter

ARB-2019

PDIO-01

24V/.5A

T I A

Power & Control

Mini-USB

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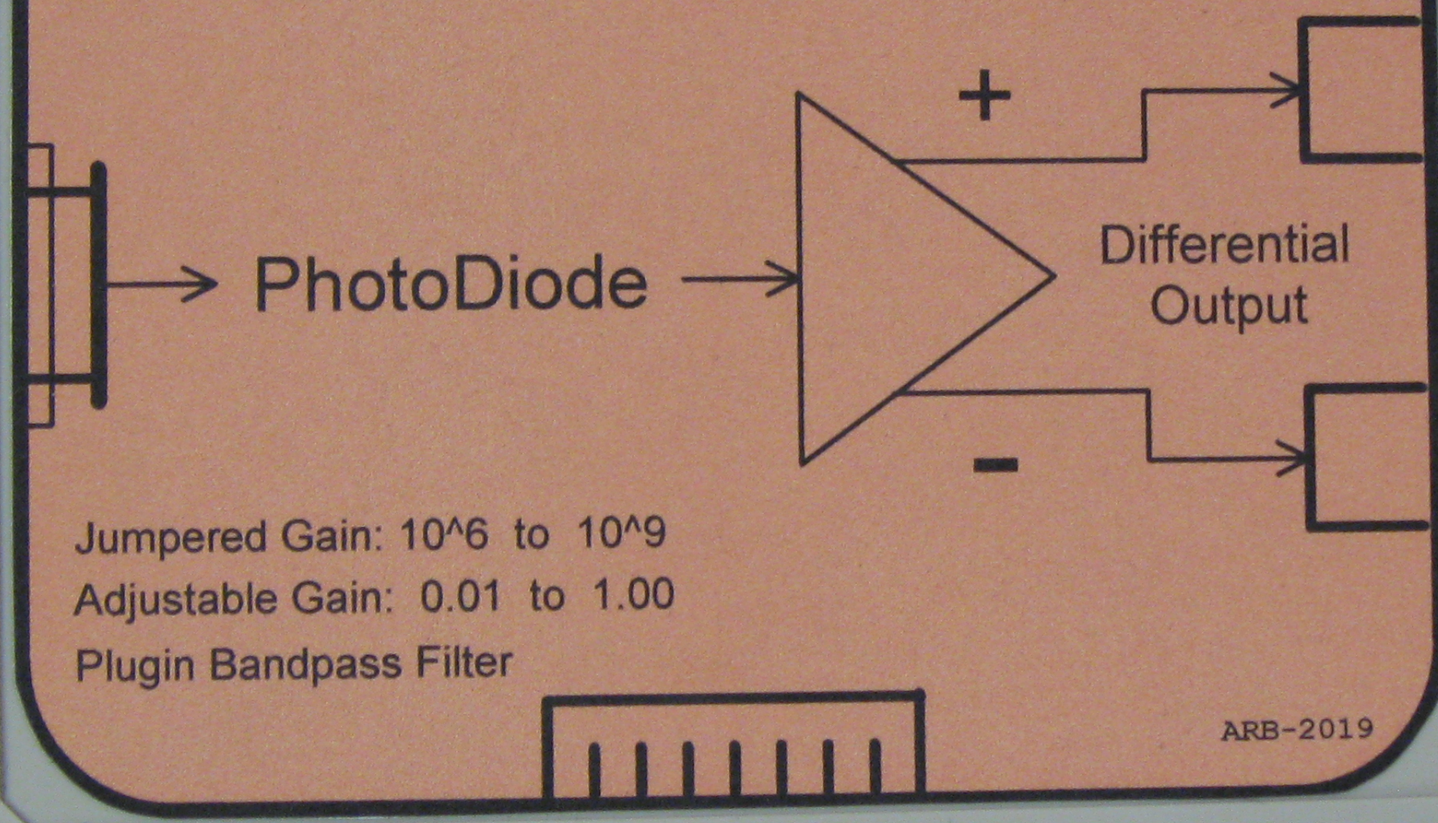
ARB-2019

TransImpedance Amplifier



Jumpered Gain: 10^6 to 10^9
Adjustable Gain: 0.01 to 1.00
Plugin Bandpass Filter

ARB-2019

TransImpedance Amplifier

PhotoDiode

+

-

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Output

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ABB~2019

TransImpedance Amplifier

+

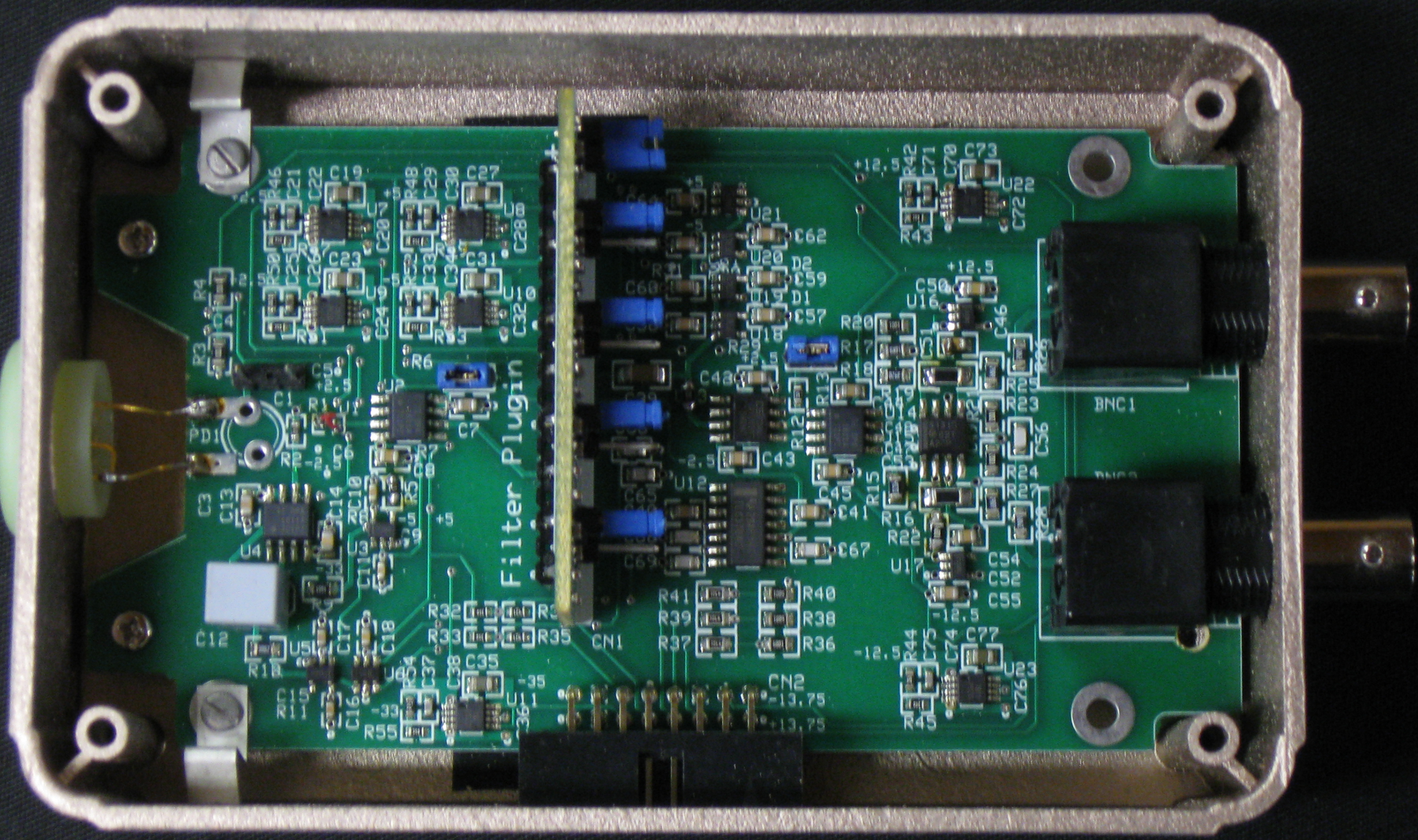
-

PhotoDiode

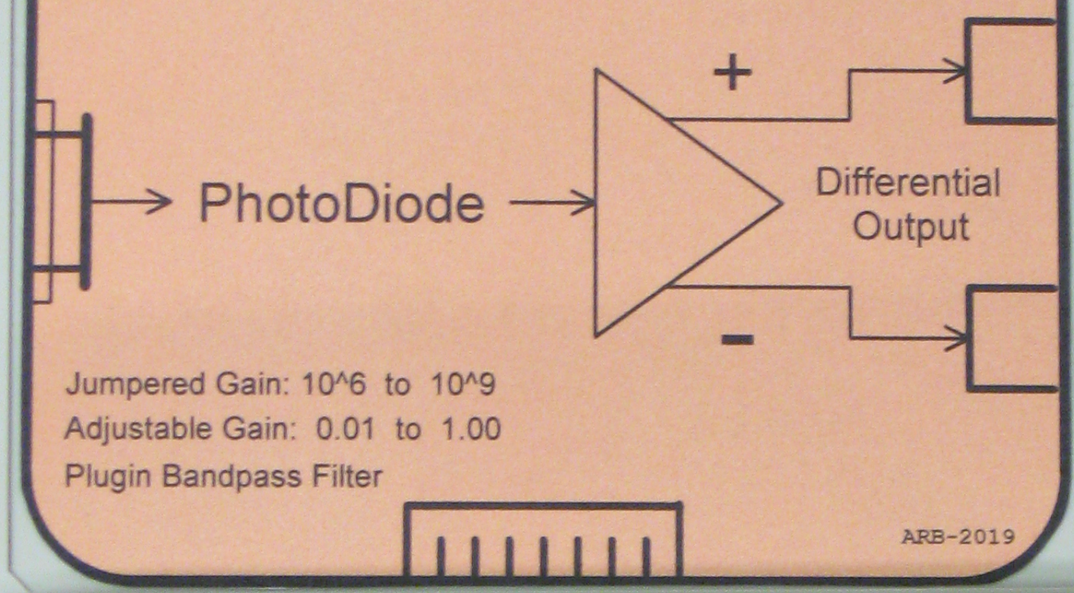
Differential
Output

Jumpered Gain: 10^6 to 10^9
Adjustable Gain: 0.01 to 1.00
Pluge Bandpass Filter

ABB–2019

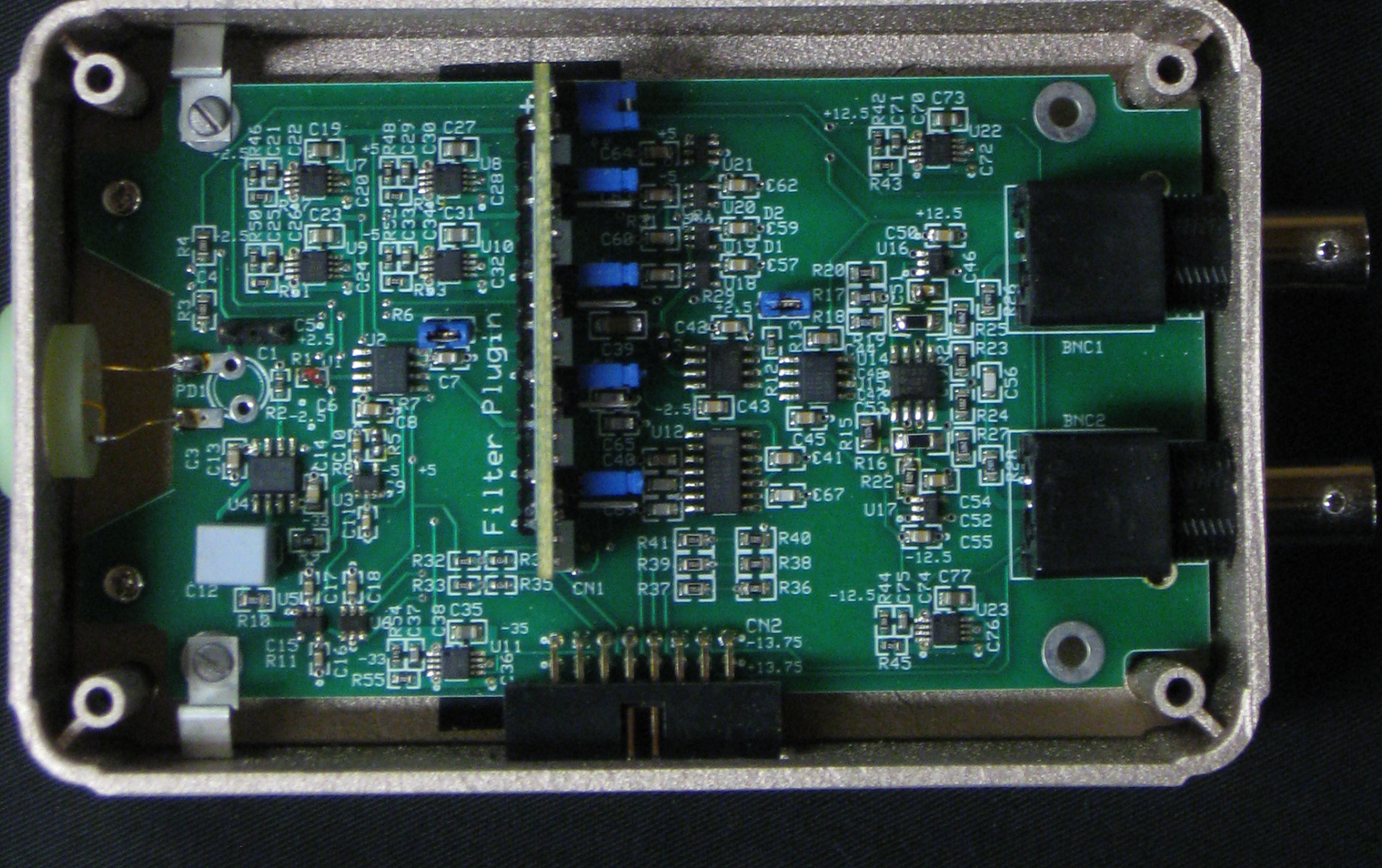

Filter Plugin
PD1
BNC1
CN1
CN2
+12.5
-12.5
+5
-5
-2.5
-33
-35
-13.75

TransImpedance Amplifier



Jumpered Gain: 10^6 to 10^9
Adjustable Gain: 0.01 to 1.00
Plugin Bandpass Filter

ARB-2019



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NOISE ANALYSIS OF FET TRANSIMPEDANCE AMPLIFIERS

The availability of detailed noise spectral density characteristics for the OPA111 amplifier allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

Noise in the OPA111 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2.

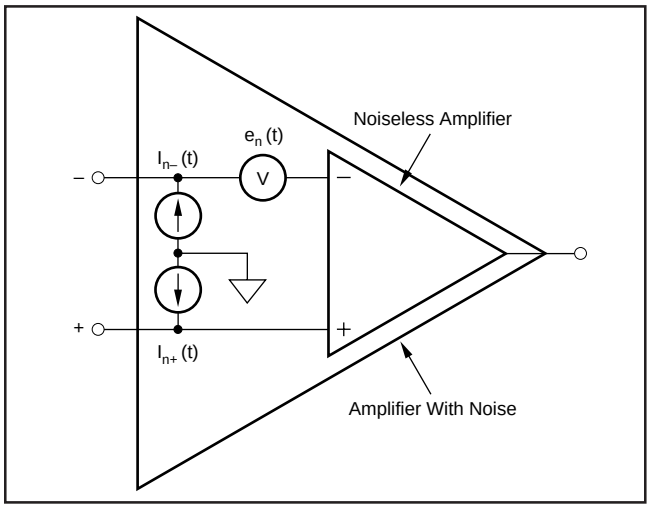

FIGURE 1. Noise Model of OPA111.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same *direct* way to computer noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average—most commonly the rms value.

$$N\ rms \stackrel{\Delta}{=} \sqrt{1/T \int_Q^T n^2(t)\, dt} \qquad (1)$$

where N rms is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

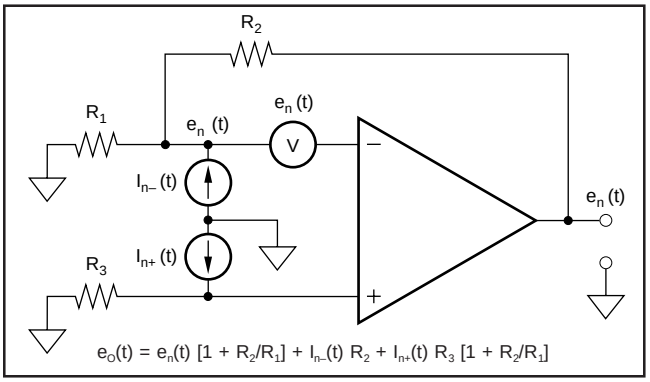

FIGURE 2. Circuit With Error Sources.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL}\ rms = \sqrt{N_1^2\ rms + N_2^2 rms + N_3^2\ rms} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

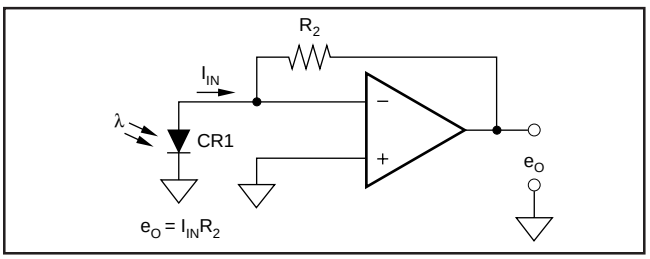

FIGURE 3. Pin Photo Diode Application.

Printed in U.S.A. February, 1994

SBOA060

CR1 is a PIN photodiode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{IN} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

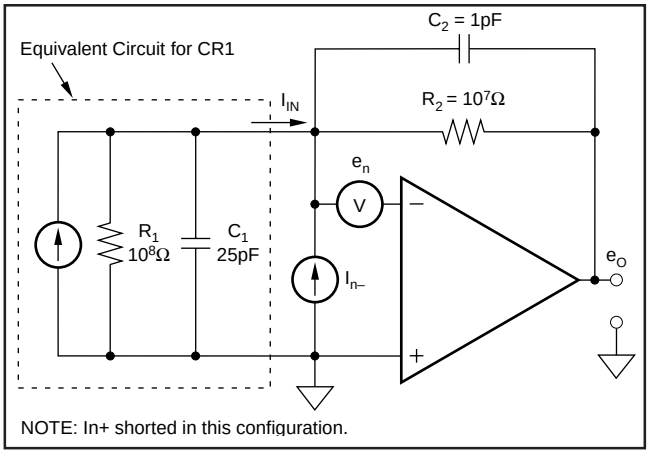

FIGURE 4. Noise Model of Photodiode Application.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$, respectively. These are shown in Figure 5.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_O/i_{IN} = Z_2(s)$). It has a single-pole rolloff at $f_2 = 1/(2\pi R_2 C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{IN} full scale) and maximum output (e_O max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

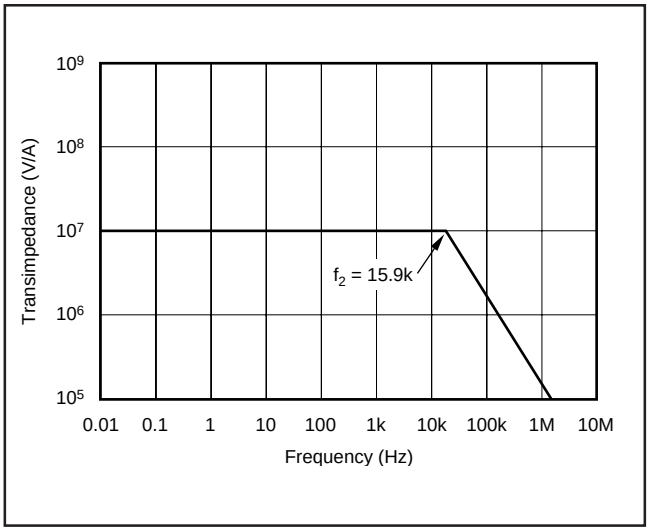

FIGURE 6. Transimpedance.

VOLTAGE NOISE

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_O = e_n\left[\frac{A}{1+A\beta}\right] = e_n\,\frac{1}{\beta}\left[\frac{1}{1+\frac{1}{A\beta}}\right] \qquad (3)$$

where:

A = $A(\omega)$ is the open-loop gain.

β = $\beta(\omega)$ is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

$A\beta$ = $A(\omega)\,\beta(\omega)$ is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

Note that for large loop gain ($A\beta >> 1$)

$$e_O \cong e_n\,\frac{1}{\beta} \qquad (4)$$

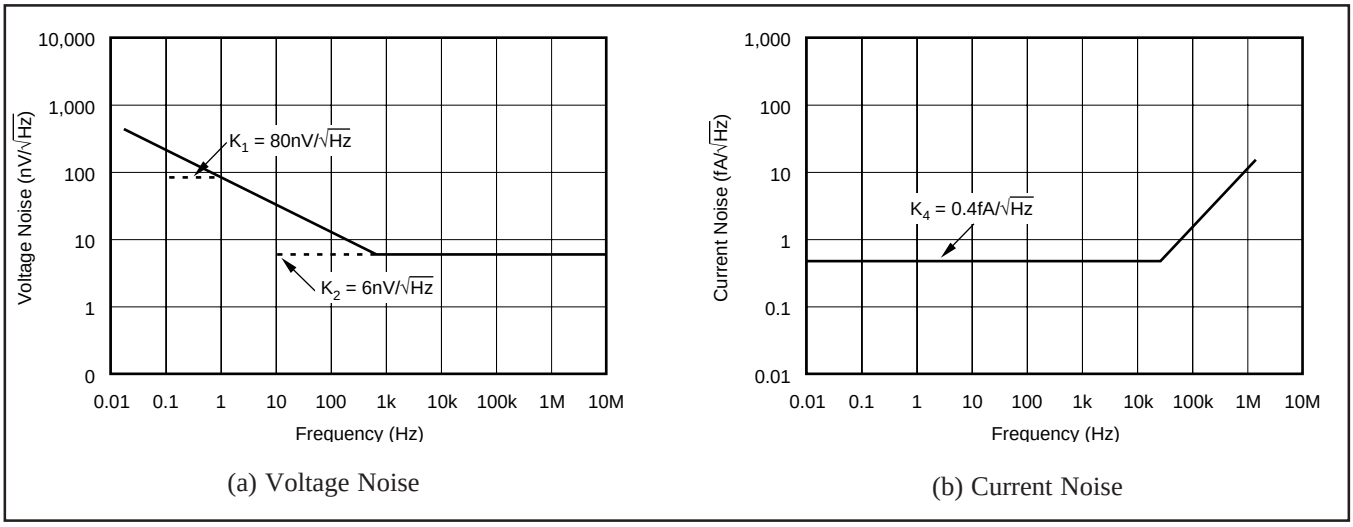

FIGURE 5. Noise Voltage and Current Spectral Density.

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2\left(R_1C_{1S}+1\right)}{R_1\left(R_2C_{2S}+1\right)} \tag{5}$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2 + R_1}{R_1'}\left[\frac{\tau_A s + 1}{\tau_2 s + 1}\right] \tag{5a}$$

where $\tau a = (R_1 \parallel R_2)\,(C_1 \parallel C_2)$

$$\frac{1}{\beta} = \left[\frac{R_1R_2}{R_1 + R_2}\right](C_1 + C_2) \tag{5b}$$

and $\tau_2 = R_2C_2$. (5c)

$$\text{Then, } f_a = \frac{1}{2\pi\,\tau_a} \text{ and } f_2 = \frac{1}{2\pi\,\tau_2} \tag{5d}$$

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}. \tag{6}$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2}. \tag{7}$$

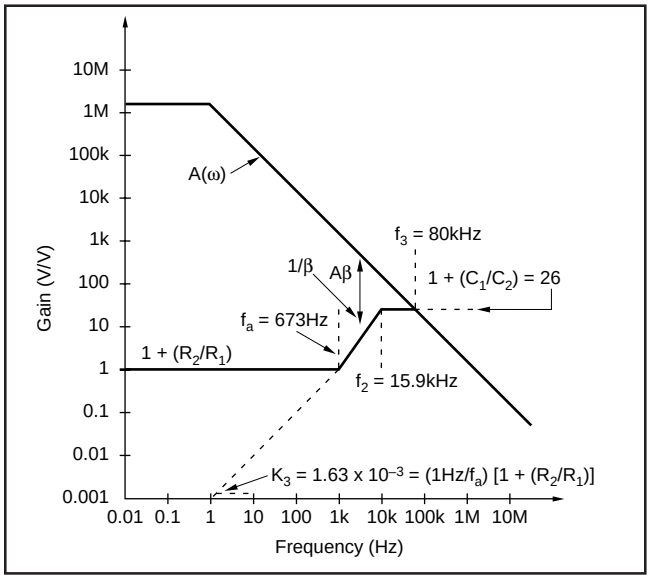

FIGURE 7. Noise Voltage Gain.

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales, the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

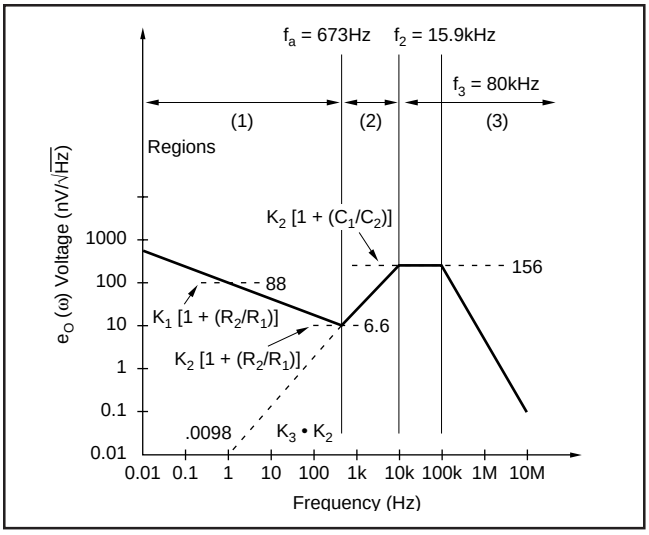

FIGURE 8. Output Voltage Noise Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_O(\omega)$ function in Figure 8 with the following expression:

$$E_O \text{ rms} = \sqrt{\int_{-\infty}^{+\infty} e_O{}^2(\omega)\, d\omega} \tag{8}$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the three regions indicated in Figure 8.

Region 1; $f_1 = 0.01\text{Hz}$ to $f_C = 100\text{Hz}$

$$E_{n1} \text{ rms} = K_1\left[1 + \frac{R_2}{R_1}\right]\sqrt{\ell n\left(\frac{f_C}{f_1}\right)} \tag{9}$$

$$= 80\text{nV}/\sqrt{\text{Hz}}\left[1 + \frac{10^7}{10^8}\right]\sqrt{\ell n\left(\frac{100}{0.01}\right)} \tag{9a}$$

$$= 0.267\mu\text{V}$$

This region has the characteristic of 1/f or "pink" noise (slope of –10dB per decade on the log-log plot of $e_n\omega$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_1 several decades lower. Note that $K_1\,(1 + R_2/R_1)$ is the value of e_O at f = 1Hz.

Region 2; $f_a = 673\text{Hz}$ to $f_2 = 15.9\text{kHz}$

$$E_{n2} \text{ rms} = K_2 \bullet K_3\sqrt{\frac{f_2{}^3}{3} - \frac{f_a{}^3}{3}} \tag{10}$$

$$= \left(6\text{nV}/\sqrt{\text{Hz}}\right)(1.63\times10^{-3})\sqrt{\frac{(15.9\text{kHz})^3}{3} - \frac{(673)^3}{3}} \tag{10a}$$

$$= 11.3\mu\text{V} \tag{9}$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 \parallel R_2$ and the capacitance (C_1 + C_2). Note that $K_3 \bullet K_2$ is the value of the e_O (ω) function for this segment projected back to 1Hz.

Region 3; f > 15.9kHz

$$E_{n3}\ \text{rms} = K_2\left(1+\frac{C_1}{C_2}\right)\sqrt{\left(\frac{\pi}{2}\right)f_3 - f_2} \quad (11)$$

$$= \left(6\text{nV}/\sqrt{\text{Hz}}\right)\left(1+\frac{25}{1}\right)\sqrt{\left(\frac{\pi}{2}\right)(80\text{k}) - 15.9\text{k}} \quad (11a)$$

$$= 51.7\mu\text{V}$$

This is a region of white noise with a single order rolloff at f_3 = 80kHz caused by the intersection of the 1/β curve and the open-loop gain curve. The value of 80kHz is obtained from observing the intersection point of Figure 7. The π/2 applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

CURRENT NOISE

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \quad (12)$$

where $Z_2(s) = R_2 \parallel X_{C2}$ (12a)

This voltage may be obtained by combining the information from Figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9.

Using the same techniques that were used for the voltage noise:

Region l; 0.1Hz to 10kHz

$$E_{ni1} = 4\times10^{-9}\sqrt{10\text{k} - 0.1} \quad (13)$$

$$= 0.4\mu\text{V}$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 4\times10^{-13}\sqrt{\frac{(15.9\text{kHz})^3}{3} - \frac{(10\text{kHz})^3}{3}}$$

$$= 0.4\mu\text{V} \quad (13a)$$

Region 3; f > 15.9kHz

$$E_{ni3} = 6.36\times10^{-9}\sqrt{\frac{\pi}{2}(80\text{kHz}) - 15.9\text{kHz}}$$

$$= 2.1\mu\text{V} \quad (13b)$$

$$E_{ni\ \text{TOTAL}} = 10^{-6}\sqrt{(0.4)^2 + (0.4)^2 + (2.1)^2}$$

$$= 2.2\mu\text{Vrms} \quad (13c)$$

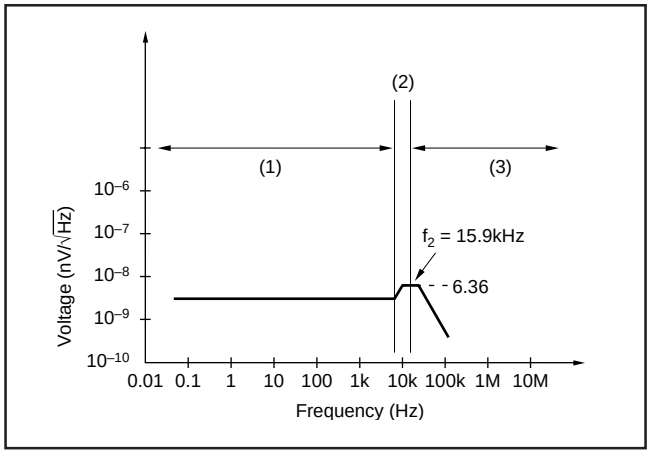

FIGURE 9. Output Voltage Due to Noise Current.

RESISTOR NOISE

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_R\ \text{rms} = \sqrt{4\text{kTRB}} \quad (14)$$

K = Boltzmann's constant = 1.38 x 10^{-23} Joules/°Kelvin
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

$$E_R\ \text{rms} \cong 0.13\sqrt{\text{RB}}$$

E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4

$$R_2 = 10^7\Omega = 10\text{M}\Omega$$

$$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2}15.9\text{kHz}$$

Then

$$E_R\ \text{rms} = \left(411\text{nV}/\sqrt{\text{Hz}}\right)\sqrt{B}$$

$$= \left(411\text{nV}/\sqrt{\text{Hz}}\right)\sqrt{\frac{\pi}{2}15.9\text{kHz}}$$

$$= 64.9\mu\text{Vrms}$$

TOTAL NOISE

The total noise may now be computed from

$$E_{n\,TOTAL} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{nR}^2 + E_{ni}^2} \quad (15)$$

(15a)

$$= 10^{-6}\sqrt{(0.293)^2 + (11.3)^2 + (51.7)^2 + (64.9)^2 + (2.2)^2}$$

$$= 83.8\mu Vrms$$

CONCLUSIONS

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions.

The largest component is the resistor noise E_{nR} (60% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

The second largest component of total noise comes from E_n^3 (38%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

It should be noted that increasing C_2 will also lower the value of $K_2(1 + C_1/C_2)$, and the value of f_2 (see equation 5b). This reduces signal bandwidth and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 0.1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{CHARACTERISTIC} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz$$

$$= \frac{6nV/\sqrt{Hz}}{0.4fA\sqrt{Hz}}$$

$$= 15M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

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Application Report
SNOA942A–November 2015–Revised May 2017

Transimpedance Amplifiers (TIA): Choosing the Best Amplifier for the Job

Hooman Hashemi

ABSTRACT

This application note is intended as a guide for the designer looking to amplify the small signal from a photodiode or avalanche diode so that it would be large enough for further processing (e.g. data acquisition) or to trigger some other event in a system. The challenge in doing so, as always, is to not degrade the signal such that it becomes indistinguishable from random noise and to maintain enough signal bandwidth so that "information" is preserved. We will present some ideas on this and develop analysis and optimization techniques, as well as list the devices with the most desirable specifications for such applications.

Explore TI transconductance amplifiers

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1 General Considerations

As it turns out, selecting the best operational amplifier to interface to the photodiode is a juggling act between many parameters, some significant while others less so; for now, suffice to say that the lowest noise voltage device is *not always* the winner. We will discuss the tradeoffs further in this document.

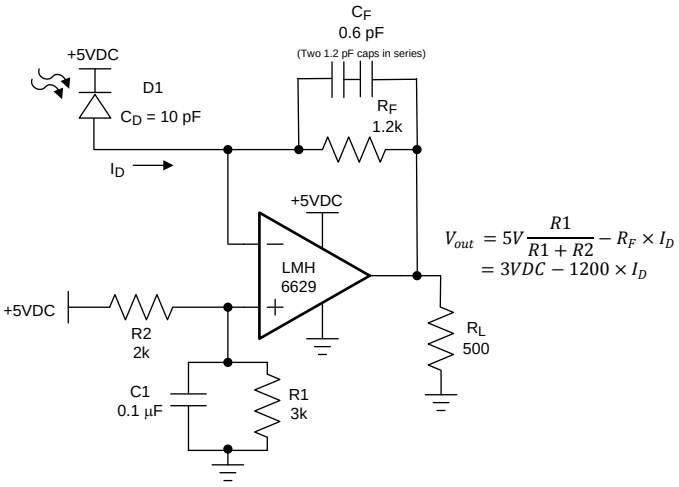

Figure 1. Basic TIA Configuration Using and Ultra-Low Noise Device (LMH6629)

Often times, the transducer (Photodiode) is chosen based on its form factor or electrical characteristics and the following need to be determined:

(a) How much gain is needed?

(b) What bandwidth has to be achieved?

(c) What is the highest noise than can be tolerated?

In most cases, since the photodiode signal is usually very small, the 1st TIA stage is followed by subsequent gain stage(s) to optimize the balance between noise and bandwidth. Photodiode manufacturers specify how much current can be generated for a certain incident light power. A large area photodiode produces more current in response to incident light, at the expense of higher capacitance (and hence lower speed).

So, knowing the final voltage level desired, based on the specifics of what needs to be driven (e.g. input of ADC, logic gate, etc.), the "total" signal path gain can be nailed down. Set the 1st Transimpedance stage gain too high, and you will limit the attainable bandwidth for the signal spectrum at hand. On the other hand, not enough gain degrades SNR and leaves you with too much gain to make up for and unnecessary cost, complexity, and possible signal degradation. Inherent in the question of the what gain to run the 1st stage, is the second order effect of the photodiode capacitance causing excessive noise gain increase at the higher frequencies (more on that later).

The equations in Figure 2 define the value of the compensation capacitor (C_F) as a function of the Operational Amplifier Gain Bandwidth Product (GBWP), Transimpedance gain (R_F), and the total input capacitance (C_{IN}) where:

$$C_{IN} = C_D + C_{CM} + C_{DIFF} \quad (1)$$

where:

C_D : Photodiode capacitance
C_{CM} : Amplifier common mode capacitance (each input to ground)
C_{DIFF} : Amplifier differential mode capacitance (across the inputs)

Optimum CF Value:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}}$$

Resulting -3dB Bandwidth:

$$f_{-3\,dB} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}}$$

Figure 2. TIA Compensation Capacitor (C_F) and Subsequent Bandwidth (f_{-3dB})

The attainable -3dB bandwidth (f_{-3dB}) can also be inferred from Figure 2.

2 Equivalent Input Noise Source Modeling

The highest noise that can be tolerated should be at least a few dB lower than the smallest signal present. It is a common technique to utilize noise analysis, using hand calculation or alternatively a simulation tool such as TINA-TI, on the entire signal path in order to make sure the noise level is below this limit. Often times, this is done with “input referred noise” modeled as a noise source next to the input such that it is possible to directly compare the signal and the noise level with each other. Refer to Figure 3 for the depiction of this input referred source “i_{ni}”.

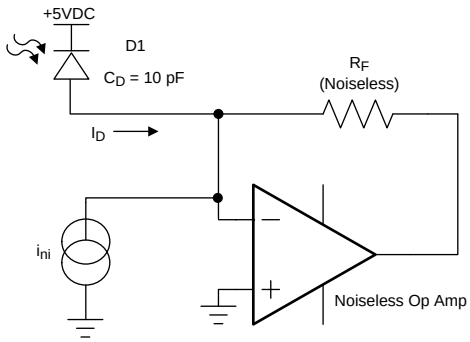

Figure 3. Transimpedance Amplifier Equivalent Input Source (i_{ni}) Model

Referring all noise sources to the input allows immediate SNR evaluation and highlights the “dominant noise” source, which can be an effective tool in any attempt at improving SNR by tackling the most offensive noise source(s).

The expression for i_{ni} is derived within the “*Transimpedance Considerations for High-Speed Amplifiers*” (shown as “i_{EQ}”) and copied below for reference:

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_F}\right)^2 + \frac{4kT}{R_F} + \frac{(e_n 2\pi f_{-3dB} C_{IN})^2}{3}} \quad (2)$$

Where:

- i_n = inverting input spot current noise
- $4kT = 16.4 \times 10^{-21}$J at room temperature
- R_F = feedback resistor
- e_n = non-inverting input spot voltage noise
- C_{IN} = Total inverting input total capacitance. See Equation 1
- f_{-3dB} = noise integration frequency limit

The contributing terms to input referred noise current (i_{ni}) in Equation 2 are:

a) Noise Current Term:

$$i_n \quad (3)$$

b) Noise Voltage Term:

$$e_n / R_F \quad (4)$$

c) Thermal Noise Term:

$$\sqrt{\frac{4kT}{R_F}} \quad (5)$$

where $4kT = 16.4E^{-21}$ J at room temperature

d) Input Capacitance Term:

$$\frac{e_n 2\pi f_{-3dB} C_{IN}}{\sqrt{3}} \quad (6)$$

While most of the terms shown may be self-explanatory, the last term needs to be described. This term is the result of the noise increase caused by the presence of the total inverting input capacitance (C_{IN}), which has the net effect of increasing Noise Gain beyond a certain frequency set by R_F and C_{IN}.

The overall SNR can be optimized by the proper choice of operational amplifier, selected gain, and the total signal path gain. With several cascaded stages, it is desirable to take the highest gain at the earliest stage and to minimize its noise contribution since it has the highest impact on SNR. So, for the 1st stage, choose the best operational amplifier (by using the analysis method developed here) while operating at the highest Transimpedance gain possible which still allows the entire spectrum of interest to pass.

3 Optimizing the Device Choice and Operation

For a given operational amplifier GBWP, use the expression in Figure 2 to pick the highest gain (R_F) that achieves the required bandwidth. If this R_F value causes excessive swing at maximum signal, set R_F to what the maximum signal and voltage swing dictates. A spreadsheet is a good tool to use so that you can evaluate many possible device options side-by-side, given their datasheet specifications and application operating conditions. Next, use the i_{ni} expression in Equation 2 to compute the equivalent input referred noise current and determine if the resulting SNR is adequate for the application at hand. To improve SNR, select a different operational amplifier to try and maximize SNR as much as possible. The individual noise sources in (Equation 3 through Equation 6) can point out which noise source is dominant and should therefore be targeted for reduction to have the maximum impact on SNR.

Let's take an example photodiode and try to find the best amplifier to be used with it while considering all input referred noise sources described earlier:

Example:

- Total input capacitance C_{IN}: 10pF. Note: Device input capacitance not considered (assumed $C_{IN} = C_D$)
- Photodiode signal range: 10nA (Min) to 1uA (Max)
- Required Bandwidth: 80MHz
- Required swing with minimum signal: 1mV

Following the procedure above, and comparing some possible device candidates for the 1st stage amplification, here is what you get:

Table 1. Different Amplifier Candidates Optimized Setting Compared Side-by-Side

Device (1)	GBWP (MHz)(2)	i_n (pA / RtHz)(2)	e_n (nV / RtHz)(2)	R_F (Ohm) (3)	Noise Current Term (pA / RtHz) (4)	Noise Voltage Term (pA / RtHz) (4)	Thermal Noise Term (pA / RtHz) (4)	Input Capacitance Term (pA / RtHz) (4)	SNR (dB)(5)	Post Amp Gain (dB)(6)
THS4631	325	0.002	7	810	0.002	8.7	4.5	20.3(7)	53	42
LMH6629	4,000	2.6	0.69	10k	2.6(7)	0.07	1.3	2(7)	69	20
OPA657	1,600	0.0013	4.8	3.9k	0.0013	1	2	14(7)	57	28

(1) Device input capacitance not considered (assumed $C_{IN} = C_D$)
(2) Datasheet parameter
(3) Selected to meet bandwidth required using Figure 2
(4) Computed using Equation 2
(5) SNR computed as ratio of minimum signal (10nA) to input referred spot noise i_{ni} [= 20 * log(10nA / i_{ni})]
(6) For 1mV final signal with minimum signal
(7) Dominant term

Table 1 results show that the LMH6629 delivers the highest SNR for this application by virtue of its ultra-low input noise voltage (e_n) which is low enough to be a non-factor and also results in a minimal "input capacitance term" as well. In the end, which amplifier gives the best SNR is determined by the specifics of the application or operating conditions and the determining factor depends which of the noise terms dominates. Notice that one must weigh the benefit of the highest SNR against cost, and also the additional post amp gain needed. The small R_F value for THS4631, and the subsequent large post amp gain it

needs, might prohibit this device's application in this particular example. A very important thing to note is that the FET input devices (e.g. THS4631, OPA657, etc.) not only have an inherent noise current advantage over BJT input devices (e.g. LMH6629, etc.), but they also reduce the output offset error that arises from their near zero input bias current working against the feedback resistor R_F. If the operating conditions of this example were different, one might very well end up with a situation where low noise current sets the attainable SNR and thus it would be more appropriate to select a FET input device instead.

4 Post Amplification Effect on SNR

To demonstrate how SNR is affected when the 1st TIA stage is followed by additional non-ideal (noisy) amplifiers to increase signal amplitude to what is needed, let's consider an example shown in Figure 4. In this example, the LMH6629 1st stage from Table 1 is chosen along with a cascade of 6dB voltage gain stages having a NF of 10dB each as post amp. To get 20dB total post amp voltage gain needed, we must use more than 3 cascaded stages. Four cascaded stages are shown in the example below:

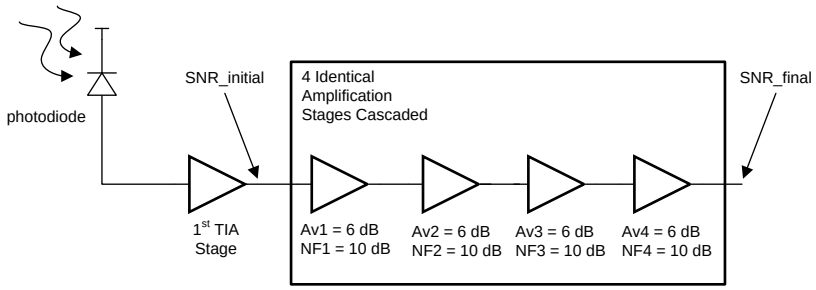

Figure 4. Block Diagram of Entire Signal Path to Compute Overall SNR

The post amp consists of a series of identical cascaded stages of voltage gain (A_v) and Noise figure (NF) each.

Here is the overall Noise Factor (F) expression (known as "Friis Formula") at the post amp output using Power Gain (G_n) and Noise Factor (F_n) of the n stages:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{F_n - 1}{G_1 G_2 G_3 \ldots G_{n-1}} \quad (7)$$

Knowing the entire signal path Noise Figure (NF= 10*log(F)), one can compute the resulting SNR_final with SNR_initial known (69dB in this case from the Table 1 entry for the LMH6629):

$$SNR\_final = SNR\_initial - NF \quad (8)$$

Let's compute G and F from A_v and NF given:

$$G_1 = G_2 = G_3 = G_4 = [10^{(A_v / 20)}]^2 = [10^{(6 / 20)}]^2 = (2)^2 = 4\ (V^2/V^2) \quad (9)$$

$$F_1 = F_2 = F_3 = F_4 = 10^{(NF / 10)} = 10^{(10 / 10)} = 10\ (V^2/V^2) \quad (10)$$

From Equation 7:

$$F = 10 + (10-1) / 4 + (10-1) / 4^2 + (10-1) / 4^3 = 13 \quad (11)$$

Computing NF from knowing F:

$$NF = 10 * \log (13) = 11.1dB \quad (12)$$

From Equation 8:

$$SNR\_final = SNR\_initial - NF = 69dB - 11.1dB = 57.9dB \quad (13)$$

5 Summary

This application note developed some insight into the parameters that affect the TIA most in terms of bandwidth and noise and demonstrated with examples how to compute SNR, and optimize it which in turn allows one to find the most suitable amplifier to use for the 1st TIA stage. Furthermore, the impact of additional amplification on overall SNR was analyzed and evaluated numerically such that the user can keep track of the noise in order to successfully specify and build an optimized photodiode amplifier system.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2015) to A Revision	Page
• Added link for Explore TI transconductance amplifiers	1

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Application Report
SBOA122–November 2009

Transimpedance Considerations for High-Speed Amplifiers

Xavier Ramus *High-Speed Products*

ABSTRACT

Designing high-resolution detection circuits using photodiodes presents considerable challenges because bandwidth, gain, and input-referred noise are coupled together. This application note reviews the basic issues of transimpedance design, provides a set of detailed design equations, explains those equations, and develops an approach to easily compare potential solutions.

Contents

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1 Introduction

The purpose of a transimpedance circuit is to convert an input current from a current source (typically a photodiode) into an output voltage. The simplest method to achieve this conversion is to use a resistor connected to ground. However, the achievable gain using this method is limited by the following factors:

1. The current source input impedance;
2. The load impedance; and
3. Desired bandwidth.

A closed-loop approach, using an operational amplifier, is normally beneficial to most applications as it has the potential of eliminating those issues. A typical circuit with all necessary components for this analysis is shown in Figure 1. In this circuit, the generator is a photodiode, whose role is to convert the photons into a current. This current is then amplified by the feedback resistor R_F. Working with an ideal amplifier for now, we can see that because no bias current is present, all the signal generated by the photodiode is going to be converted to the output. Note that the source impedance is not of interest here; it is isolated from the output. Note also that the output is low impedance, allowing a wide variety of load to be connected. The bandwidth is going to be a function of the source capacitance (C_S), the feedback capacitance (C_F), and the gain bandwidth product of the actual amplifier used.

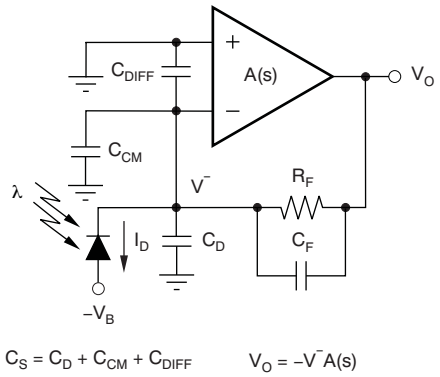


Figure 1. Transimpedance Circuit with Modeled Elements

The source capacitance (C_S) is the sum of the photodiode capacitance (C_D), the common-mode capacitance of the amplifier (C_{CM}), and the differential capacitance of the amplifier (C_{DIFF}). C_{CM} and C_{DIFF} include both the board layout and the op amp parasitic capacitance.

2 Stability Analysis

The first non-ideal op-amp characteristic we examine here is the non-infinite open-loop gain. The architecture for the operational amplifier used in the rest of this application report is a single pole op-amp model, as shown in Equation 1. This model allows us to analyze the resulting transimpedance design as a second-order, closed-loop transfer function.

$$A(s) = \frac{A_{OL} \cdot \omega_A}{s + \omega_A} \tag{1}$$

Expressing the Laplace transfer function in Bode analysis form yields the following equation.

$$\frac{V_O}{I_D} = \frac{-Z_F}{1 + \left(\frac{1 + \frac{Z_F}{Z_G}}{A(s)} \right)} \tag{2}$$

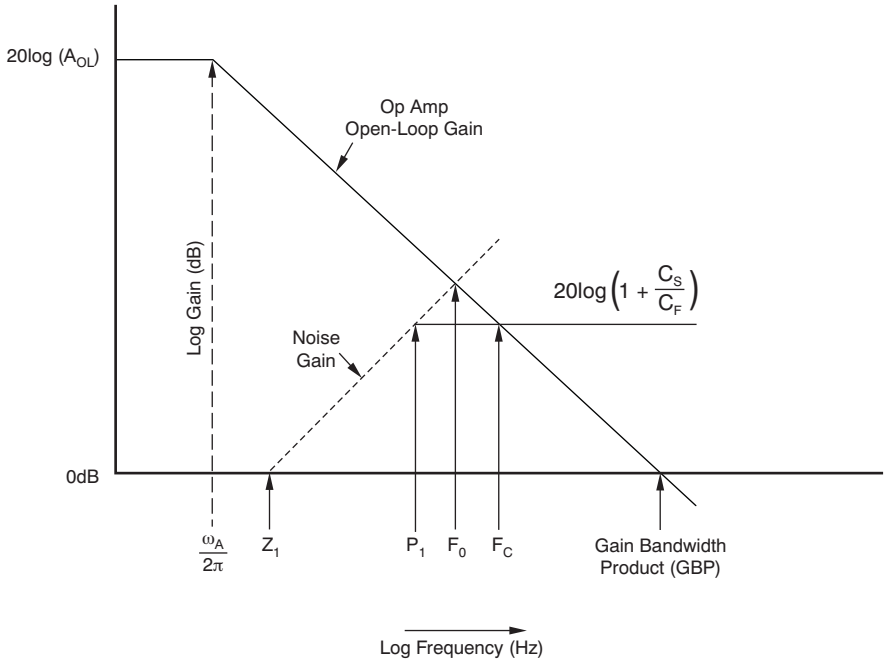
where:

$$Z_F = R_F \parallel \frac{1}{s \cdot C_F} = \frac{\frac{1}{C_F}}{s + \frac{1}{R_F \cdot C_F}} \quad (3)$$

$$Z_G = \frac{1}{s \cdot C_S} \quad (4)$$

At dc, and if the open-loop gain of the amplifier is infinite, the amplifier gain is set by the feedback resistor. This effect can be seen by setting s = 0 in Equation 3 and plugging the result into Equation 2 while setting A(s) = ∞.

$1 + \frac{Z_F}{Z_G}$ is the noise gain. The loop gain is the difference between the open-loop gain (A_{OL}) and the noise gain. The noise gain is plotted in Figure 2 alongside the single pole, open-loop gain model of the amplifier.



$$Z_1 = \frac{1}{2\pi R_F (C_S + C_F)} \text{ Hz}$$

$$P_1 = \frac{1}{2\pi R_F C_F} \text{ Hz}$$

$$F_0 = \sqrt{Z_1 \cdot GBP}$$

$$F_C = \frac{GBP}{\left(1 + \frac{C_S}{C_F}\right)}$$

Figure 2. Bode Plot Magnitude

At dc, the gain is indeed the expected transimpedance gain R_F, while at high frequency, it is $1 + \frac{C_S}{C_F}$. Note that only the feedback capacitor (C_F) and the source capacitance (C_S) are used for stability; consequently, it can be noted that a unity-gain stable amplifier is not necessary for transimpedance applications. In fact, it is recommended to use a decompensated amplifier instead, because these decompensated amplifiers offer better voltage noise specifications and larger gain bandwidth products than any compensated version. This fact is easily illustrated by two families of devices: the OPA842/3/6/7 and the OPA656/7. The OPA842 is unity-gain stable and has 2.7nV/√Hz input voltage noise. The OPA843 is stable for gains greater than 3V/V and has a voltage noise of 2nV/√Hz. The OPA846 is stable for gains greater than 7V/V and has a 1.2nV/√Hz voltage noise. Finally, the OPA847 has a voltage noise of 0.85nV/√Hz and is stable for gains greater than 12V/V. For FET devices such as the OPA656 and OPA657, the OPA656 provides unity-gain stability with a 7nV/√Hz input voltage noise; the OPA657 has a 4.8nV/√Hz voltage noise, but is stable for gains greater than 7V/V.

Coming back to the analysis and expressing the full transfer function as a function of ω_o and Q.—given in Equation 5 with Equation 6 and Equation 7 expressing ω_o and Q with physical elements of the circuit —yields the following results:

$$\frac{V_O}{I_D} = R_F \bullet \frac{A_{OL}}{A_{OL} + 1} \bullet \frac{\omega_o^2}{s^2 + s \bullet \frac{\omega_o}{Q} + \omega_o^2} \tag{5}$$

$$\omega_o = 2\pi \bullet F_0 = \sqrt{\frac{(A_{OL} + 1) \bullet \omega_A}{R_F \bullet (C_S + C_F)}} \tag{6}$$

$$Q = \frac{\sqrt{\frac{(A_{OL} + 1) \bullet \omega_A}{R_F \bullet (C_S + C_F)}}}{\omega_A \bullet \left(1 + A_{OL} \bullet \frac{C_F}{C_S + C_F}\right) + \frac{1}{R_F \bullet (C_S + C_F)}} \tag{7}$$

Setting $Z_1 = \frac{1}{R_F \bullet (C_S + C_F)}$, and recognizing that the gain bandwidth product (GBP) is equal to $GBP = \frac{A_{OL} \bullet \omega_A}{2\pi}$ and using the following algebraic simplifications:

- $C_S >> C_F$ to simplify Z_1
- $(A_{OL} + 1) \bullet \omega_A \cong A_{OL} \bullet \omega_A = 2\pi \bullet GBP$
- $\left(1 + A_{OL} \bullet \frac{C_F}{C_S + C_F}\right) \cong A_{OL} \bullet \frac{C_F}{C_S + C_F}$

Leads to the following:

$$F_0 = \sqrt{Z_1 \bullet GBP} \tag{8}$$

$$Q = \frac{F_0}{Z_1 + F_C} \tag{9}$$

Further simplification on Q leads to these easier-to-use equations:

$$F_0 = \sqrt{Z_1 \bullet GBP}$$

$$Q = \frac{P_1}{F_0} \tag{10}$$

with:

$$P_1 = \frac{1}{2\pi \bullet R_F C_F} \tag{11}$$

3 Bandwidth Considerations

Maximum bandwidth will be achieved for a Butterworth response with Q = 0.707. This result is an interesting point because this is also equivalent to saying that the –3dB bandwidth is equal to F_0, and allows us to derive a design equation that proves very useful for amplifier selection.

$$GBP = 2\pi \bullet F^2_{-3dB} \bullet R_F C_S \quad (12)$$

Note that the –3dB bandwidth and the transimpedance gain are desired parameters and the source capacitance is known. Thus, Equation 12 allows you to do the following:

- Knowing the bandwidth required by the application, the photodiode capacitance, and the transimpedance gain specification, calculate the minimum GBP requirement for the amplifier
- Knowing the amplifier, the transimpedance gain, and the photodiode capacitance, calculate the maximum achievable bandwidth

We can use this last point to calculate the maximum achievable bandwidth for a few selected amplifiers. The OPA847 is a 3.9GHz GBP amplifier with 0.85nV/√Hz input voltage noise. The OPA846 has a 1.75GHz GBP with a 1.2nV/√Hz input voltage noise. The OPA843 is a 800MHz GBP device with a 2nV/√Hz input voltage noise. All three amplifiers—OPA847, OPA846 and OPA843—are bipolar amplifiers. Finally, the OPA657 is a 1.65GHz GBP device with a 4.8nV/√Hz input voltage noise. Unlike the other three devices, the OPA657 is a FET input amplifier.

Figure 3 shows an example of achievable bandwidth versus transimpedance gain for a 10pF source capacitance for various amplifiers.

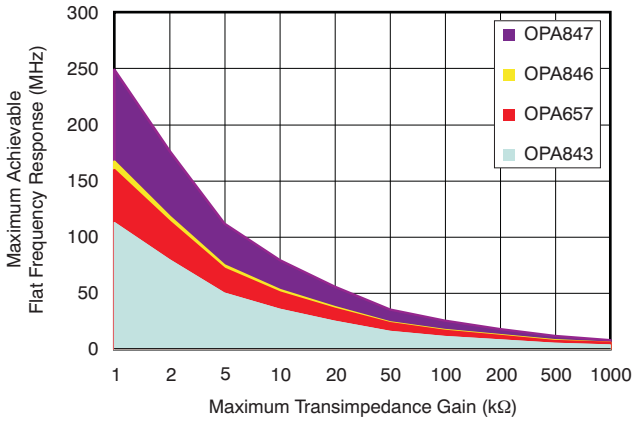


Figure 3. Maximum Achievable Bandwidth for Selected Op Amps (10pF Source Capacitance)

The relative performance for each amplifier is maintained as the source capacitance varies. Note that the source capacitance in this example considers the amplifier parasitic, both common-mode and differential capacitance. When multiple amplifiers can be selected to meet the desired performance—for example, for R_F = 20kΩ, f_{-3dB} = 10MHz—other considerations such as noise or power dissipation must be considered before making the amplifier selection.

At first glance, using a FET input amplifier does not present any advantages and has one major inconvenience: its high input voltage noise. The noise analysis will be developed next and then the relative performance of bipolar technology will be compared with FET technology.

4 Noise Considerations

The equivalent input current noise for a transimpedance amplifier makes the following assumptions:

- This evaluation is an integrated noise analysis that uses spot noise over frequency, and is not intended to be used as a spot noise equation for narrowband applications.
- The application is dc-coupled, pulse-oriented where the integrated noise is of interest.
- The final signal bandwidth for both the transimpedance design and any post-filtering is greater than 10 times the 1/f noise corner frequency of any of the amplifier noise terms. This consideration allows those effects to be neglected.
- The transimpedance bandwidth is set greater than the post-filtering.
- The current noise term on the noninverting is either negligible or made negligible by providing adequate bypassing.

With these assumptions at hand, the noise terms of interest are shown in Figure 4.

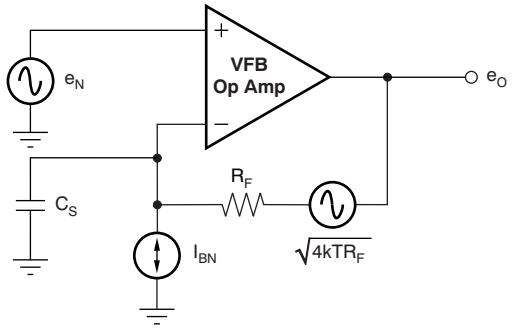


Figure 4. Noise Analysis Circuit

The equivalent input-referred noise current for wideband transimpedance design is provided in Equation 13.

$$i_{EQ} = \sqrt{i_B^2 + \frac{4kT}{R_F} + \left(\frac{e_N}{R_F}\right)^2 + \frac{(e_N 2\pi F C_S)^2}{3}} \quad (13)$$

where:

- I_B = inverting input spot current noise
- 4kT = 16×10^{-21}J at 290 degrees Kelvin
- R_F = feedback resistor
- e_N = noninverting input spot voltage noise
- C_S = inverting input total capacitance
- F = noise integration frequency limit

All these parameters except the noise integration frequency limit can be found in the respective operational amplifier product data sheet. The noise integration frequency limit (F) represents the equivalent *brick-wall* filter of a post-amplifier passive filter.

Using Equation 13 and comparing two amplifiers with very similar GBP—the OPA846 and the OPA657—we can then determine an appropriate transimpedance gain threshold. Below this threshold, it is preferable to use bipolar technology to achieve lower noise, while above the threshold it is better to use FET technology. For this comparison, we will consider that the noise integration frequency limit is the same for both amplifiers. This problem is expressed in Equation 14.

$$\sqrt{i_{B\,(BIP)}^{2} + \frac{4kT}{R_F} + \left(\frac{e_{N(BIP)}}{R_F}\right)^2 + \frac{(e_{N(BIP)} \bullet 2\pi \bullet F \bullet C_{S(BIP)})^2}{3}} = \sqrt{i_{B\,(FET)}^{2} + \frac{4kT}{R_F} + \left(\frac{e_{N(FET)}}{R_F}\right)^2 + \frac{(e_{N(FET)} \bullet 2\pi \bullet F \bullet C_{S(FET)})^2}{3}} \quad (14)$$

The solution for R_F is shown in Equation 15.

$$R_F = \sqrt{\frac{e_{N\,(FET)}^{2} - e_{N\,(BIP)}^{2}}{i_{B\,(BIP)}^{2} - i_{B\,(FET)}^{2} + \frac{2\pi \bullet F}{3} \bullet (C_{S(BIP)} \bullet e_{N\,(BIP)}^{2} - C_{S(FET)} \bullet e_{N\,(FET)}^{2})}} \quad (15)$$

For example, with a band-limit filter bandwidth set at 10MHz and a 10pF diode capacitance, all other parameters are set according to Table 1 (taken from the OPA657 and OPA846 product data sheets).

Table 1. Device Performance Comparison

Device	Element Specifications
OPA657	$e_{N(FET)}$ = 4.8nV/√Hz
	$I_{B(FET)}$ = 1.3fA/√Hz
	$C_{S(FET)}$ = 10pF + 5.2pF = 15.2pF
OPA846	$e_{N(BIP)}$ = 1.2nV/√Hz
	$I_{B(BIP)}$ = 2.8pA/√Hz
	$C_{S(BIP)}$ = 10pF + 3.8pF = 13.8pF

The result is that for a resistor lower than 2kΩ, the bipolar amplifier offers a noise advantage; we can therefore conclude that even though the voltage noise of the OPA657 is high, the total input-referred noise generated by the OPA657 FET amplifier will be lower than that of the OPA846 bipolar amplifier for any transimpedance gain greater than 2kΩ. If a larger post-amplifier filter bandwidth is necessary, the bipolar amplifier (such as the OPA846) will have the lowest noise contribution independent of the resistor.

In general (and from a noise perspective), FET input amplifiers such as the OPA657 are best for large or very large transimpedance gain with low-to-medium bandwidth because of the post-amplifier filter limitations, whereas bipolar amplifiers such as the OPA846 are best for medium-to-large transimpedance gain applications with high bandwidth as limited by the post-amplifier filter.

5 Example

From Figure 3, the maximum achievable bandwidth versus transimpedance gain, it is difficult to separate the OPA846 from the OPA657 simply by achievable bandwidth. In order to help assess the behavioral differences between these two amplifiers, first consider the following application circuit (Figure 5).

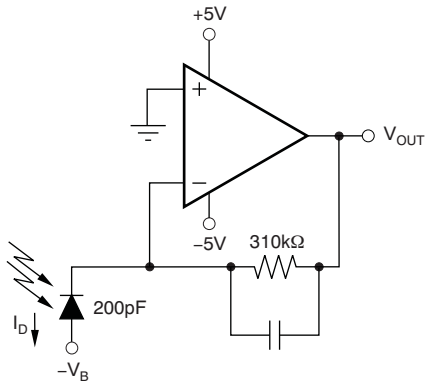
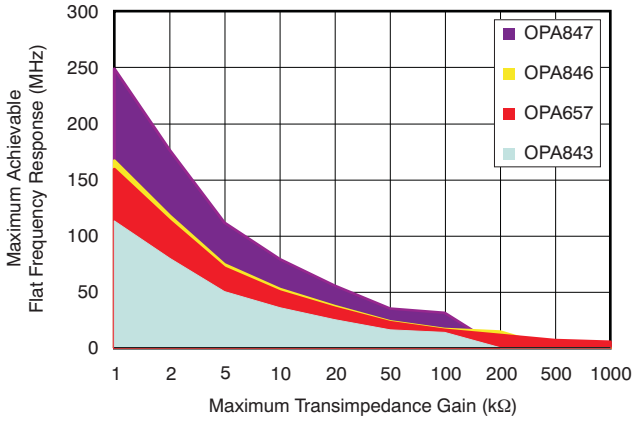


Figure 5. 310kΩ Transimpedance Gain with 200pF Source Capacitance Circuit

In this circuit, using Equation 12, the OPA846 achieves 2.1MHz while the OPA657 achieves 2MHz, making them equivalent on that specification. Looking at the noise, the OPA657 yields a 5pA/$\sqrt{Hz}$ equivalent input noise current if we assume the noise power bandwidth limit is set at 1.4MHz. This noise is dominated by the third term of the total noise equation, which is the effect of the rising portion of the noise gain curve times the relatively high 4.8nV/$\sqrt{Hz}$ input voltage noise for the OPA657. The OPA846, which has a much lower voltage noise but much higher current noise, actually yielded a lower equivalent input noise current of 3pA/$\sqrt{Hz}$. So why is the OPA846 not used in this application?

6 DC-Parameters Consideration

The input bias current of the OPA846, 19μA, generates an output offset voltage with the feedback resistor of 310kΩ of 5.89V. Because the OPA846 is operating on a ±5V power supply, this offset voltage sends the output into saturation. Adding a 310kΩ resistor on the noninverting input allows bias current cancellation but now puts 5.89V common-mode voltage on the input, exceeding the common-mode input range of the OPA846. Figure 6 shows the maximum achievable bandwidth as a function of the transimpedance gain for a few operational amplifiers when taking into consideration dc parameters. The difference between bipolar technology and FET-input technology is now easy to establish. FET-input operational amplifiers, such as the OPA657, are capable of higher transimpedance, where decompensated bipolar operational amplifiers are capable of much higher bandwidth but are limited in gain range.



This measurement takes into consideration a dc parameter for a 10pF source capacitance.

Figure 6. Maximum Achievable Bandwidth vs Transimpedance Gain for Selected Op Amps

7 Conclusion

Although all operational amplifiers can be used in transimpedance applications, the limit in performance is always limited by the transimpedance gain, the bandwidth, and the noise. Many potential problems have been discussed along with suggestions and solutions. This application report developed an emphasis on the methodology to approach transimpedance designs as well as component selection.

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Silicon photodiodes are semiconductor devices responsive to high-energy particles and photons. Photodiodes operate by absorption of photons or charged particles and generate a flow of current in an external circuit, proportional to the incident power. Photodiodes can be used to detect the presence or absence of minute quantities of light and can be calibrated for extremely accurate measurements from intensities below 1 pW/cm^2 to intensities above 100 mW/cm^2. Silicon photodiodes are utilized in such diverse applications as spectroscopy, photography, analytical instrumentation, optical position sensors, beam alignment, surface characterization, laser range finders, optical communications, and medical imaging instruments.

PLANAR DIFFUSED SILICON PHOTODIODE CONSTRUCTION

Planar diffused silicon photodiodes are simply P-N junction diodes. A P-N junction can be formed by diffusing either a P-type impurity (anode), such as Boron, into a N-type bulk silicon wafer, or a N-type impurity, such as Phosphorous, into a P-type bulk silicon wafer. The diffused area defines the photodiode active area. To form an ohmic contact another impurity diffusion into the backside of the wafer is necessary. The impurity is an N-type for P-type active area and P-type for an N-type active area. The contact pads are deposited on the front active area on defined areas, and on the backside, completely covering the device. The active area is then passivated with an antireflection coating to reduce the reflection of the light for a specific predefined wavelength. The non-active area on the top is covered with a thick layer of silicon oxide. By controlling the thickness of bulk substrate, the speed and responsivity of the photodiode can be controlled. Note that the photodiodes, when biased, must be operated in the reverse bias mode, i.e. a negative voltage applied to anode and positive voltage to cathode.

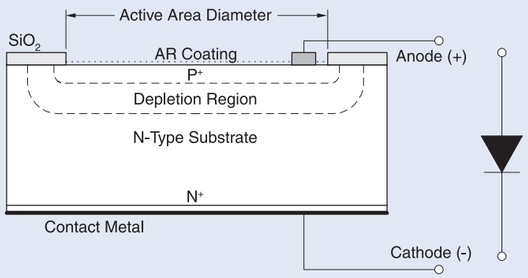


Figure 1. Planar diffused silicon photodiode

PRINCIPLE OF OPERATION

Silicon is a semiconductor with a band gap energy of 1.12 eV at room temperature. This is the gap between the valence band and the conduction band. At absolute zero temperature the valence band is completely filled and the conduction band is vacant. As the temperature increases, the electrons become excited and escalate from the valence band to the conduction band by thermal energy. The electrons can also be escalated to the conduction band by particles or photons with energies greater than 1.12eV, which corresponds to wavelengths shorter than 1100 nm. The resulting electrons in the conduction band are free to conduct current.

Due to concentration gradient, the diffusion of electrons from the N-type region to the P-type region and the diffusion of holes from the P-type region to the N-type region, develops a built-in voltage across the junction. The inter-diffusion of electrons and holes between the N and P regions across the junction results in a region with no free carriers. This is the depletion region. The built-in voltage across the depletion region results in an electric field with maximum at the junction and no field outside of the depletion region. Any applied reverse bias adds to the built in voltage and results in a wider depletion region. The electron-hole pairs generated by light are swept away by drift in the depletion region and are collected by diffusion from the undepleted region. The current generated is proportional to the incident light or radiation power. The light is absorbed exponentially with distance and is proportional to the absorption coefficient. The absorption coefficient is very high for shorter wavelengths in the UV region and is small for longer wavelengths (Figure 2). Hence, short wavelength photons such as UV, are absorbed in a thin top surface layer while silicon becomes transparent to light wavelengths longer than 1200 nm. Moreover, photons with energies smaller than the band gap are not absorbed at all.

(continued)

Penetration Depth

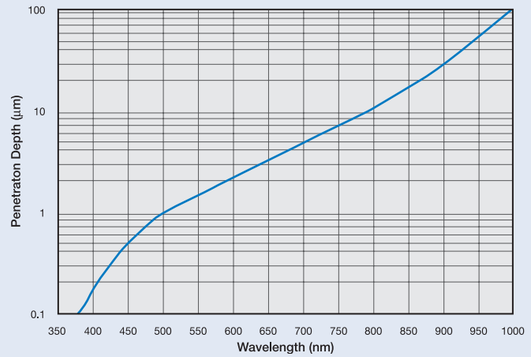


Figure 2. Penetration depth (1/e) of light into silicon substrate for various wavelengths.

ELECTRICAL CHARACTERISTICS

A silicon photodiode can be represented by a current source in parallel with an ideal diode (Figure. 3). The current source represents the current generated by the incident radiation, and the diode represents the p-n junction. In addition, a *junction capacitance* (C_j) and a *shunt resistance* (R_{SH}) are in parallel with the other components. *Series resistance* (R_S) is connected in series with all components in this model.

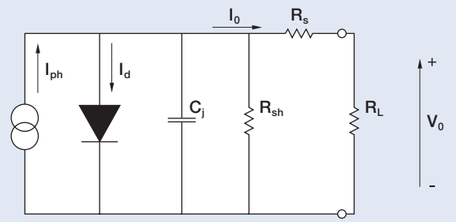


Figure 3. Equivalent Circuit for the silicon photodiode

Shunt Resistance, R_{SH}

Shunt resistance is the slope of the current-voltage curve of the photodiode at the origin, i.e. V=0. Although an ideal photodiode should have an infinite shunt resistance, actual values range from 10's to 1000's of Mega ohms. Experimentally it is obtained by applying ±10 mV, measuring the current and calculating the resistance. Shunt resistance is used to determine the noise current in the photodiode with no bias (photovoltaic mode). For best photodiode performance the highest shunt resistance is desired.

Series Resistance, R_S

Series resistance of a photodiode arises from the resistance of the contacts and the resistance of the undepleted silicon (Figure 1). It is given by:

$$R_S = \frac{(W_S - W_d)\rho}{A} + R_C \qquad (1)$$

Where W_s is the thickness of the substrate, W_d is the width of the depleted region, *A* is the diffused area of the junction, ρ is the resistivity of the substrate and R_c is the contact resistance. Series resistance is used to determine the linearity of the photodiode in photovoltaic mode (no bias, V=0). Although an ideal photodiode should have no series resistance, typical values ranging from 10 to 1000 Ω's are measured.

Junction Capacitance, C_J

The boundaries of the depletion region act as the plates of a parallel plate capacitor (Figure 1). The junction capacitance is directly proportional to the diffused area and inversely proportional to the width of the depletion region. In addition, higher resistivity substrates have lower junction capacitance. Furthermore, the capacitance is dependent on the reverse bias as follows:

$$C_J = \frac{\epsilon_{Si}\epsilon_0 A}{\sqrt{2\epsilon_{Si}\epsilon_0\mu\rho(V_A + V_{bi})}} \qquad (2)$$

$$= A\sqrt{\frac{\epsilon_{Si}\epsilon_0}{2\mu\rho(V_A + V_{bi})}}$$

$$= \frac{\epsilon_{Si}\epsilon_0 A}{W_d}$$

$$\text{Depletion Depth } W_d = \sqrt{2\epsilon_{Si}\epsilon_0\mu\rho(V_A + V_{bi})}$$

Typical Capacitance vs. Reverse Bias

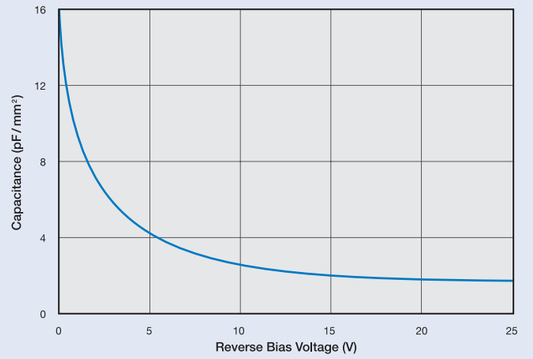


Figure 4. Capacitance of Photoconductive Devices versus Reverse Bias Voltage

where ϵ_0= 8.854x10^{-14} F/cm, is the permittivity of free space, ϵ_{Si}=11.9 is the silicon dielectric constant, μ = 1400 cm^2/Vs is the mobility of the electrons at 300 K, ρ is the resistivity of the silicon, V_{bi} is the built-in voltage of silicon and V_A is the applied bias. Figure 4 shows the dependence of the capacitance on the applied reverse bias voltage. Junction capacitance is used to determine the speed of the response of the photodiode.

Rise / Fall Time and Frequency Response, t_r / t_f / f_{3dB}

The rise time and fall time of a photodiode is defined as the time for the signal to rise or fall from 10% to 90% or 90% to 10% of the final value respectively. This parameter can be also expressed as frequency response, which is the frequency at which the photodiode output decreases by 3dB. It is roughly approximated by:

$$t_r \cong \frac{0.35}{f_{3db}} \qquad (3)$$

There are three factors defining the response time of a photodiode:

1. t_{DRIFT}, the charge collection time of the carriers in the depleted region of the photodiode.

2. $t_{DIFFUSED}$, the charge collection time of the carriers in the undepleted region of the photodiode.

3. t_{RC}, the RC time constant of the diode-circuit combination.

t_{RC} is determined by t_{RC}=2.2 RC, where R, is the sum of the diode series resistance and the load resistance (R_S + R_L), and C, is the sum of the photodiode junction and the stray capacitances (C_j+C_S). Since the junction capacitance (C_j) is dependent on the diffused area of the photodiode and the applied reverse bias (Equation 2), faster rise times are obtained with smaller diffused area photodiodes, and larger applied reverse biases. In addition, stray capacitance can be minimized by using short leads, and careful lay-out of the electronic components. The total rise time is determined by:

$$t_R = \sqrt{t_{DRIFT}^{\,2} + t_{DIFFUSED}^{\,2} + t_{RC}^{\,2}} \qquad (4)$$

Generally, in photovoltaic mode of operation (no bias), rise time is dominated by the diffusion time for diffused areas less than 5 mm^2 and by RC time constant for larger diffused areas for all wavelengths. When operated in photoconductive mode (applied reverse bias), if the photodiode is fully depleted, such as high speed series, the dominant factor is the drift time. In non-fully depleted photodiodes, however, all three factors contribute to the response time.

OPTICAL CHARACTERISTICS

Responsivity, R_λ

The responsivity of a silicon photodiode is a measure of the sensitivity to light, and it is defined as the ratio of the photocurrent I_P to the incident light power P at a given wavelength:

$$R_\lambda = \frac{I_P}{P} \qquad (5)$$

In other words, it is a measure of the effectiveness of the conversion of the light power into electrical current. It varies with the wavelength of the incident light (Figure 5) as well as applied reverse bias and temperature.

Typical Spectral Responsivity

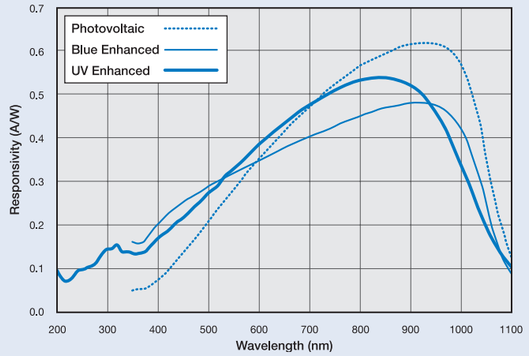


Figure 5. Typical Spectral Responsivity of Several Different Types of Planar Diffused Photodiodes

Responsivity increases slightly with applied reverse bias due to improved charge collection efficiency in the photodiode. Also there are responsivity variations due to change in temperature as shown in figure 6. This is due to decrease or increase of the band gap, because of increase or decrease in the temperature respectively. Spectral responsivity may vary from lot to lot and it is dependent on wavelength. However, the relative variations in responsivity can be reduced to less than 1% on a selected basis.

Temperature Dependence of Responsivity

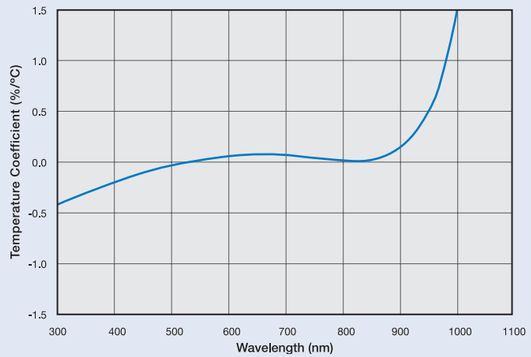


Figure 6. Typical Temperature Coefficient of Responsivity For Silicon Photodiode

Quantum Efficiency, Q.E.

Quantum efficiency is defined as the fraction of the incident photons that contribute to photocurrent. It is related to responsivity by:

$$Q.E. = \frac{R_{\lambda\ Observed}}{R_{\lambda\ Ideal}} = R_\lambda \frac{hc}{\lambda q} = 1240\ \frac{R_\lambda}{\lambda} \qquad (6)$$

where h=6.63 x 10^{-34} J-s, is the Planck constant, c=3 x 10^8 m/s, is the speed of light, q=1.6 x 10^{-19} C, is the electron charge, R_λ is the responsivity in A/W and λ is the wavelength in nm.

Non-Uniformity

Non-Uniformity of response is defined as variations of responsivity observed over the surface of the photodiode active area with a small spot of light. Non-uniformity is inversely proportional to spot size, i.e. larger non-uniformity for smaller spot size.

Non-Linearity

A silicon photodiode is considered linear if the generated photocurrent increases linearly with the incident light power. Photocurrent linearity is determined by measuring the small change in photocurrent as a result of a small change in the incident light power as a function of total photocurrent or incident light power. Non-Linearity is the variation of the ratio of the change in photocurrent to the same change in light power, i.e. $\Delta I/\Delta P$. In another words, linearity exhibits the consistency of responsivity over a range of light power. Non-linearity of less than ±1% are specified over 6-9 decades for planar diffused photodiodes. The lower limit of the photocurrent linearity is determined by the noise current and the upper limit by the series resistance and the load resistance. As the photocurrent increases, first the non-linearity sets in, gradually increasing with increasing photocurrent, and finally at saturation level, the photocurrent remains constant with increasing incident light power. In general, the change in photocurrent generated for the same change in incident light power, is smaller at higher current levels, when the photodetector exhibits non-linearity. The linearity range can slightly be extended by applying a reverse bias to the photodiode.

(continued)

I-V CHARACTERISTICS

The current-voltage characteristic of a photodiode with no incident light is similar to a rectifying diode. When the photodiode is forward biased, there is an exponential increase in the current. When a reverse bias is applied, a small reverse saturation current appears. It is related to dark current as:

$$I_D = I_{SAT}(e^{\frac{qV_A}{k_BT}} - 1) \qquad (7)$$

where I_D is the photodiode dark current, I_{SAT} is the reverse saturation current, q is the electron charge, V_A is the applied bias voltage, k_B=1.38 x 10^{-23} J / K, is the Boltzmann Constant and T is the absolute temperature (273 K= 0 °C).

Photodetector I-V Curves

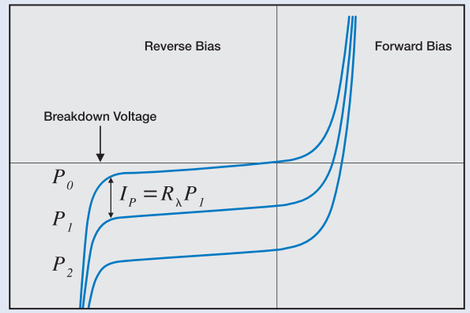


Figure 7. Characteristic I-V Curves of an OSI Optoelectronics photodiode for Photoconductive and Photovoltaic modes of operation. P_0-P_2 represent different light levels.

This relationship is shown in figure 7. From equation 7, three various states can be defined:

a) V = 0, In this state, the dark current I_P=0.
b) V = +V, In this state the current increases exponentially. This state is also known as forward bias mode.
c) V = -V, When a very large reverse bias is applied to the photodiode, the dark current becomes the reverse saturation current, I_{Sat}.

Illuminating the photodiode with optical radiation, shifts the I-V curve by the amount of photocurrent (I_P). Thus:

$$I_{TOTAL} = I_{SAT}(e^{\frac{qV_A}{k_BT}} - 1) - I_P \qquad (8)$$

where I_P is defined as the photocurrent in equation 5.

As the applied reverse bias increases, there is a sharp increase in the photodiode current. The applied reverse bias at this point is referred to as breakdown voltage. This is the maximum applied reverse bias, below which, the photodiode should be operated (also known as maximum reverse voltage). Breakdown voltage, varies from one photodiode to another and is usually measured, for small active areas, at a dark current of 10 µA.

NOISE

In a photodiode, two sources of noise can be identified; Shot noise and Johnson noise:

Shot Noise

Shot noise is related to the statistical fluctuation in both the photocurrent and the dark current. The magnitude of the shot noise is expressed as the root mean square (rms) noise current:

$$I_{sn} = \sqrt{2q(I_P + I_D)\Delta f} \qquad (9)$$

Where q=1.6x10^{-19}C, is the electron charge, I_P is the photogenerated current, I_D is the photodetector dark current and Δf is the noise measurement bandwidth. Shot noise is the dominating source when operating in photoconductive (biased) mode.

Thermal or Johnson Noise

The shunt resistance in a photodetector has a Johnson noise associated with it. This is due to the thermal generation of carriers. The magnitude of this generated noise current is:

$$I_{jn} = \sqrt{\frac{4k_B T\Delta f}{R_{SH}}} \qquad (10)$$

Where k_B=1.38 x 10^{-23} J/K, is the Boltzmann Constant, T, is the absolute temperature in degrees Kelvin (273 K= 0 °C), Δf is the noise measurement bandwidth and R_{SH} , is the shunt resistance of the photodiode. This type of noise is the dominant current noise in photovoltaic (unbiased) operation mode.

Note: All resistors have a Johnson noise associated with them, including the load resistor. This additional noise current is large and adds to the Johnson noise current caused by the photodetector shunt resistance.

Total Noise

The total noise current generated in a photodetector is determined by:

$$I_{tn} = \sqrt{I_{sn}^2 + I_{jn}^2} \qquad (11)$$

Noise Equivalent Power (NEP)

Noise Equivalent Power is the amount of incident light power on a photodetector, which generates a photocurrent equal to the noise current. NEP is defined as:

$$NEP = \frac{I_{tn}}{R_\lambda} \qquad (12)$$

Where R_λ is the responsivity in A/W and I_{tn} is the total noise of the photodetector. NEP values can vary from 10^{-11} W/√Hz for large active area photodiodes down to 10^{-15} W /√Hz for small active area photodiodes.

(continued)

■ TEMPERATURE EFFECTS

All photodiode characteristics are affected by changes in temperature. They include shunt resistance, dark current, breakdown voltage, responsivity and to a lesser extent other parameters such as junction capacitance.

Shunt Resistance and Dark Current:

There are two major currents in a photodiode contributing to dark current and shunt resistance. Diffusion current is the dominating factor in a photovoltaic (unbiased) mode of operation, which determines the shunt resistance. It varies as the square of the temperature. In photoconductive mode (reverse biased), however, the drift current becomes the dominant current (dark current) and varies directly with temperature. Thus, change in temperature affects the photodetector more in photovoltaic mode than in photoconductive mode of operation.

In photoconductive mode the dark current may approximately double for every 10 °C increase change in temperature. And in photovoltaic mode, shunt resistance may approximately double for every 6 °C decrease in temperature. The exact change is dependent on additional parameters such as the applied reverse bias, resistivity of the substrate as well as the thickness of the substrate.

Breakdown Voltage:

For small active area devices, by definition breakdown voltage is defined as the voltage at which the dark current becomes 10µA. Since dark current increases with temperature, therefore, breakdown voltage decreases similarly with increase in temperature.

Responsivity:

Effects of temperature on responsivity is discussed in the “Responsivity” section of these notes.

■ BIASING

A photodiode signal can be measured as a voltage or a current. Current measurement demonstrates far better linearity, offset, and bandwidth performance. The generated photocurrent is proportional to the incident light power and it must be converted to voltage using a transimpedance configuration. The photodiode can be operated with or without an applied reverse bias depending on the application specific requirements. They are referred to as “Photoconductive” (biased) and “Photovoltaic” (unbiased) modes.

Photoconductive Mode (PC)

Application of a reverse bias (i.e. cathode positive, anode negative) can greatly improve the speed of response and linearity of the devices. This is due to increase in the depletion region width and consequently decrease in junction capacitance. Applying a reverse bias, however, will increase the dark and noise currents. An example of low light level / high-speed response operated in photoconductive mode is shown in figure 8.

In this configuration the detector is biased to reduce junction capacitance thus reducing noise and rise time (t_r). A two stage amplification is used in this example since a high gain with a wide bandwidth is required. The two stages include a transimpedance pre-amp for current- to-voltage conversion and a non-inverting amplifier for voltage amplification. Gain and bandwidth ($f_{3dB\ Max}$) are directly determined by R_F, per equations (13) and (14) . The gain of the second stage is approximated by 1+ R1 / R2. A feedback capacitor (C_F) will limit the frequency response and avoids gain peaking.

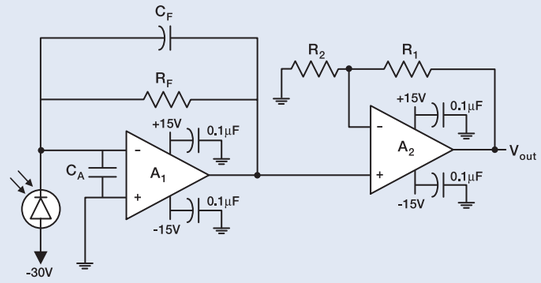


Figure 8. Photoconductive mode of operation circuit example: Low Light Level / Wide Bandwidth

$$f_{3dB\mathrm{Max}}[Hz] = \sqrt{\frac{GBP}{2\pi R_F (C_J + C_F + C_A)}} \qquad (13)$$

Where GBP is the Gain Bandwidth Product of amplifier (A_1) and C_A is the amplifier input capacitance.

$$Gain(V/W) = \frac{V_{OUT}}{P} = R_F\left(1 + \frac{R_1}{R_2}\right)R_\lambda \qquad (14)$$

In low speed applications, a large gain, e.g. >10MΩ can be achieved by introducing a large value (R_F) without the need for the second stage.

Typical components used in this configuration are:

Amplifier :	OPA-637, OPA-686, OPA-687, or similar
R_F :	1 to 10 KΩ Typical, depending on C_j
R_1 :	10 to 50 kΩ
R_2 :	0.5 to 10 kΩ
C_F :	0.2 to 2 pF

In high speed, high light level measurements, however, a different approach is preferred. The most common example is pulse width measurements of short pulse gas lasers, solid state laser diodes, or any other similar short pulse light source. The photodiode output can be either directly connected to an oscilloscope (Figure 9) or fed to a fast response amplifier. When using an oscilloscope, the bandwidth of the scope can be adjusted to the pulse width of the light source for maximum signal to noise ratio. In this application the bias voltage is large. Two opposing protection diodes should be connected to the input of the oscilloscope across the input and ground.

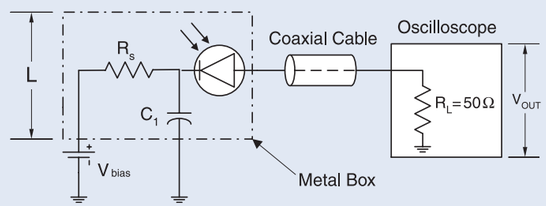


Figure 9. Photoconductive mode of operation circuit example: High Light Level / High Speed Response

(continued)

To avoid ringing in the output signal, the cable between the detector and the oscilloscope should be short (i.e. < 20cm) and terminated with a 50 ohm load resistor (R_L). The photodiode should be enclosed in a metallic box, if possible, with short leads between the detector and the capacitor, and between the detector and the coaxial cable. The metallic box should be tied through a capacitor (C1), with lead length (L) less than 2 cm, where R_L C_j > 10 τ (τ is the pulse width in seconds). R_S is chosen such that $R_S < V_{BIAS} / 10\ I_{PDC}$, where I_{PDC} is the DC photocurrent. Bandwidth is defined as 0.35 / τ. A minimum of 10V reverse bias is necessary for this application. Note that a bias larger than the photodiode maximum reverse voltage should not be applied.

Photovoltaic Mode (PV)

The photovoltaic mode of operation (unbiased) is preferred when a photodiode is used in low frequency applications (up to 350 kHz) as well as ultra low light level applications. In addition to offering a simple operational configuration, the photocurrents in this mode have less variations in responsivity with temperature. An example of an ultra low light level / low speed is shown in figure 10.

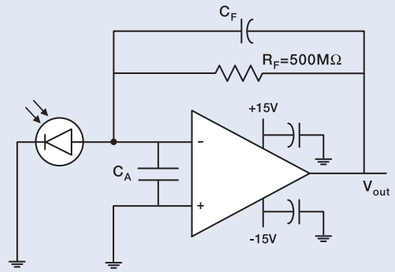


Figure 10. Photovoltaic mode of operation circuit example: Ultra low level light / low speed

In this example, a FET input operational amplifier as well as a large resistance feedback resistor (R_F) is considered. The detector is unbiased to eliminate any additional noise current. The total output is determined by equation (15) and the op-amp noise current is determined by R_F in equation (16):

$$V_{OUT} = I_P \times R_F \qquad (15)$$

$$I_N\left[\frac{A_{rms}}{\sqrt{Hz}}\right] = \sqrt{\frac{4kT}{R_F}} \qquad (16)$$

where k=1.38 x 10^{-23} J/K and T is temperature in K.

For stability, select C_F such that

$$\sqrt{\frac{GBP}{2\pi R_F (C_J + C_F + C_A)}} > \frac{1}{2\pi R_F C_F} \qquad (\ )$$

Operating bandwidth, after gain peaking compensation is:

$$f_{OP}[Hz] = \frac{1}{2\pi R_F C_F} \qquad (18)$$

Some recommended components for this configuration are:

Amplifier :	OPA-117 or similar
R_F :	500 MΩ

These examples or any other configurations for single photodiodes can be applied to any of OSI Optoelectronics’ monolithic, common substrate liner array photodiodes. The output of the first stage pre-amplifiers can be connected to a sample and hold circuit and a multiplexer. Figure 11 shows the block diagram for such configuration.

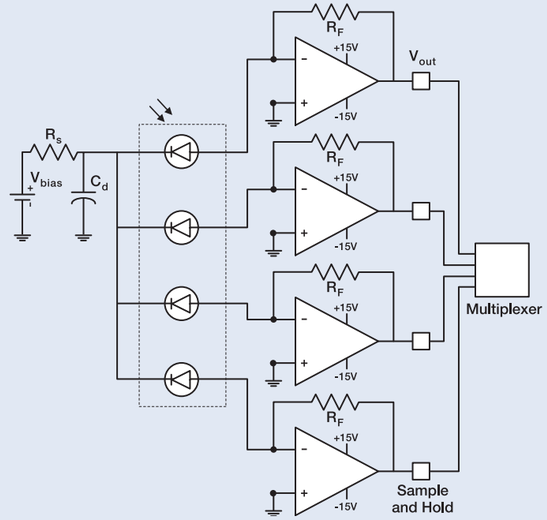


Figure 11. Circuit example for a multi-element, common cathode array

Kynar 460 Insulation on 30 awg Wire-Wrap wire

Wire Diameter - .01" +/- .001"
Insulation Thickness - .004" +/- .001"
Relative Premittivity - 7

Twisted Wire - ~7pf/inch

4GHz Ultra-Low Bias Current FET Input Op Amp

FEATURES

- **Gain Bandwidth Product: 4GHz**
- **Low Input Bias Current:**
  - **±3fA Typ. Room Temperature**
  - **4pA Max at 125°C**
- **Current Noise (100kHz): 7fA/√Hz**
- **Voltage Noise (1MHz): 4.0nV/√Hz**
- **Extremely Low C_{IN} 0.45pF**
- **Rail-to-Rail Output**
- $A_V \geq 10$
- Slew Rate: +1500V/µs, –1000V/µs
- Supply Range: 3.1V to 5.25V
- Quiescent Current: 16.5mA
- Operating Temp Range: –40°C to 125°C
- Single in 8-Lead SO-8, 6-Lead TSOT-23 Packages
- Dual in 8-Lead MS8, 3mm × 3mm 10-Lead DFN 10 Packages

APPLICATIONS

- Transimpedance Amplifiers
- ADC Drivers
- Photomultiplier Tube Post-Amplifier
- Low I_{BIAS} Circuits

DESCRIPTION

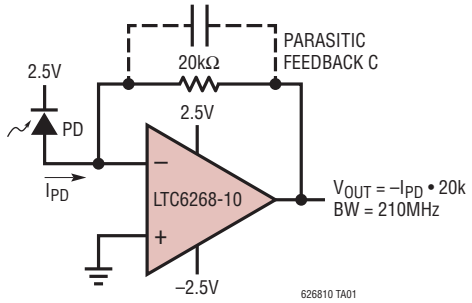
The LTC®6268-10/LTC6269-10 is a single/dual 4GHz FET-input operational amplifier with extremely low input bias current and low input capacitance. It also features low input-referred current noise and voltage noise making it an ideal choice for high speed transimpedance amplifiers, and high-impedance sensor amplifiers. It is a decompensated op amp that is gain-of-10 stable.

It operates on 3.1V to 5.25V supply and consumes 16.5mA per amplifier. A shutdown feature can be used to lower power consumption when the amplifier is not in use.

The LTC6268-10 single op amp is available in 8-lead SOIC and 6-lead SOT-23 packages. The SOIC package includes two unconnected pins which can be used to create an input pin guard ring to protect against board leakage currents. The LTC6269-10 dual op amp is available in 8-lead MSOP with exposed pad and 3mm × 3mm 10-lead DFN packages. They are fully specified over the –40°C to 85°C and the –40°C to 125°C temperature ranges.

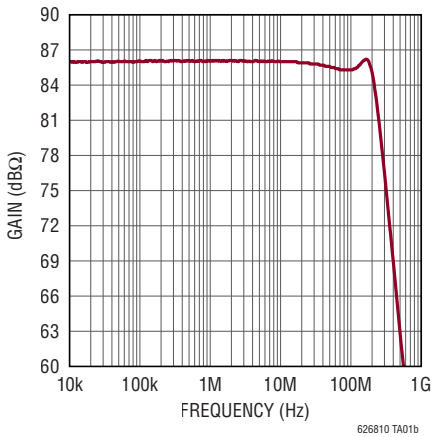
TYPICAL APPLICATION

20kΩ Gain 210MHz Transimpedance Amplifier



PD = OSI OPTOELECTRONICS, FCI-125G-006

20kΩ TIA Frequency Response

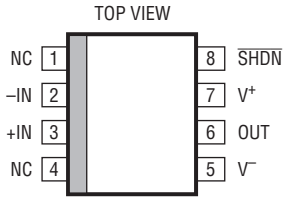


ABSOLUTE MAXIMUM RATINGS

(Note 1)

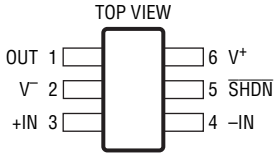
Supply Voltage V^+ to V^- 5.5V
Input Voltage ..... V^- – 0.2V to V^+ + 0.2V
Input Current (+IN, –IN) (Note 2) ..... ±1mA
Input Current ($\overline{SHDN}$) ..... ±1mA
Output Current (I_{OUT}) (Note 8, 9) 135mA
Output Short-Circuit Duration (Note 3) ... Thermally Limited
Operating Temperature Range
LTC6268-10I/LTC6269-10I ..... –40°C to 85°C
LTC6268-10H/LTC6269-10H ..... –40°C to 125°C
Specified Temperature Range (Note 4)
LTC6268-10I/LTC6269-10I ..... –40°C to 85°C
LTC6268-10H/LTC6269-10H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature S8, S6 and
MS8E (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



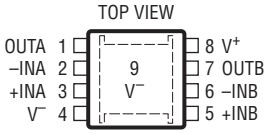
S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 120°C/W (NOTE 5)



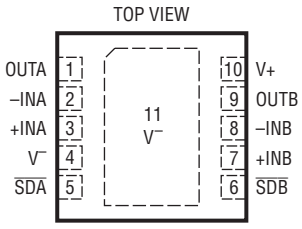
S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 192°C/W (NOTE 5)



MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W (NOTE 5)
EXPOSED PAD (PIN 9) IS V^-, IT IS RECOMMENDED TO SOLDER TO PCB



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W (NOTE 5)
EXPOSED PAD (PIN 11) IS V^-, IT IS RECOMMENDED TO SOLDER TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6268IS6-10#TRMPBF	LTC6268IS6-10#TRPBF	LTGQT	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6268HS6-10#TRMPBF	LTC6268HS6-10#TRPBF	LTGQT	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6268IS8-10#PBF	LTC6268IS8-10#TRPBF	626810	8-Lead Plastic SOIC	–40°C to 85°C
LTC6268HS8-10#PBF	LTC6268HS8-10#TRPBF	626810	8-Lead Plastic SOIC	–40°C to 125°C
LTC6269IMS8E-10#PBF	LTC6269IMS8E-10#TRPBF	LTGRM	8-Lead Plastic MSOP	–40°C to 85°C
LTC6269HMS8E-10#PBF	LTC6269HMS8E-10#TRPBF	LTGRM	8-Lead Plastic MSOP	–40°C to 125°C
LTC6269IDD-10#PBF	LTC6269IDD-10#TRPBF	LGRK	10-Lead Plastic DD	–40°C to 85°C
LTC6269HDD-10#PBF	LTC6269HDD-10#TRPBF	LGRK	10-Lead Plastic DD	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

5.0V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 5.0V (V^+ = 5V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 2.75V	 ●	–0.7 –3	0.2	0.7 3	mV mV
		V_{CM} = 4.0V	 ●	–1.0 –4.5	0.2	1.0 4.5	mV mV
TC V_{OS}	Input Offset Voltage Drift	V_{CM} = 2.75V			4		µV/°C
I_B	Input Bias Current (Notes 6, 8)	V_{CM} = 2.75V LTC6268I-10/LTC6269I-10 LTC6268H-10/LTC6269H-10	 ● ●	–20 –900 –4	±3	20 900 4	fA fA pA
		V_{CM} = 4.0V LTC6268I-10/LTC6269I-10 LTC6268H-10/LTC6269H-10	 ● ●	–20 –900 –4	±3	20 900 4	fA fA pA
I_{OS}	Input Offset Current (Notes 6, 8)	V_{CM} = 2.75V LTC6268I-10/LTC6269I-10 LTC6268H-10/LTC6269H-10	 ● ●	–40 –450 –2	±6	40 450 2	fA fA pA
e_n	Input Voltage Noise Density, V_{CM} = 2.75V	f = 1MHz			4.0		nV/√Hz
	Input Voltage Noise Density, V_{CM} = 4.0V	f = 1MHz			4.0		nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz			12.6		μV_{P-P}
i_n	Input Current Noise Density, V_{CM} = 2.75V	f = 100kHz			7		fA/√Hz
	Input Current Noise Density, V_{CM} = 4.0V	f = 100kHz			7		fA/√Hz
R_{IN}	Input Resistance	Differential			>1000		GΩ
		Common Mode			>1000		GΩ
C_{IN}	Input Capacitance	Differential (DC to 200MHz)			0.1		pF
		Common Mode (DC to 100MHz)			0.45		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.5V to 3.2V (PNP Side)	 ●	72 68	85		dB dB
		V_{CM} = –0.1V to 4.5V	 ●	64 52	82		dB dB
IVR	Input Voltage Range	Guaranteed by CMRR	●	–0.1		4.5	V

5.0V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 5.0V (V^+ = 5V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_{CM} = 1.0V, V_{SUPPLY} Ranges from 3.1V to 5.25V		 ●	78 75	95		dB dB
	Supply Voltage Range			●	3.1		5.25	
A_V	Open Loop Voltage Gain	V_{OUT} = 0.5V to 4.5V	R_{LOAD} = 10k	 ●	125 40	250		V/mV V/mV
			R_{LOAD} = 100	 ●	10 2	21		V/mV V/mV
V_{OL}	Output Swing Low (Input Overdrive 30mV) Measured from V^-	I_{SINK} = 10mA		●		80	140 200	mV mV
		I_{SINK} = 25mA		●		130	200 260	mV mV
V_{OH}	Output Swing High (Input Overdrive 30mV) Measured from V^+	I_{SOURCE} = 10mA		●		70	140 200	mV mV
		I_{SOURCE} = 25mA		●		160	270 370	mV mV
I_{SC}	Output Short Circuit Current (Note 9)			 ●	60 40	90		mA mA
I_S	Supply Current Per Amplifier			 ●	15 9	16.5	18 25	mA mA
	Supply Current in Shutdown (Per Amplifier)			●		0.39	0.85 1.5	mA mA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.75V $V_{\overline{SHDN}}$ =1.50V		● ●	–12 –12	2 2	12 12	µA µA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable		●			0.75	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable. If $\overline{SHDN}$ is Unconnected, Amp is Enabled		●	1.5			V
t_{ON}	Turn On Time, Delay from $\overline{SHDN}$ Toggle to Output Reaching 90% of Target	$\overline{SHDN}$ Toggle from 0V to 2V				360		ns
t_{OFF}	Turn Off Time, Delay from $\overline{SHDN}$ Toggle to Output High Z	$\overline{SHDN}$ Toggle from 2V to 0V				183		ns
GBW	Gain-Bandwidth Product (Note 8)	f = 10MHz		●	3500	4000		MHz
SR+	Slew Rate+	A_V = 11 (R_F = 1000, R_G = 100) V_{OUT} = 0.5V to 4.5V, Measured 20% to 80%, R_{LOAD} = 500Ω		 ●	1100 600	1500		 V/µs V/µs
SR–	Slew Rate–	A_V = 11 (R_F = 1000, R_G = 100) V_{OUT} = 4.5V to 0.5V, Measured 80% to 20%,		 ●	900 500	 1000		V/µs V/µs
FPBW	Full Power Bandwidth (Note 7)	$4V_{P-P}$				73		MHz
HD	Harmonic Distortion(HD2/HD3)	A_V = 10, 10MHz. $2V_{P-P}$, V_{CM} = 2.25V, R_L = 1k, RF = 450Ω, RG = 50Ω				–91/–96		dB
I_{LEAK}	Output Leakage Current in Shutdown	$V_{\overline{SHDN}}$ = 0V, V_{OUT} = 0V $V_{\overline{SHDN}}$ = 0V, V_{OUT} = 5V					400 400	nA nA

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 3.3V (V^+ = 3.3V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 1.0V		–0.7	0.2	0.7	mV
			●	–3		3	mV
		V_{CM} = 2.3V		–1.0	0.2	1.0	mV
			●	–4.5		4.5	mV
TC V_{OS}	Input Offset Voltage Drift	V_{CM} = 1.0V			4		µV/C
I_B	Input Bias Current (Notes 6, 8)	V_{CM} = 1.0V		–20	±3	20	fA
		LTC6268I-10/LTC6269I-10	●	–900		900	fA
		LTC6268H-10/LTC6269H-10	●	–4		4	pA
		V_{CM} = 2.3V		–20	±3	20	fA
		LTC6268I-10/LTC6269I-10	●	–900		900	fA
		LTC6268H-10/LTC6269H-10	●	–4		4	pA
I_{OS}	Input Offset Current (Notes 6, 8)	V_{CM} = 1.0V		–40	±6	40	fA
		LTC6268I-10/LTC6269I-10	●	–450		450	fA
		LTC6268H-10/LTC6269H-10	●	–2		2	pA
e_n	Input Voltage Noise Density, V_{CM} =1.0V	f = 1MHz			4.0		nV/√Hz
	Input Voltage Noise Density, V_{CM} = 2.3V	f = 1MHz			4.0		nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz			13.5		μV_{P-P}
i_n	Input Current Noise Density, V_{CM} = 1.0V	f = 100kHz			7		fA/√Hz
	Input Current Noise Density, V_{CM} = 2.3V	f = 100kHz			7		fA/√Hz
R_{IN}	Input Resistance	Differential			>1000		GΩ
		Common Mode			>1000		GΩ
C_{IN}	Input Capacitance	Differential (DC to 200MHz)			0.1		pF
		Common Mode (DC to 100MHz)			0.45		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.5V to 1.2V (PNP Side)		63	90		dB
			●	60			dB
		V_{CM} = –0.1V to 2.8V (Full Range)		60	77		dB
			●	50			dB
IVR	Input Voltage Range	Guaranteed by CMRR	●	–0.1		2.8	V
A_V	Open Loop Voltage Gain	V_{OUT} = 0.5V to 2.8V, R_{LOAD} = 10k		80	200		V/mV
			●	40			V/mV
		R_{LOAD} = 100		10	18		V/mV
			●	2			V/mV
V_{OL}	Output Swing Low (Input Overdrive 30mV). Measured from V^-	I_{SINK} = 10mA			80	140	mV
			●			200	mV
		I_{SINK} = 25mA			140	200	mV
			●			260	mV
V_{OH}	Output Swing High (Input Overdrive 30mV). Measured from V^+	I_{SOURCE} = 10mA			80	140	mV
			●			200	mV
		I_{SOURCE} = 25mA			170	270	mV
			●			370	mV
I_{SC}	Output Short Circuit Current (Note 9)			50	80		mA
			●	35			mA
I_S	Supply Current per Amplifier			14.5	16	17.5	mA
			●	9		25	mA

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{SUPPLY} = 3.3V (V^+ = 3.3V, V^- = 0V, V_{CM} = mid-supply) R_L = 1kΩ, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Supply Current in Shutdown (Per Amplifier)		 ●		0.23	0.6 1.2	mA mA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.75V $V_{\overline{SHDN}}$ = 1.5V	● ●	–12 –12	2 2	12 12	µA µA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable	●			0.75	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable. If $\overline{SHDN}$ is Unconnected, Amp Is Enabled	●	1.5			V
t_{ON}	Turn On Time, Delay from $\overline{SHDN}$ Toggle to Output Reaching 90% of Target	$\overline{SHDN}$ Toggle from 0V to 2V			750		ns
t_{OFF}	Turn Off Time, Delay from $\overline{SHDN}$ Toggle to Output High Z	$\overline{SHDN}$ Toggle from 2V to 0V			201		ns
GBW	Gain-Bandwidth Product (Note 8)	f = 10MHz	●	3500	4000		MHz
SR+	Slew Rate+	A_V = 11 (R_F = 1000, R_G = 100), V_{OUT} = 1V to 2.3V, Measured 20% to 80%, R_{LOAD} = 500Ω	 ●	 800 600	 1500		 V/µs V/µs
SR–	Slew Rate–	A_V = 11 (R_F = 1000, R_G = 100), V_{OUT} = 1V to 2.3V, Measured 80% to 20%, R_{LOAD} = 500Ω	 ●	 600 400	 1000		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 7)	$2.3V_{P-P}$			105		MHz
HD	Harmonic Distortion(HD2/HD3)	A = 10, 10MHz. $2V_{P-P}$, V_{CM} = 1.65V, R_L = 1k, RF = 450Ω, RG = 50Ω			–67/–78		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by two series connected ESD protection diodes to each power supply. The input current should be limited to less than 1mA. The input voltage should not exceed 200mV beyond the power supply.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC6268-10I/LTC6269-10I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6268-10H/LTC6269-10H is guaranteed to meet specified performance from –40°C to 125°C.

Note 5: Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

Note 6: The input bias current is the average of the currents into the positive and negative input pins. Typical measurement is for S8 package.

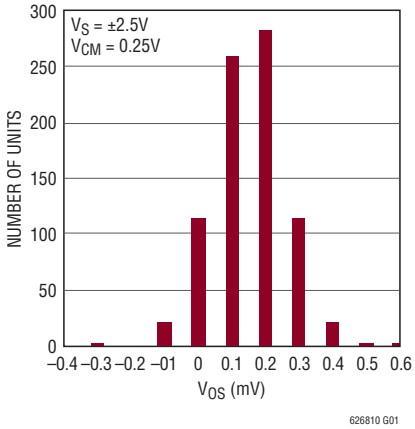
Note 7: Full Power Bandwidth is determined from distortion performance in a gain-of-10 configuration with HD2/HD3 < –40dB (1%) as the criteria for a valid output.

Note 8: This parameter is specified by design and/or characterization and is not tested in production.

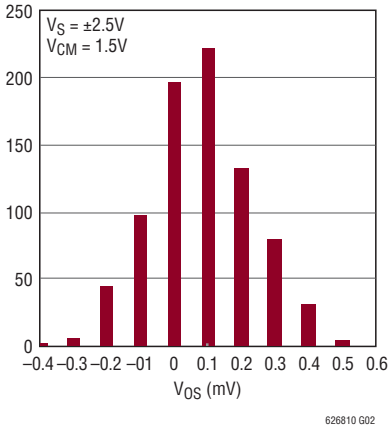
Note 9: The LTC6268-10/LTC6269-10 is capable of producing peak output currents in excess of 135mA. Current density limitations within the IC require the continuous current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 135mA (Absolute Maximum).

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

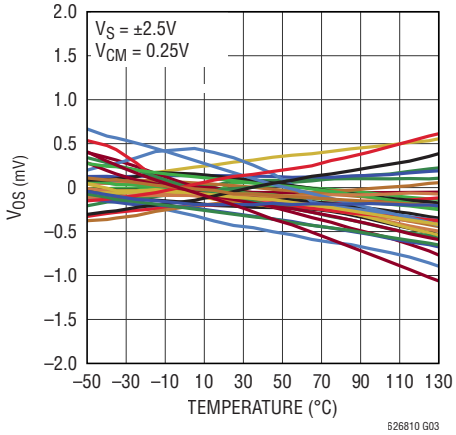
Input Offset Voltage Distribution



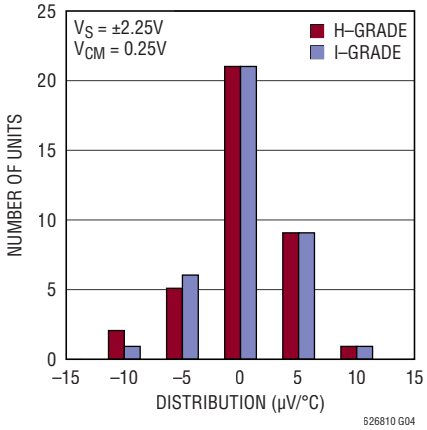
Input Offset Voltage Distribution



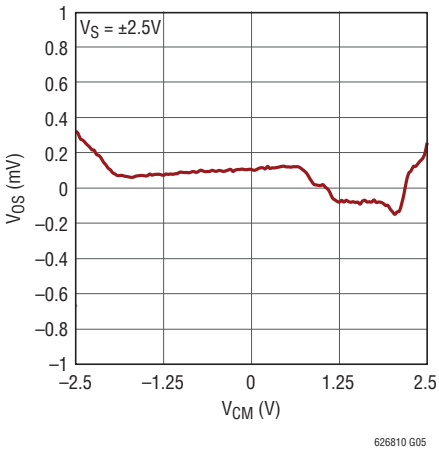
Input Offset Voltage vs Temperature



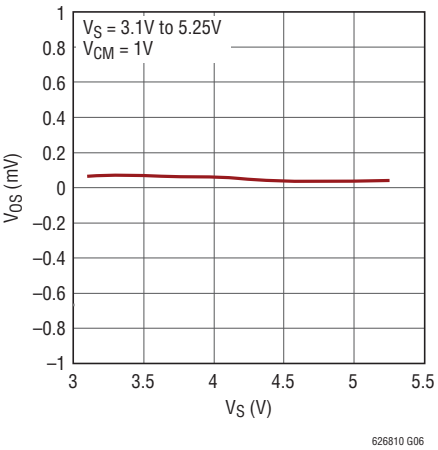
Input Offset Drift Distribution



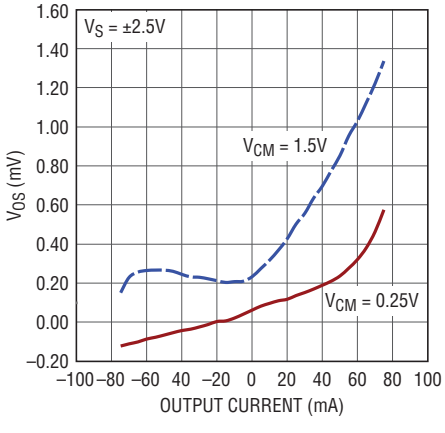
Input Offset Voltage vs Common Mode Voltage



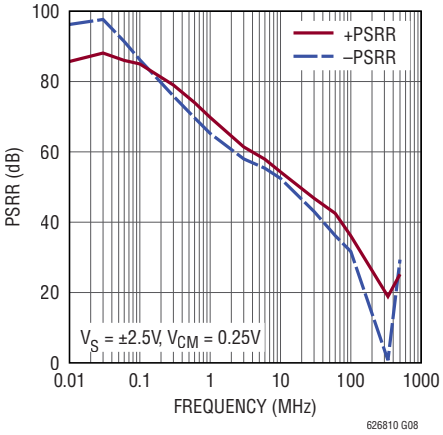
Input Offset Voltage vs Supply Voltage



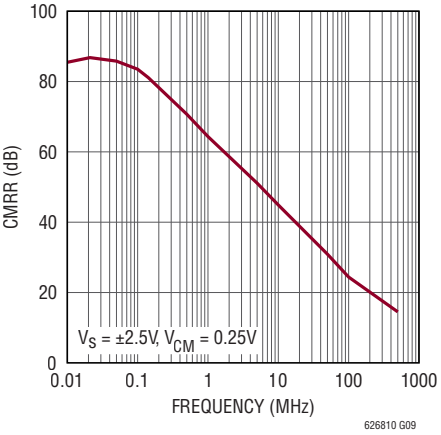
Input Offset Voltage vs Output Current



PSRR vs Frequency

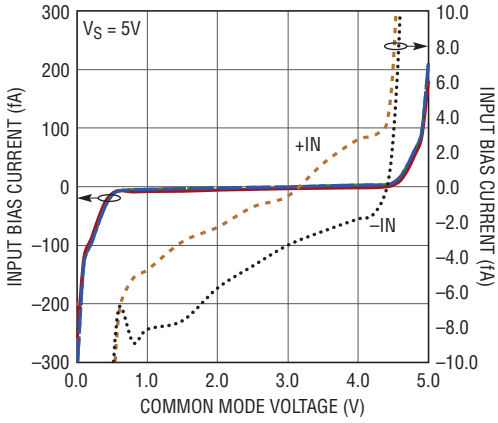


CMRR vs Frequency

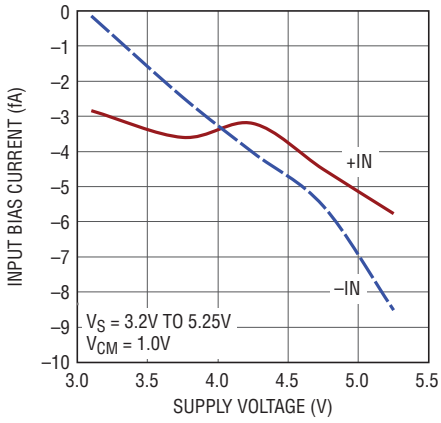


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

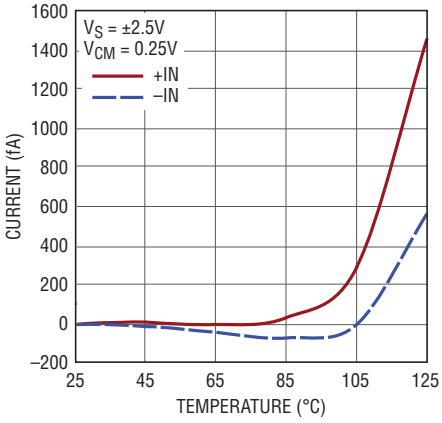
Input Bias Current vs Common Mode Voltage



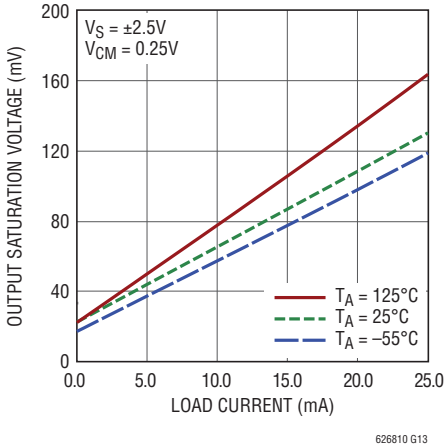
Input Bias Current vs Supply Voltage



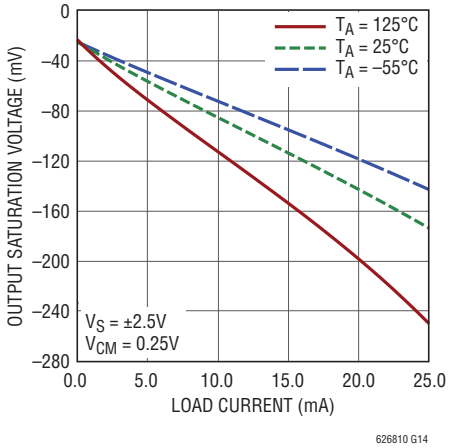
Input Bias Current vs Temperature



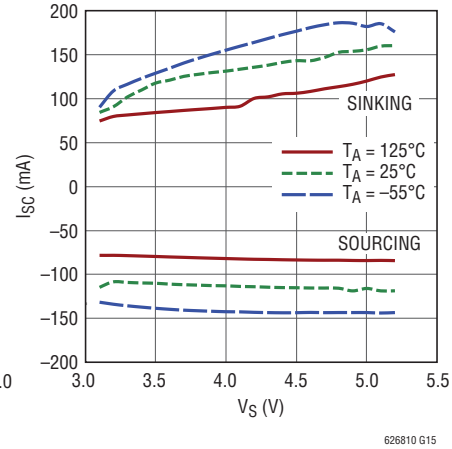
Output Saturation Voltage vs Load Current (Output Low)



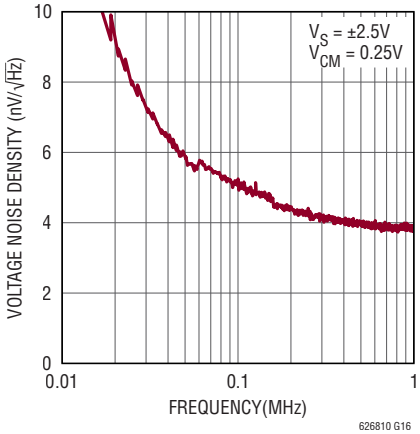
Output Saturation Voltage vs Load Current (Output High)



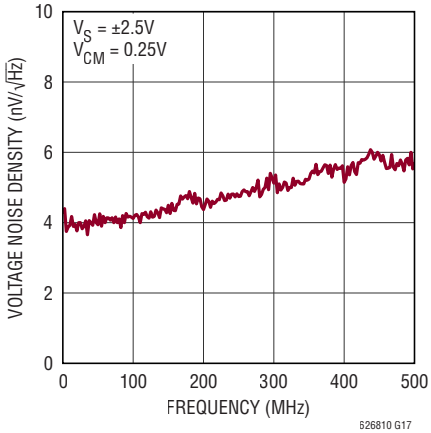
Output Short Circuit Current vs Supply Voltage



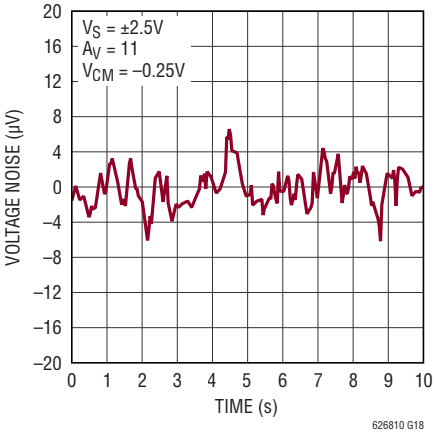
Input Referred Voltage Noise Density



Wide Band Input Referred Voltage Noise

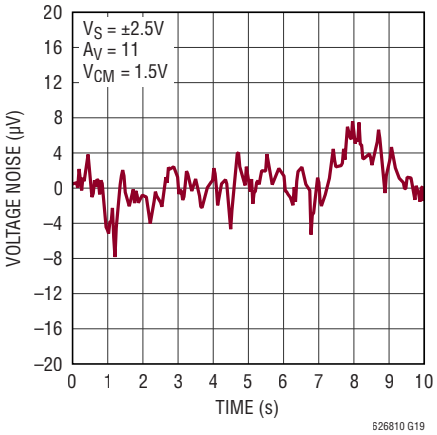


0.1Hz to 10Hz Input Referred Voltage Noise

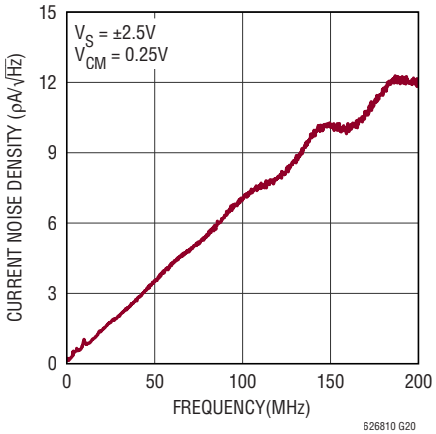


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

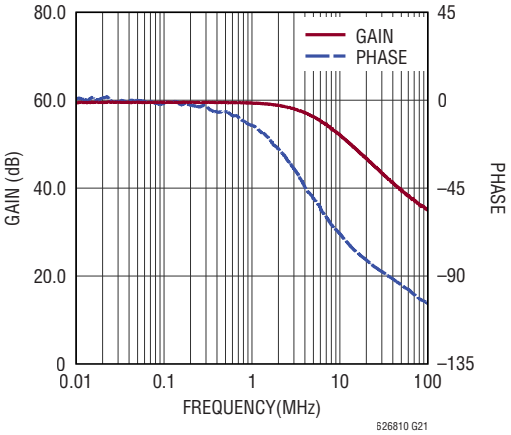
0.1Hz to 10Hz Input Referred Voltage Noise



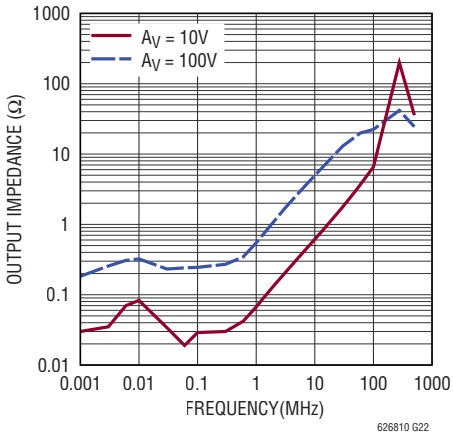
Input Referred Current Noise



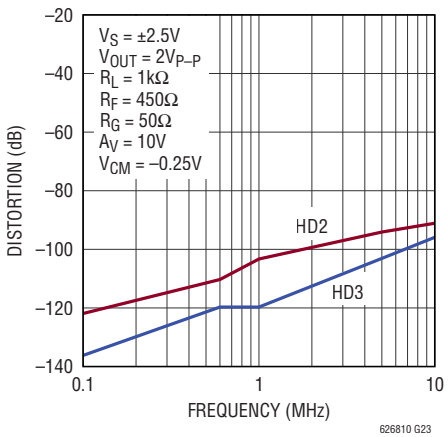
Gain/Phase vs Frequency



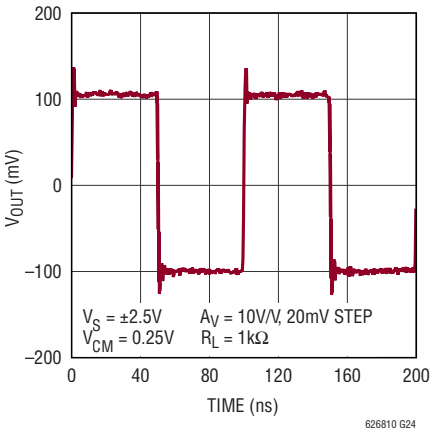
Output Impedance vs Frequency



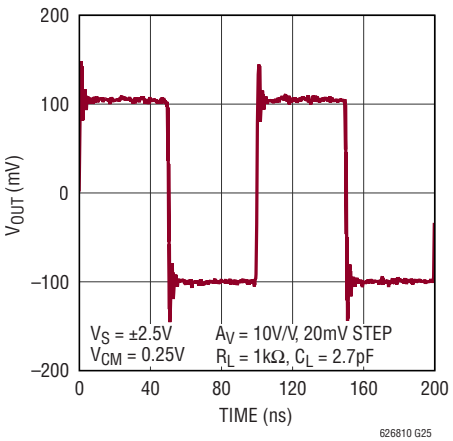
Harmonic Distortion vs Frequency



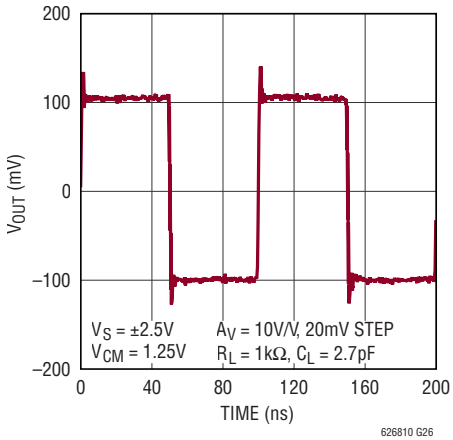
Small Signal Step Response



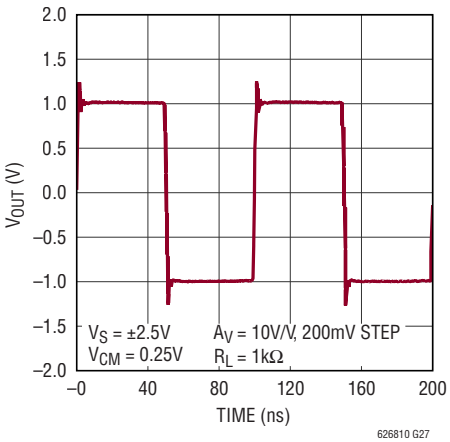
Small Signal Step Response



Small Signal Step Response

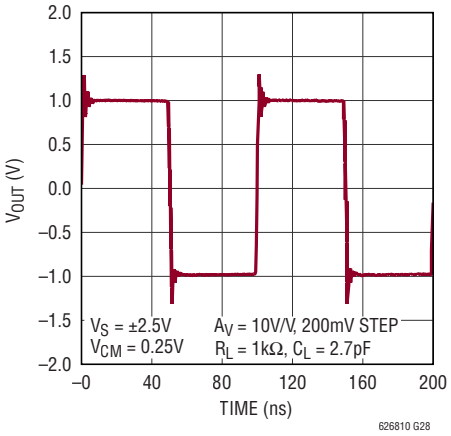


Large Signal Step Response

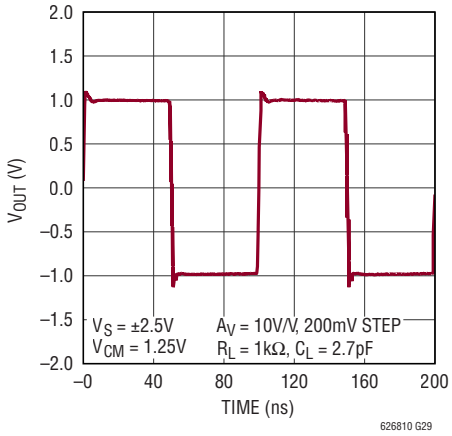


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

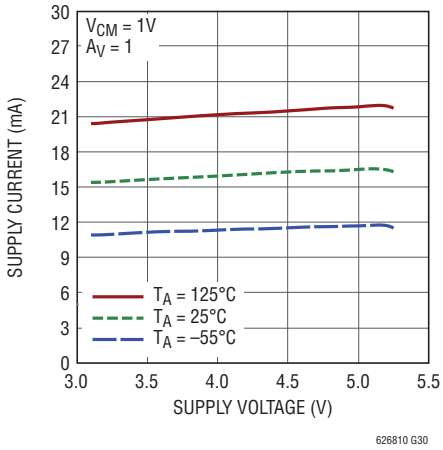
Large Signal Step Response



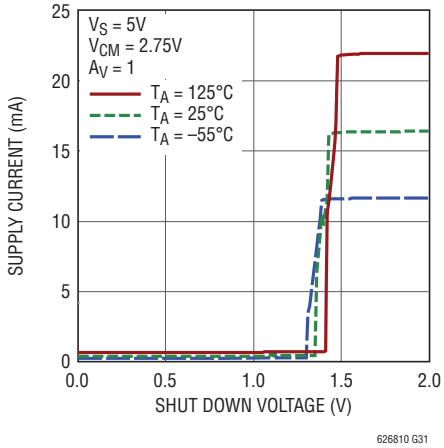
Large Signal Step Response



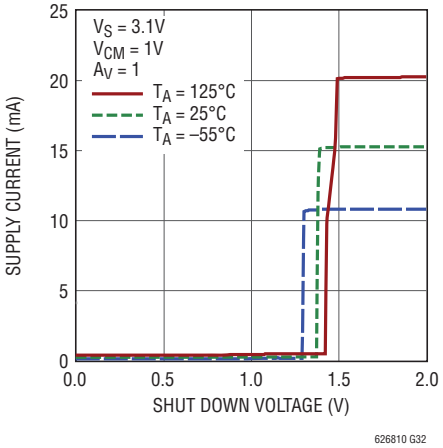
Supply Current vs Supply Voltage



Supply Current vs Shutdown Voltage



Supply Current vs Shutdown Voltage



PIN FUNCTIONS

–IN: Inverting Input of the Amplifier. The voltage range of this pin is from V^- to V^+ –0.5V.

+IN: Non-Inverting Input. The voltage range of this pin is from V^- to V^+ –0.5V.

V^+: Positive Power Supply. Total supply ($V^+ – V^-$) voltage is from 3.1V to 5.25V. Split supplies are possible as long as the total voltage between V^+ and V^- is between 3.1V and 5.25V. A bypass capacitor of 0.1µF should be used between V^+ to ground as close to the pin as possible.

V^-: Negative Power Supply. Normally tied to ground, it can also be tied to a voltage other than ground as long as the voltage difference between V^+ and V^- is between 3.1V and 5.25V. If it is not connected to ground, bypass it to ground with a capacitor of 0.1µF as close to the pin as possible.

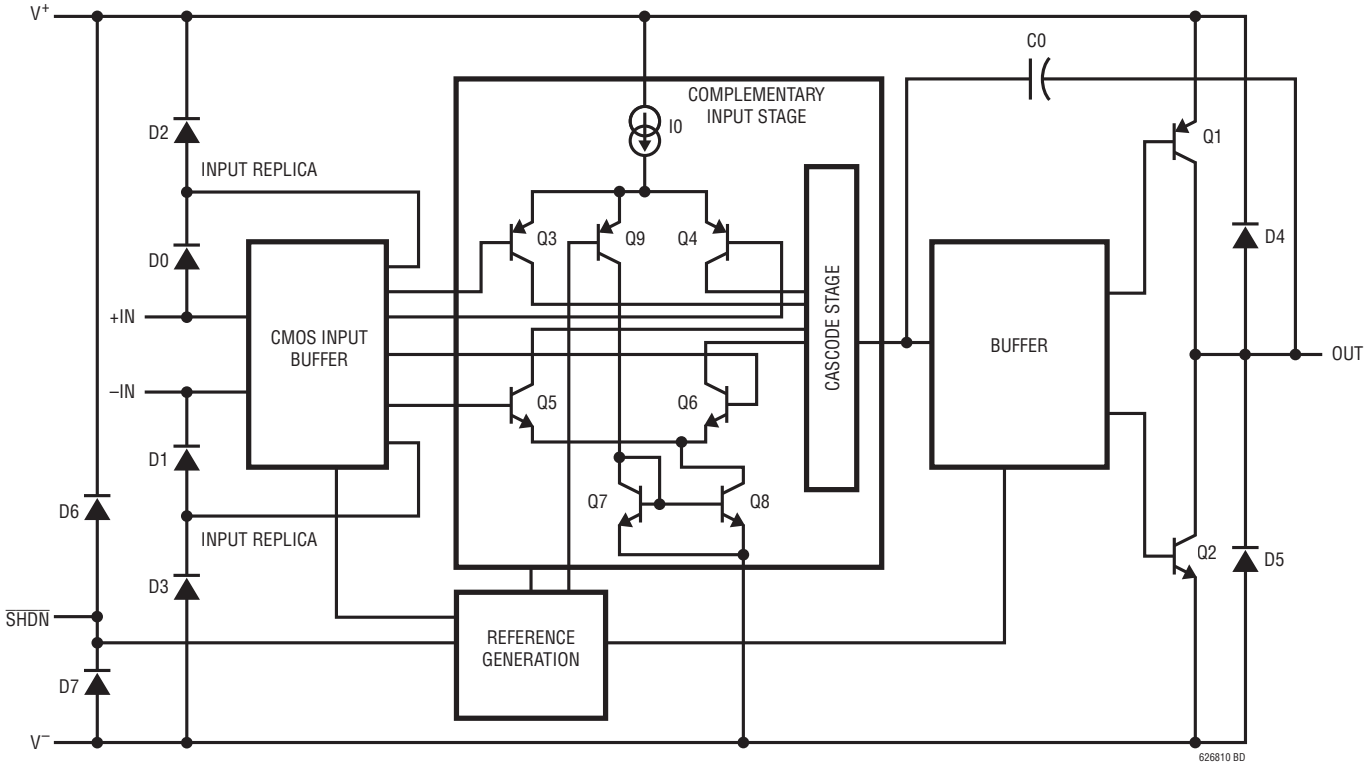
$\overline{SHDN}$, $\overline{SDA}$, $\overline{SDB}$: Active Low op amp shutdown, threshold is 0.75V above the negative supply, V^-. If left unconnected, the amplifier is enabled.

OUT: Amplifier Output.

NC: Not connected. May be used to create a guard ring around the input to guard against board leakage currents. See Applications Information section for more details.

SIMPLIFIED SCHEMATIC

LTC6268-10 Simplified Schematic Diagram



(ONE POLARITY SHOWN IN INPUT PINS)

OPERATION

The LTC6268-10/LTC6269-10 input signal range is specified from the negative supply to 0.5V below the positive power supply, while the output can swing from rail-to-rail. The schematic above depicts a simplified schematic of the amplifier.

The input pins drive a CMOS buffer stage. The CMOS buffer stage creates replicas of the input voltages to boot strap the protection diodes. In turn, the buffer stage drives a complementary input stage consisting of two differential amplifiers, active over different ranges of input common mode voltage. The main differential amplifier is active with input common mode voltages from the negative power supply to approximately 1.55V below the positive supply, with the second amplifier active over the remaining range to 0.5V below the positive supply rail. The buffer and output bias stage uses a special compensation technique ensuring stability of the op amp. The common emitter topology of output transistors Q1/Q2 enables the output to swing from rail-to-rail.

APPLICATIONS INFORMATION

Noise

To minimize the LTC6268-10's noise over a broad range of applications, careful consideration has been placed on input referred voltage noise (e_N), input referred current noise (i_N) and input capacitance C_{IN}.

For a transimpedance amplifier (TIA) application such as shown in Figure 1, all three of these op amp parameters, plus the value of feedback resistance R_F, contribute to noise behavior in different ways, and external components and traces will add to C_{IN}. It is important to understand the impact of each parameter independently. Input referred voltage noise (e_N) consists of flicker noise (or 1/f noise), which dominates at lower frequencies, and thermal noise which dominates at higher frequencies. For LTC6268-10, the 1/f corner, or transition between 1/f and thermal noise, is at 40kHz. The i_N and R_F contributions to input referred noise current at the minus input are relatively straight forward, while the e_N contribution is amplified by the noise gain. Because there is no gain resistor, the noise gain is calculated using feedback resistor(R_F) in conjunction with impedance of C_{IN} as $(1 + 2\pi R_F \bullet C_{IN} \bullet Freq)$, which increases with frequency. All of the contributions will be limited by the closed loop bandwidth. The equivalent input current noise is shown in Figure 2 and Figure 3, where e_N represents contribution from input referred voltage noise (e_N), i_N represents contribution from input referred current noise (i_N), and R_F represents contribution from feedback resistor (R_F). TIA gain (R_F) and capacitance at input (C_{IN}) are also shown on each figure. Comparing Figure 2 and Figure 3, i_N dominates at higher frequencies. At lower frequencies, the R_F contribution dominates. Since average wide band e_N is 4.0nV/$\sqrt{Hz}$ (see typical performance characteristics), R_F contribution will become a lesser factor at lower frequencies if R_F is less than 860Ω as indicated by the following equation:

$$\frac{eN/R_F}{\sqrt{4kT/R_F}} \geq 1$$

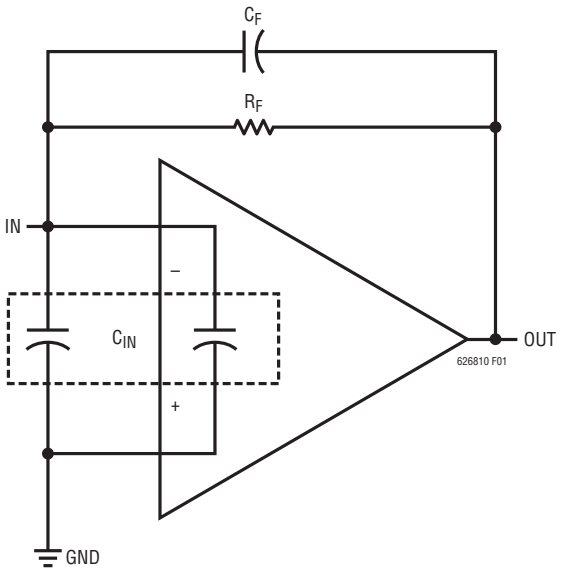


Figure 1. Simplified TIA Schematic

APPLICATIONS INFORMATION

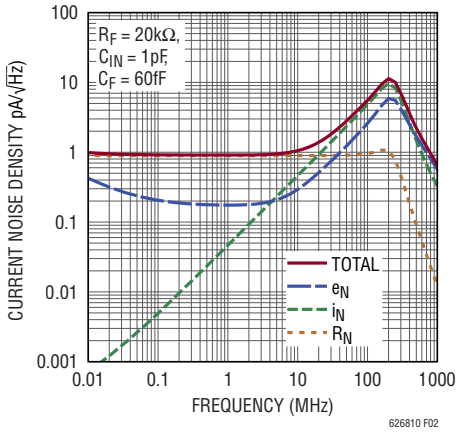


Figure 2

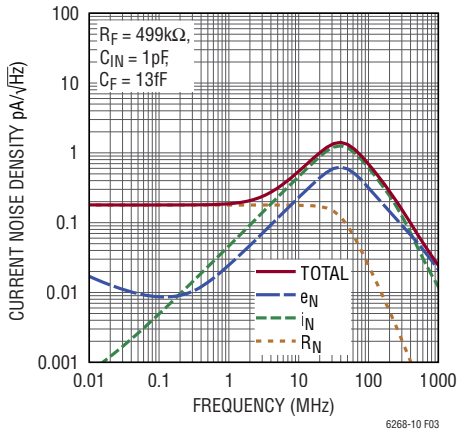


Figure 3

Optimizing the Bandwidth for TIA Application

The capacitance at the inverting input node can cause amplifier stability problems if left unchecked. When the feedback around the op amp is resistive (R_F), a pole will be created with $R_F||C_{IN}$. This pole can create excessive phase shift and possibly oscillation. Referring to Figure 1, the response at the output is:

$$\frac{R_F}{1+\frac{2\zeta s}{\omega}+\frac{S^2}{\omega^2}}$$

Where R_F is the DC gain of the TIA, ω is the natural frequency of the closed loop, which can be expressed as:

$$\omega = \sqrt{\frac{2\pi GBW}{R_F(C_{IN}+C_F)}}$$

Hence the maximum achievable bandwidth of TIA is:

$$f_{TIA}\,(Hz) = \sqrt{\frac{GBW}{2\pi R_F(C_{IN})}}$$

ζ is the damping factor of the loop, which can be expressed as:

$$\zeta = \frac{1}{2}\left(\sqrt{\frac{1}{2\pi GBW \bullet R_F(C_{IN}+C_F)}} + R_F\left(C_F+\frac{C_{IN}+C_F}{1+A_O}\right)\bullet\sqrt{\frac{2\pi GBW}{R_F(C_{IN}+C_F)}}\right)$$

Where C_{IN} is the total capacitance at the inverting input node of the op amp, GBW is the gain bandwidth of the op amp, and A_O is the DC open loop gain of the op amp.

The small capacitor C_F in parallel with R_F can introduce enough damping to stabilize the loop. By assuming $C_{IN} >> C_F$, the following condition needs to be met for C_F,

$$C_F > \sqrt{\frac{C_{IN}}{\pi \bullet GBW \bullet R_F}}$$

Since LTC6268-10 is a decompensated op amp with gain-of-10 stable, it requires that $C_{IN}/C_F \geq 10$. Table 1 shows the minimum and maximum C_F for R_F of 20k and 402k and C_{IN} of 1pF and 5pF.

Table 1. Min/Max C_F

R_F	C_{IN} = 1pF	C_{IN} = 5pF
20kΩ	60fF/100fF	140fF/500fF
402kΩ	13fF/100fF	31fF/500fF

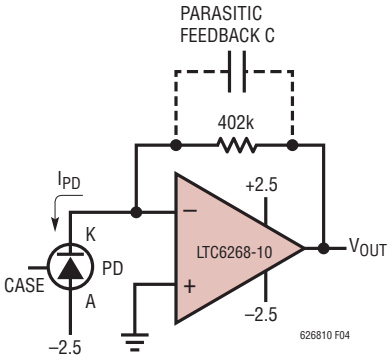
APPLICATIONS INFORMATION

Achieving Higher Bandwidth with Higher Gain TIAs

Good layout practices are essential to achieving best results from a TIA circuit. The following two examples show drastically different results from an LTC6268-10 in a 402k TIA. (See Figure 4.) The first example is with an 0805 resistor in a basic circuit layout. In a simple layout, without expending a lot of effort to reduce feedback capacitance, the rise time achieved is about 87ns (Figure 5), implying a bandwidth of 4MHz (BW = 0.35/t_r). In this case, the bandwidth of the TIA is limited not by the GBW of the LTC6268-10, but rather by the fact that the feedback capacitance is reducing the actual feedback impedance (the TIA gain itself) of the TIA. Basically, it's a resistor bandwidth limitation. The impedance of the 402kΩ is being reduced by its own parasitic capacitance at high frequency. From the 4MHz bandwidth and the 402k low frequency gain, we can estimate the total feedback capacitance as C = 1/(2π • 4MHz • 402kΩ) = 0.1pF. That's fairly low, but it can be reduced further.

With some extra layout techniques to reduce feedback capacitance, the bandwidth can be increased. Note that we are increasing the effective "bandwidth" of the 402k resistance. A very powerful method to reduce feedback capacitance is to shield the E field paths that give rise to the capacitance. In this particular case, the method is to place a ground trace between the resistor pads. Such a ground trace shields the output field from getting to the summing node end of the resistor and effectively shunts the field to ground instead. The trace increases the output load capacitance very slightly. See Figure 6 for a pictorial representation.

Figure 7 shows the dramatic increase in bandwidth simply by careful attention to low capacitance methods around the feedback resistance. Bandwidth and rise time went from 4MHz (87ns) to 34MHz (10.3ns), a factor of 8. The ground trace used for LTC6268-10 was much wider than that used in the case of the LTC6268 (see LTC6268 data sheet), extending under the entire resistor dielectric. Assuming all the bandwidth limit is due to feedback capacitance (which isn't fair), we can calculate an upper limit of C_f = 1/(2π • 402kΩ • 34MHz) = 11.6fF.



PD: OSI FCI-125G-006

Figure 4. LTC6268-10 and Low Capacitance Photodiode in a 402kΩ TIA

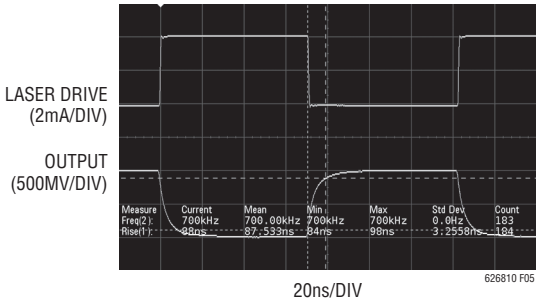


Figure 5. Time Domain Response of 402kΩ TIA without Extra Effort to Reduce Feedback Capacitance. Rise Time Is 87ns and BW Is 4MHz

APPLICATIONS INFORMATION

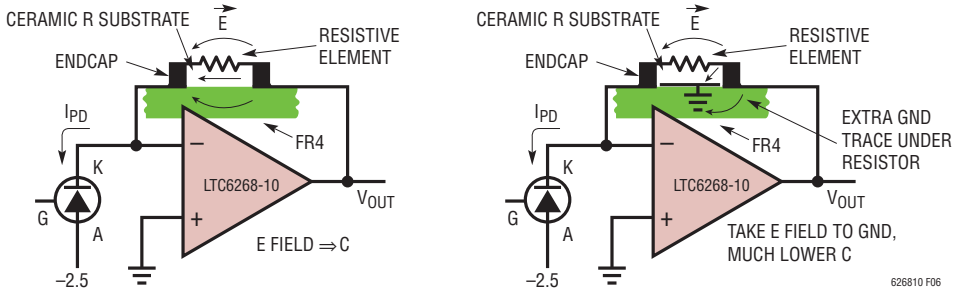


Figure 6. A Normal Layout at Left and a Field-Shunting Layout at Right. Simply Adding a Ground Trace Under the Feedback Resistor Does Much to Shunt Field Away from the Feedback Side and Dumps It to Ground. Note That the Dielectric Constant of Fr4 and Ceramic Is Typically 4, so Most of the Capacitance Is in the Solids and Not Through the Air. Feedback C is Reduced from 100fF at Left to 11.6fF at Right

Maintaining Ultralow Input Bias Current

Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of fA signals. High temperature applications are especially susceptible to these issues. For humid environments, surface coating may be necessary to provide a moisture barrier.

There are several factors to consider in a low input bias current circuit. At the femtoamp level, leakage sources can come from unexpected sources including adjacent signals on the PCB, both on the same layer and from internal layers, any form of contamination on the board from the assembly process or the environment, other components on the signal path and even the plastic of the device package. Care taken in the design of the system can mitigate these sources and achieve excellent performance.

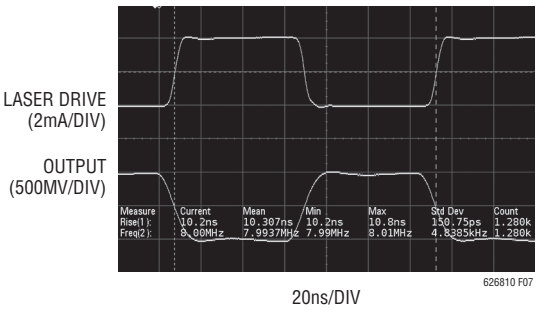


Figure 7. LTC6268-10 in a 402kΩ TIA with Extra Layout Effort to Reduce Feedback Capacitance Achieves 10.3ns Total System Rise Time, or 34MHz Total System Bandwidth

The choice of device package should be considered because although each has the same die internally, the pin spacing and adjacent signals influence the input bias current. The LTC6268-10/LTC6269-10 is available in SOIC, MSOP, DFN and SOT-23 packages. Of these, the SOIC has been designed as the best choice for low input bias current. It has the largest lead spacing which increases the impedance of the package plastic and the pinout is such that the two input pins are isolated on the far side of the package from the other signals. The gull-wing leads on this package also allow for better cleaning of the PCB and reduced contamination-induced leakage. The other packages have advantages in size and pin count but do so by reducing the input isolation. Leadless packages such as the DFN offer the minimum size but have the smallest pin spacing and may trap contaminants under the package.

The material used in the construction of the PCB can sometimes influence the leakage characteristics of the design. Exotic materials such as Teflon can be used to improve leakage performance in specific cases but they are generally not necessary if some basic rules are applied in the design of conventional FR4 PCBs. It is important to keep the high impedance signal path as short as possible on the board. A node with high impedance is susceptible to picking up any stray signals in the system so keeping it as short as possible reduces this effect. In some cases, it may be necessary to have a metallic shield over this portion of the circuit. However, metallic shielding increases capacitance. Another technique for avoiding leakage paths is to cut slots in the PCB. High impedance circuits are also

APPLICATIONS INFORMATION

susceptible to electrostatic as well as electromagnetic effects. The static charge carried by a person walking by the circuit can induce an interference on the order of 100's of femtoamps. A metallic shield can reduce this effect as well.

The layout of a high impedance input node is very important. Other signals should be routed well away from this signal path and there should be no internal power planes under it. The best defense from coupling signals is distance and this includes vertically as well as on the surface. In cases where the space is limited, slotting the board around the high impedance input nodes can provide additional isolation and reduce the effect of contamination. In electrically noisy environments the use of driven guard rings around these nodes can be effective (see Figure 8). Adding any additional components such as filters to the high impedance input node can increase leakage. The leakage current of a ceramic capacitor is orders of magnitude larger than the bias current of this device. Any filtering will need to be done after this first stage in the signal chain.

Driving Capacitive Load

The layout of the output node is also very important since LTC6268-10/LTC6269-10 is very sensitive to capacitive loading due to the very high gain-bandwidth-product. Appreciable ringing will be observed when capacitive loading is more than 5pF.

Low Input Offset Voltage

The LTC6268-10 has a maximum offset voltage of ±2.5mV (PNP region) over temperature. The low offset voltage is essential for precision applications. There are 2 different input stages that are used depending on the input common mode voltage. To increase the versatility of the LTC6268-10, the offset voltages are trimmed for both regions of operation.

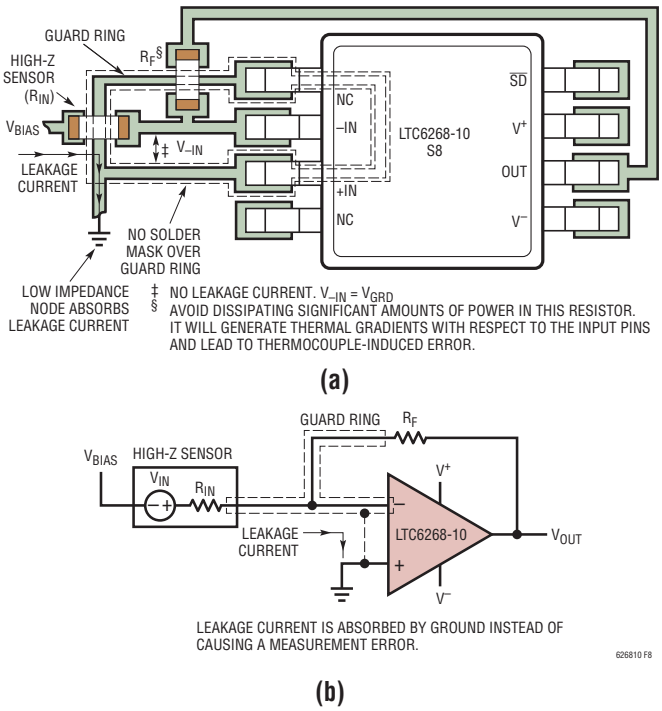


Figure 8. Example Layout of Inverting Amplifier (or Transimpedance) with Leakage Guard Ring

Rail-to-Rail Output

The LTC6268-10 has a rail-to-rail output stage that has excellent output drive capability. It is capable of delivering over ±40mA of output drive current over temperature. Furthermore, the output can reach within 200mV of either rail while driving ±10mA. Attention must be paid to keep the junction temperature of the IC below 150°C.

Input Protection

To prevent breakdown of internal devices in the input stage, the two op amp inputs should NOT be separated by more than 2.0V. To help protect the input stage, internal circuitry will engage automatically if the inputs are separated by >2.0V and input currents will begin to flow. In all cases, care should be taken so that these currents remain less than 1mA. Additionally, if only one input is driven, internal circuitry will prevent any breakdown condition under

APPLICATIONS INFORMATION

transient conditions. The worst-case differential input voltage usually occurs when the +input is driven and the output is accidentally shorted to ground while in a unity gain configuration.

ESD

ESD Protection devices can be seen in the simplified schematic. The +IN and –IN pins use a sophisticated method of ESD protection that incorporates a total of 4 reverse-biased diodes connected as 2 series diodes to each rail. To maintain extremely low input bias currents, the center node of each of these series diode chains is driven by a buffered copy of the input voltage. This maintains the two diodes connected directly to the input pins at low reverse bias, minimizing leakage current of these ESD diodes to the input pins.

The remaining pins have traditional ESD protection, using reverse-biased ESD diodes connected to each power supply rail. Care should be taken to make sure that the voltages on these pins do not exceed the supply voltages by more than 100mV or these diodes will begin to conduct large amounts of current.

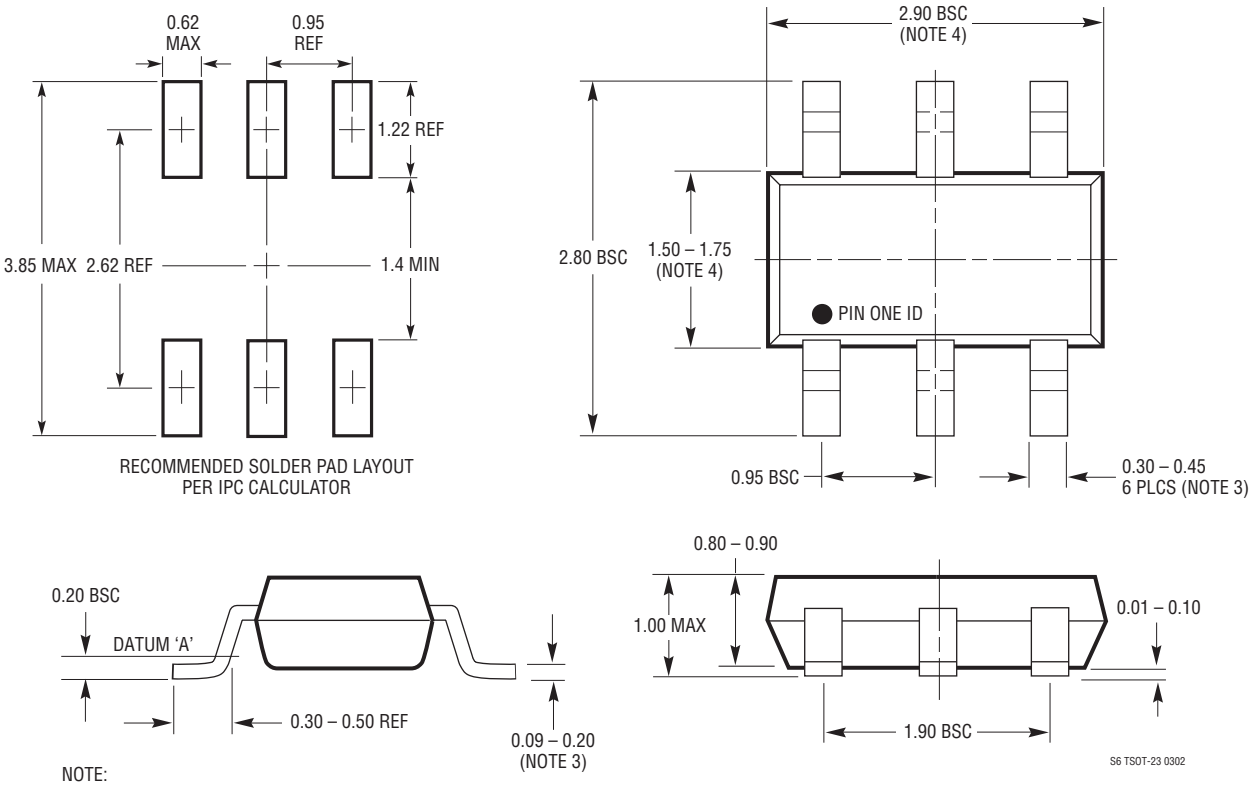
Shutdown

The LTC6268-10S6, LTC6268-10S8, and LTC6268-10DD have $\overline{SHDN}$ pins that can shut down the amplifier to less than 1.2mA supply current per amplifier. The $\overline{SHDN}$ pin voltage needs to be within 0.75V of V^- for the amplifier to shut down. During shutdown, the output will be in a high output resistance state, so the LTC6268-10 is suitable for multiplexer applications. The internal circuitry is kept in a low current active state for fast recovery. When left floating, the $\overline{SHDN}$ pin is internally pulled up to the positive supply and the amplifier is enabled.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

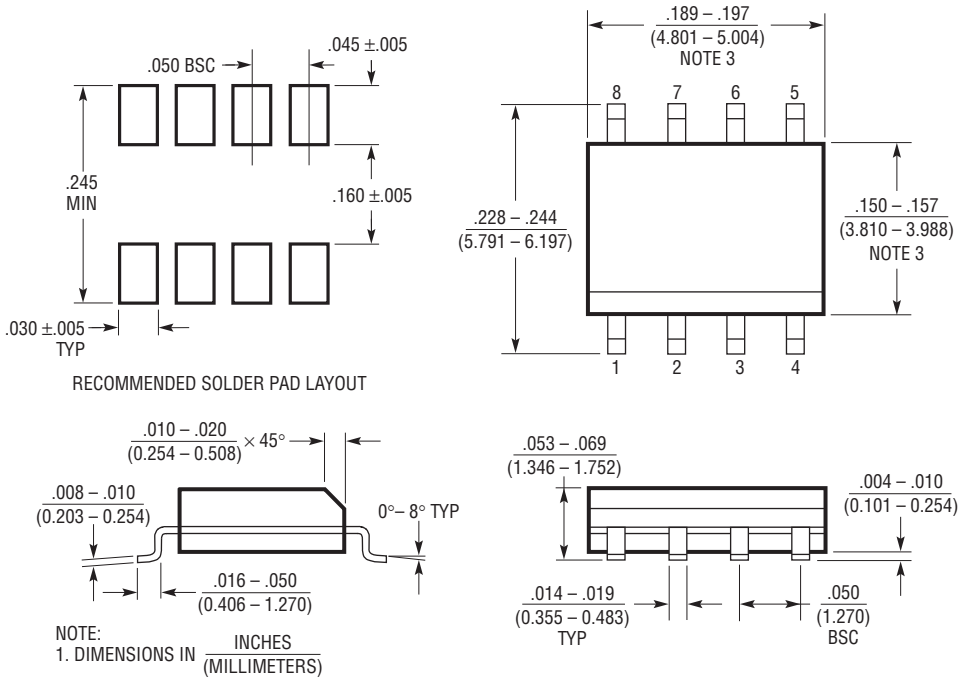


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



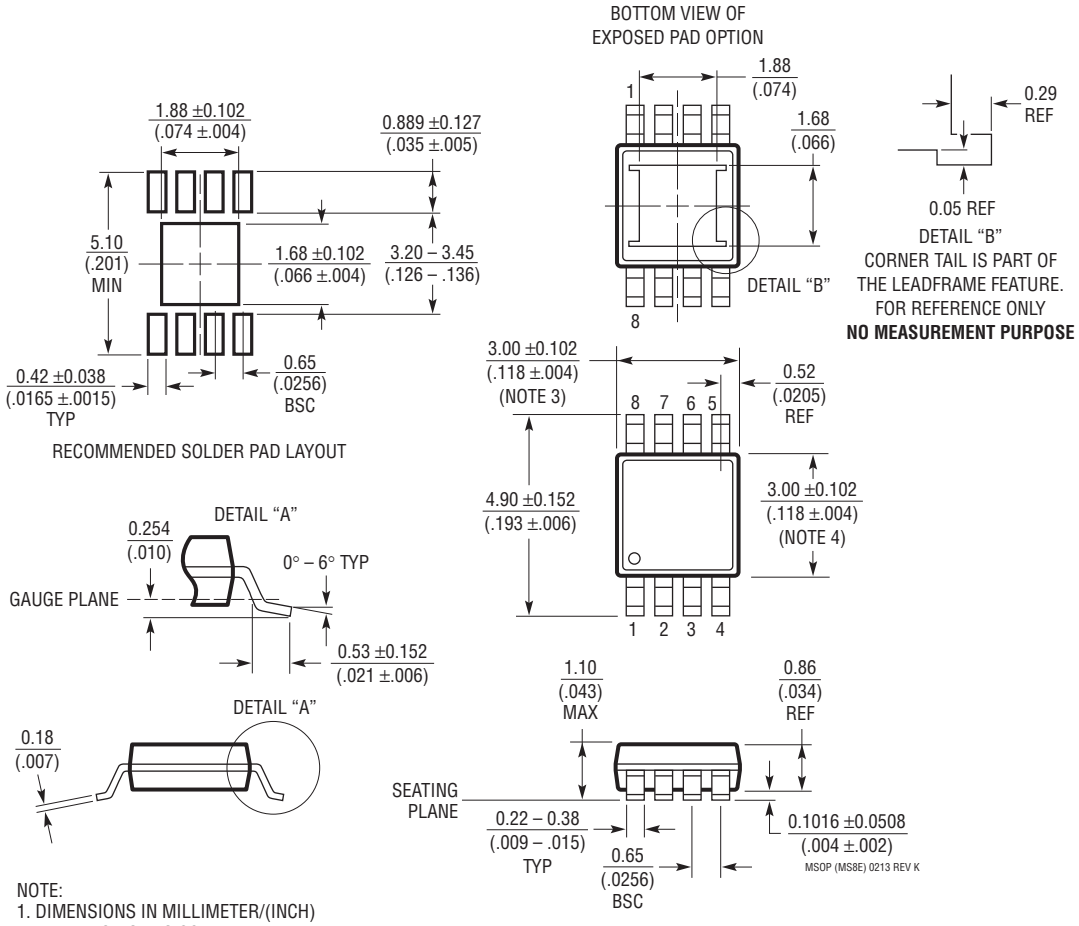
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)

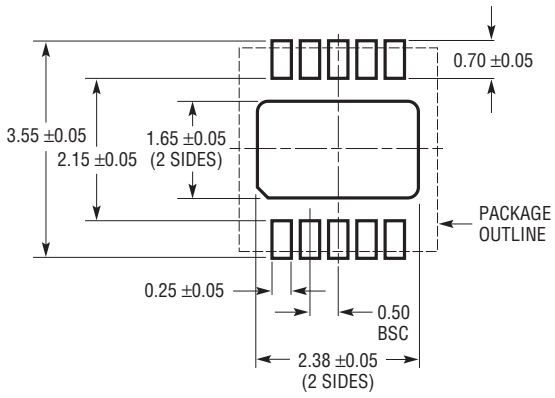


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

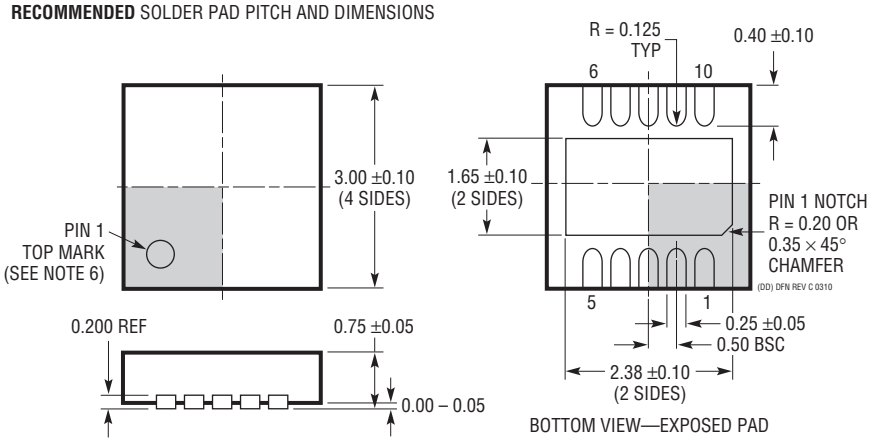
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

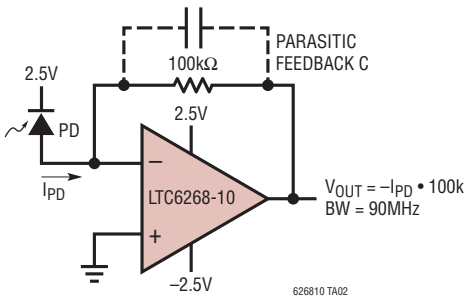


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

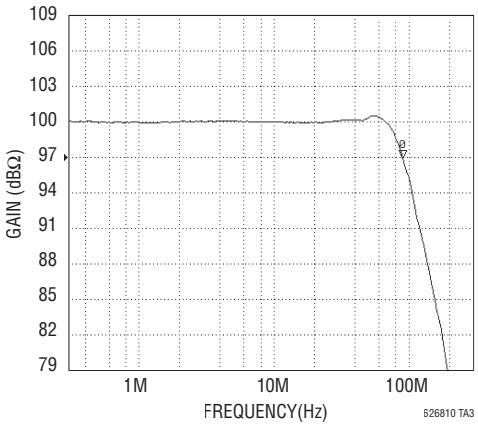
TYPICAL APPLICATION

100kΩ Gain 90MHz Transimpedance Amplifier



PD = OSI OPTOELECTRONICS, FCI-125G-006
OUTPUT NOISE = 20mV$_{P-P}$ MEASURED ON A 100MHz BW

100kΩ TIA Frequency Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Op Amps		
LTC6268/LTC6269	500MHz Ultra-Low Bias Current FET Input Op Amp	Unity Gain Stable, Ultra Low Input Bias Current (3fA), 500MHz GBW
LTC6244	Dual 50MHz, Low Noise, Rail-to-Rail, CMOS Op Amp	Unity Gain Stable, 1pA Input Bias Current, 100µV Max Offset.
LTC6240/LTC6241/ LTC6242	18MHz, Low Noise, Rail-to-Rail Output, CMOS Op Amp	18MHz GBW, 0.2pA Input Current, 125µV Max Offset.
LTC6252/LTC6253/ LTC6254	720MHz, 3.5mA Power Efficient Rail-to-Rail I/O Op Amp	720MHz GBW, Unity Gain Stable, Low Noise
LTC6246/LTC6247/ LTC6248	180MHz, 1mA Power Efficient Rail-to-Rail I/O Op Amps	180MHz GBW, Unity Gain Stable, Low Noise
LT1818	400MHz, 2500V/µs, 9mA Single Operational Amplifier	Unity Gain Stable, 6nV/√Hz Unity Gain Stable
LT6236	215MHz, Rail-to-Rail Output, 1.1nV/√Hz, 3.5mA Op Amp Family	350µV Max Offset Voltage, 3V to 12.6V Supply
LT6411	650MHz Differential ADC Driver/Dual Selectable Amplifier	SR 3300V/µs, 6ns 0.1% Settling.
SAR ADC		
LTC2376-18/ LTC2377-18/ LTC2378-18/ LTC2379-18	18-Bit, 250ksps to 1.6Msps, Low Power SAR ADC, 102dB SNR	18mW at 1.6Msps, 3.4µW at 250sps, –126dB THD.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC6268-10
LT 0415 • PRINTED IN USA

OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers

1 Features

- Superior Sound Quality
- Ultralow Noise: 1.1 nV/√Hz at 1 kHz
- Ultralow Distortion: 0.000015% at 1 kHz
- High Slew Rate: 27 V/µs
- Wide Bandwidth: 40 MHz (G = +1)
- High Open-Loop Gain: 130 dB
- Unity Gain Stable
- Low Quiescent Current: 3.6 mA per Channel
- Rail-to-Rail Output
- Wide Supply Range: ±2.25 V to ±18 V
- Single and Dual Versions Available

2 Applications

- Professional Audio Equipment
- Microphone Preamplifiers
- Analog and Digital Mixing Consoles
- Broadcast Studio Equipment
- Audio Test And Measurement
- High-End A/V Receivers

3 Description

The OPA1611 (single) and OPA1612 (dual) bipolar-input operational amplifiers achieve very low 1.1-nV/√Hz noise density with an ultralow distortion of 0.000015% at 1 kHz. The OPA1611 and OPA1612 offer rail-to-rail output swing to within 600 mV with a 2-kΩ load, which increases headroom and maximizes dynamic range. These devices also have a high output drive capability of ±30 mA.

These devices operate over a very wide supply range of ±2.25 V to ±18 V, on only 3.6 mA of supply current per channel. The OPA1611 and OPA1612 op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

The dual version features completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

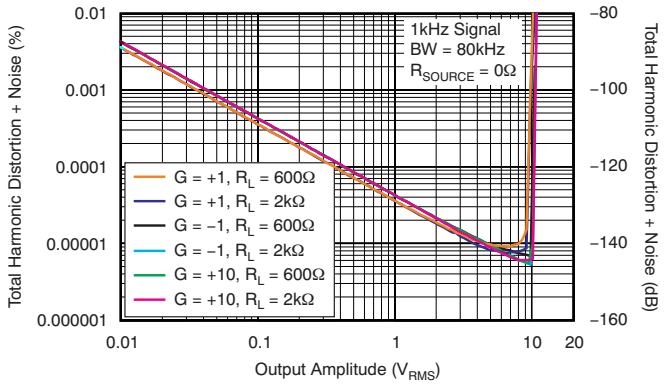
Both the OPA1611 and OPA1612 are available in SOIC-8 packages and the OPA1612 is available in SON-8. These devices are specified from –40°C to +85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1611	SOIC (8)	4.90 mm × 3.91 mm
OPA1612	SOIC (8)	4.90 mm × 3.91 mm
	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

THD+N Ratio vs Output Amplitude



Functional Block Diagram

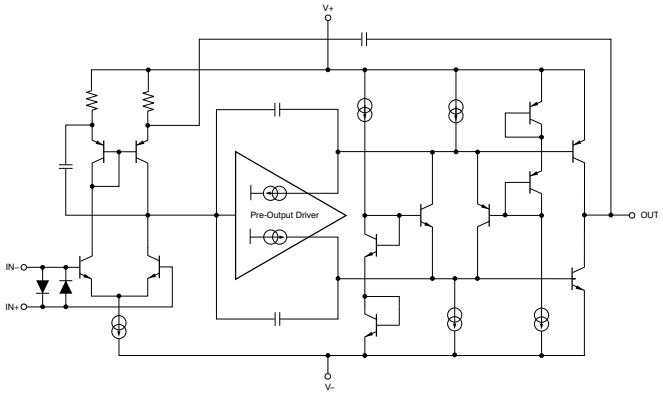


Table of Contents

4 Revision History

Changes from Revision B (July 2011) to Revision C **Page**

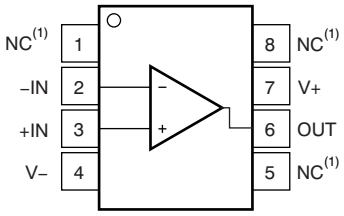
- Changed format to meet latest data sheet standards; added new sections, and moved existing sections ... 1
- Added SON-8 (DRG) package to data sheet ... 1
- Changed SO to SOIC throughout document to match industry standard term ... 1
- Added front-page curve ... 1
- Added title to block diagram ... 1
- Deleted Package Information table; see package option addendum ... 3

Changes from Revision A (August 2009) to Revision B **Page**

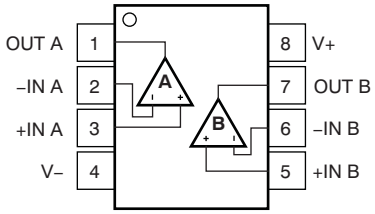
- Revised *Features* list items ... 1
- Updated front-page figure ... 1
- Added max specification for input voltage noise density at f = 1kHz ... 5
- Corrected typo in footnote 1 for Electrical Characteristics ... 5
- Revised Figure 4 ... 7
- Updated Figure 7 ... 7
- Changed Figure 9 ... 7
- Revised Figure 11 ... 7
- Corrected typo in Figure 15 ... 8
- Updated Figure 29 ... 12
- Revised fourth paragraph of *Electrincal Overstress* section ... 13
- Revised table in Figure 34 ... 17

5 Pin Configuration and Functions

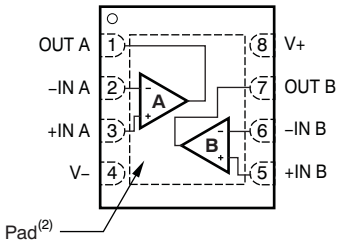
D Package
OPA1611, SOIC-8
(Top View)



D Package
OPA1612, SOIC-8
(Top View)



DRG Package
OPA1612, SON-8
(Top View)



(1) NC denotes no internal connection. Pin can be left floating or connected to any voltage between (V–) and (V+).

(2) Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad improves heat dissipation and provides specified performance.

Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	D (OPA1611)	D (OPA1612)	DRG (OPA1612)		
–IN	2	—	—	I	Inverting input
+IN	3	—	—	I	Noninverting input
–IN A	—	2	2	I	Inverting input, channel A
+IN A	—	3	3	I	Noninverting input, channel A
–IN B	—	6	6	I	Inverting input, channel B
+IN B	—	5	5	I	Noninverting input, channel B
NC	1, 5, 8	—	—	—	No internal connection
OUT	6	—	—	O	Output
OUT A	—	1	1	O	Output, channel A
OUT B	—	7	7	O	Output, channel B
V–	4	4	4	—	Negative (lowest) power supply
V+	7	8	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)		40	V
Input voltage		(V–) – 0.5	(V+) + 0.5	V
Input current (all pins except power-supply pins)			±10	mA
Output short-circuit(2)			Continuous	
Operating temperature	(T_A)	–55	+125	°C
Junction temperature	(T_J)		200	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–3000	3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	
		Machine model (MM)	–200	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		+85	°C

6.4 Electrical Characteristics: V_S = ±2.25 V to ±18 V

At T_A = +25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 3 V_{RMS}		0.000015%		
				–136		dB
IMD	Intermodulation distortion	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz), G = +1, V_O = 3 V_{RMS}		0.000015%		
				–136		dB
		DIM 30 (3-kHz square wave and 15-kHz sine wave), G = +1, V_O = 3 V_{RMS}		0.000012%		
				–138		dB
		CCIF twin-tone (19 kHz and 20 kHz), G = +1, V_O = 3 V_{RMS}		0.000008%		
				–142		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 100		80		MHz
		G = 1		40		MHz
SR	Slew rate	G = –1		27		V/µs
	Full-power bandwidth(1)	V_O = 1 V_{PP}		4		MHz
	Overload recovery time	G = –10		500		ns
	Channel separation (dual)	f = 1 kHz		–130		dB
NOISE						
	Input voltage noise	f = 20 Hz to 20 kHz		1.2		μV_{PP}
e_n	Input voltage noise density(2)	f = 10 Hz		2		nV/√Hz
		f = 100 Hz		1.5		nV/√Hz
		f = 1 kHz		1.1	1.5	nV/√Hz
I_n	Input current noise density	f = 10 Hz		3		pA/√Hz
		f = 1 kHz		1.7		pA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±15 V		±100	±500	µV
dV_{OS}/dT	V_{OS} over temperature(2)	T_A = –40°C to +85°C		1	4	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V		0.1	1	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±60	±250	nA
		VCM = 0 V, DRG package only		±60	±300	nA
	I_B over temperature(2)	T_A = –40°C to +85°C			350	nA
I_{OS}	Input offset current	V_{CM} = 0 V		±25	±175	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V	110	120		dB
INPUT IMPEDANCE						
	Differential			20k || 8		Ω || pF
	Common-mode			10^9 || 2		Ω || pF

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.

Electrical Characteristics: V_S = ±2.25 V to ±18 V (continued)

At T_A = +25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ	114	130		dB
		(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 2 kΩ	110	114		dB
OUTPUT						
V_{OUT}	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 114 dB	(V–) + 0.2		(V+) – 0.2	V
		R_L = 2 kΩ, A_{OL} ≥ 110 dB	(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current		See Figure 27			mA
Z_O	Open-loop output impedance		See Figure 28			Ω
I_{SC}	Short-circuit current			+55		mA
				–62		mA
C_{LOAD}	Capacitive load drive		See Typical Characteristics			pF
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		3.6	4.5	mA
	I_Q over Temperature(3)	T_A = –40°C to +85°C			5.5	mA
TEMPERATURE RANGE						
	Specified range		–40		+85	°C
	Operating range		–55		+125	°C
θ_{JA}	Thermal resistance, SOIC-8			150		°C/W

(3) Specified by design and characterization.

6.5 Typical Characteristics

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

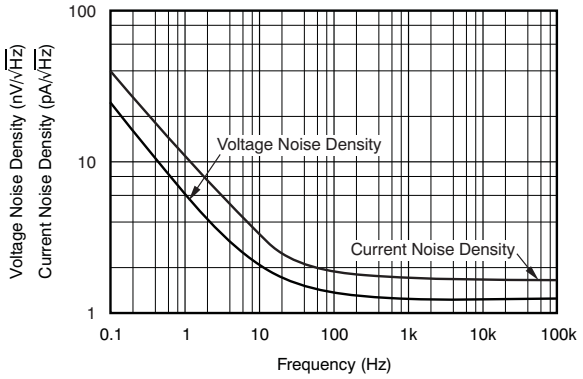


Figure 1. Input Voltage Noise Density and Input Current Noise Density vs Frequency

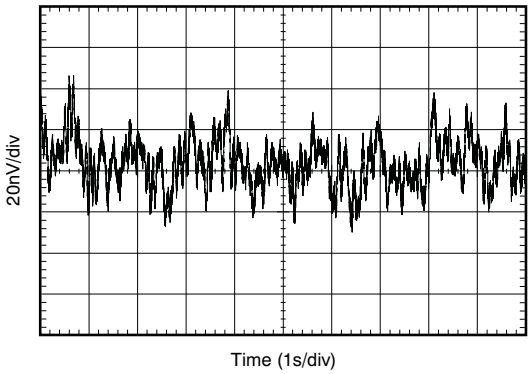


Figure 2. 0.1-Hz to 10-Hz Noise

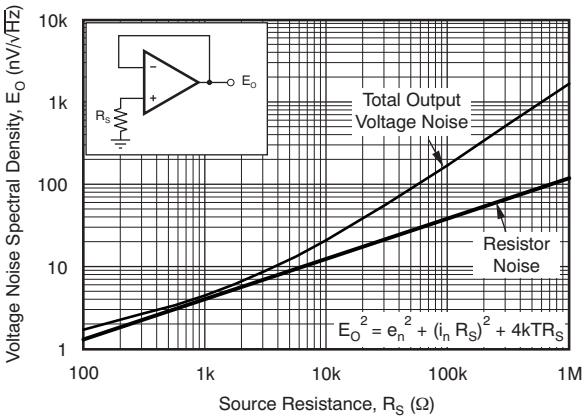


Figure 3. Voltage Noise vs Source Resistance

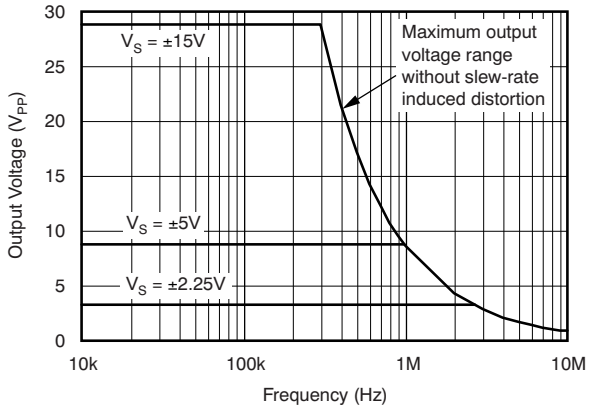


Figure 4. Maximum Output Voltage vs Frequency

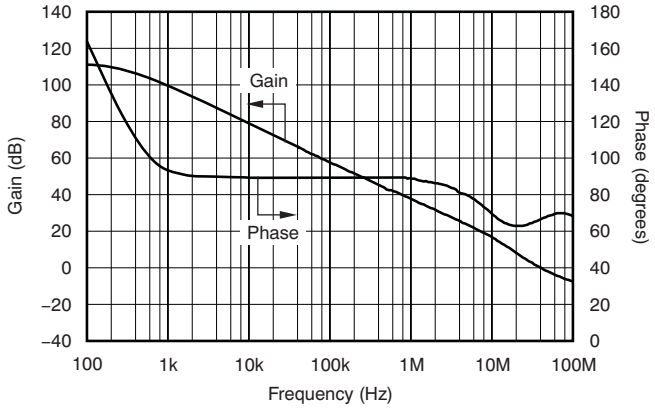


Figure 5. Gain and Phase vs Frequency

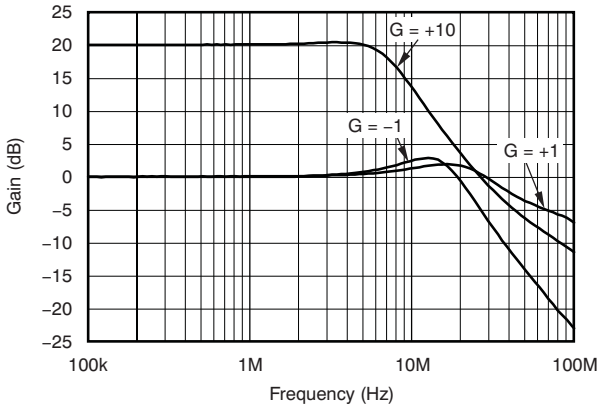


Figure 6. Closed-Loop Gain vs Frequency

Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

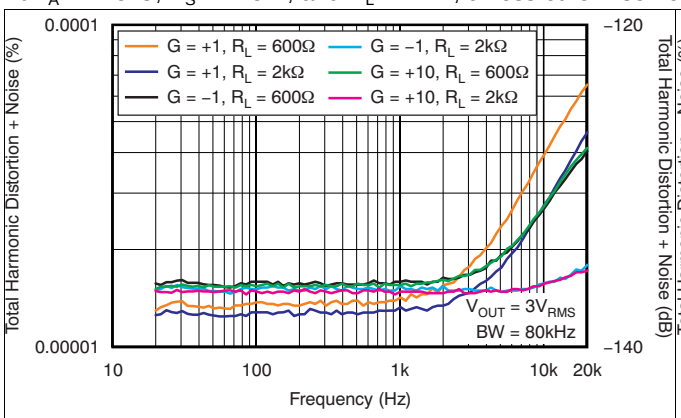


Figure 7. THD+N Ratio vs Frequency

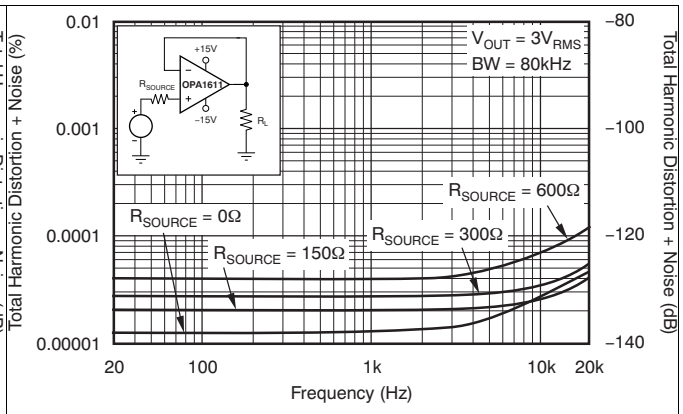


Figure 8. THD+N Ratio vs Frequency

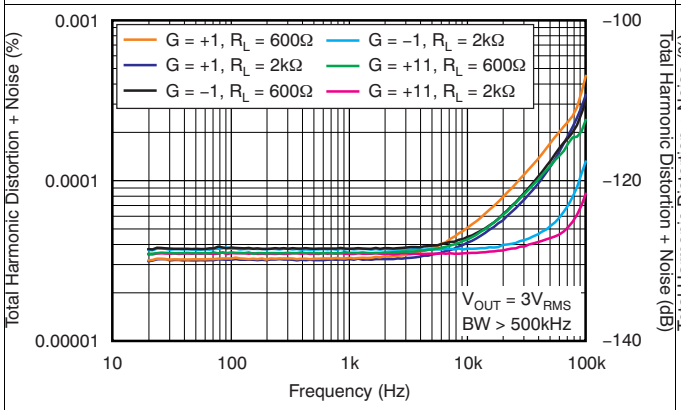


Figure 9. THD+N Ratio vs Frequency

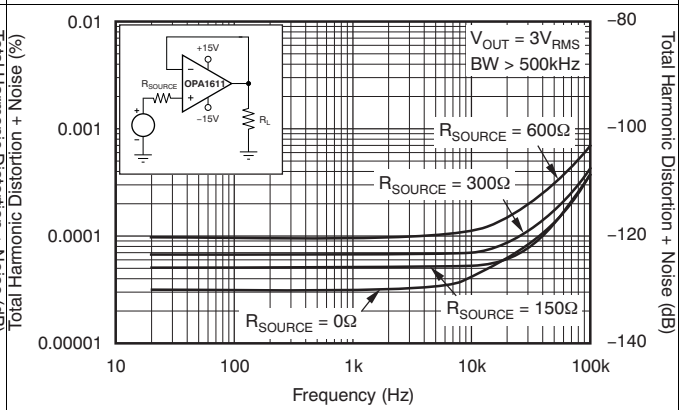


Figure 10. THD+N Ratio vs Frequency

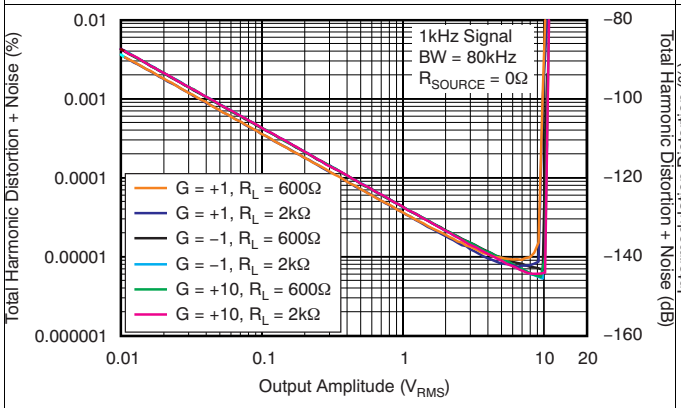


Figure 11. THD+N Ratio vs Output Amplitude

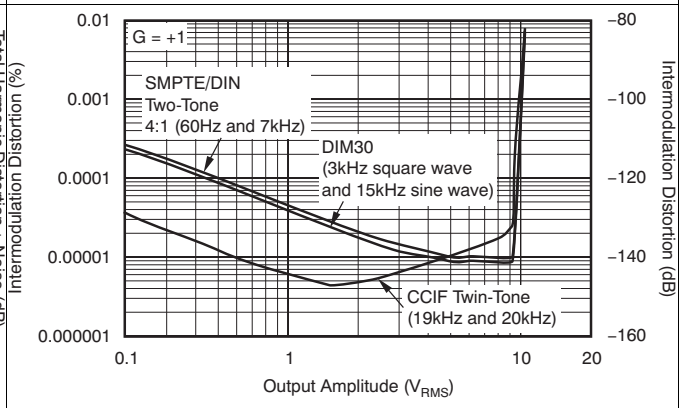


Figure 12. Intermodulation Distortion vs Output Amplitude

Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

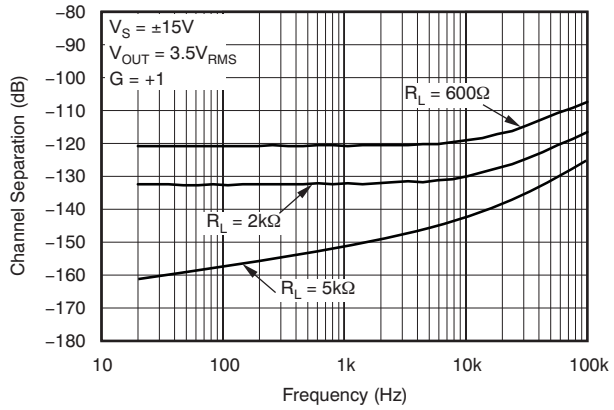


Figure 13. Channel Separation vs Frequency

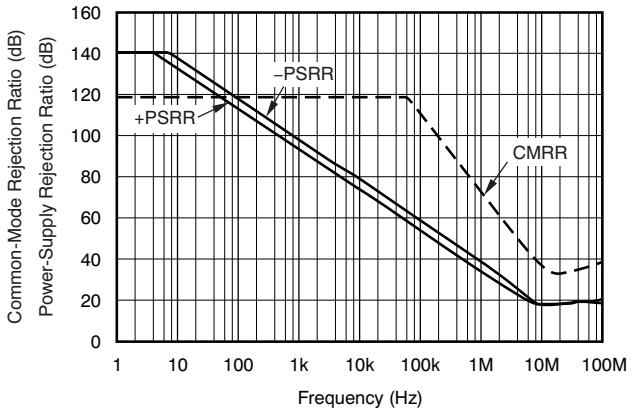


Figure 14. CMRR and PSRR vs Frequency (Referred to Input)

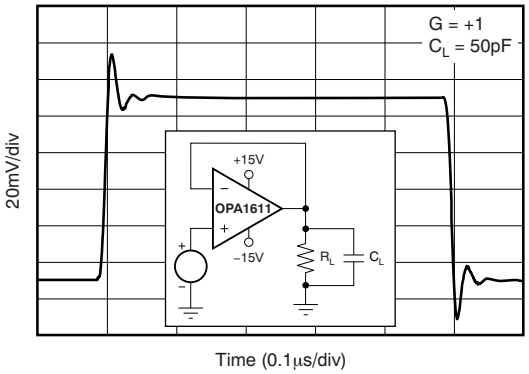


Figure 15. Small-Signal Step Response (100 mV)

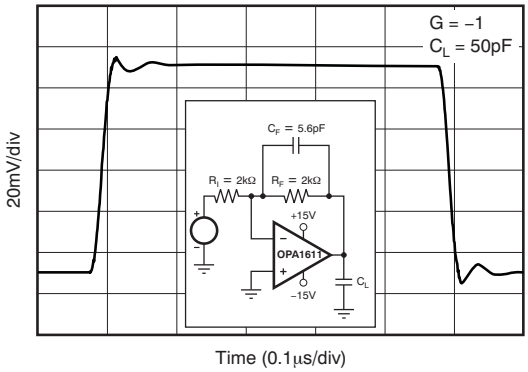


Figure 16. Small-Signal Step Response (100 mV)

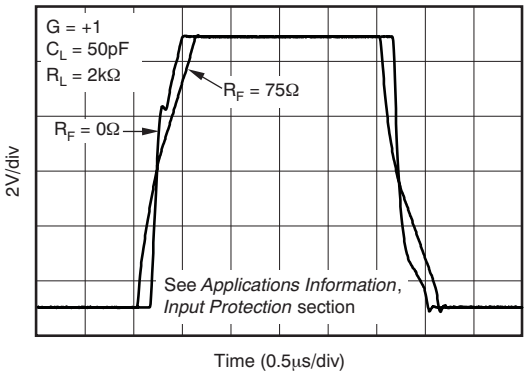


Figure 17. Large-Signal Step Response

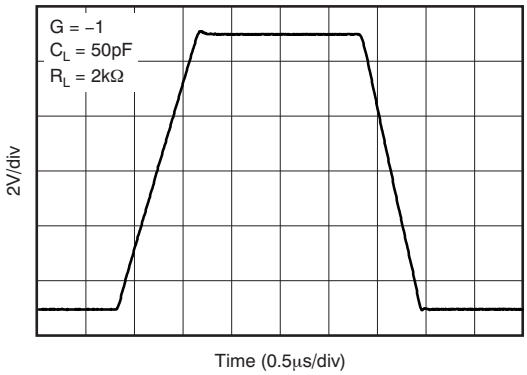


Figure 18. Large-Signal Step Response

Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

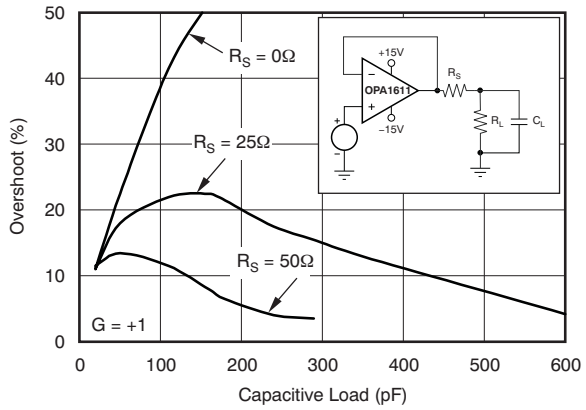


Figure 19. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

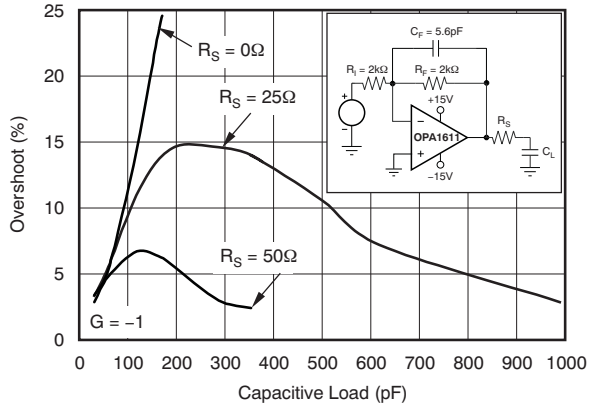


Figure 20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

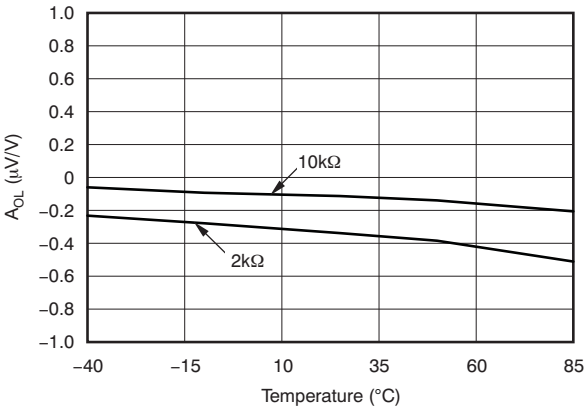


Figure 21. Open-Loop Gain vs Temperature

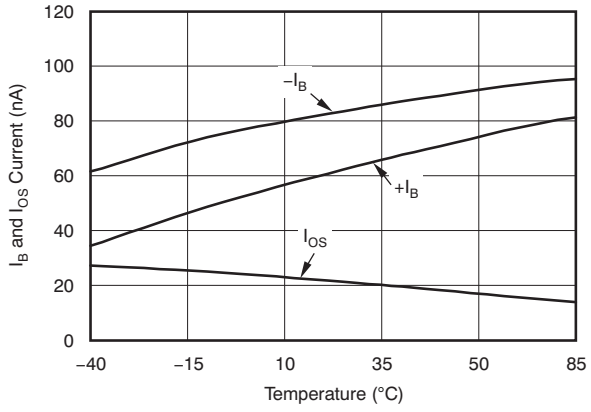


Figure 22. I_B and I_{OS} vs Temperature

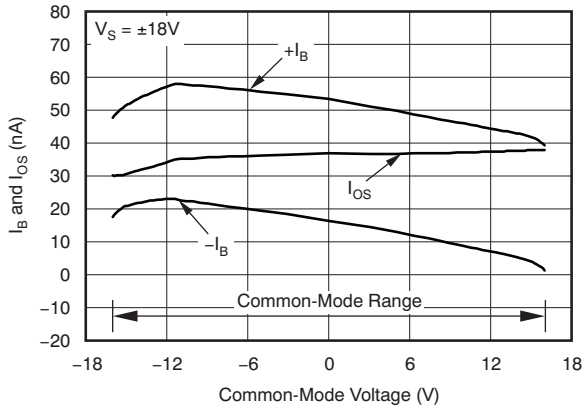


Figure 23. I_B and I_{OS} vs Common-Mode Voltage

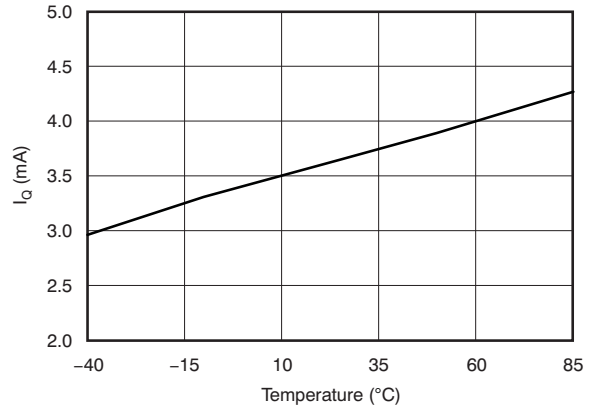


Figure 24. Quiescent Current vs Temperature

Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

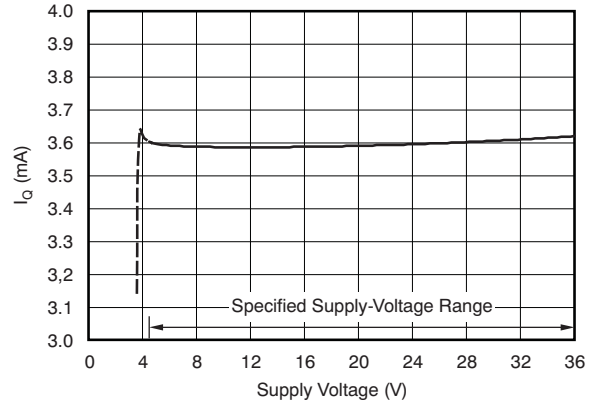


Figure 25. Quiescent Current vs Supply Voltage

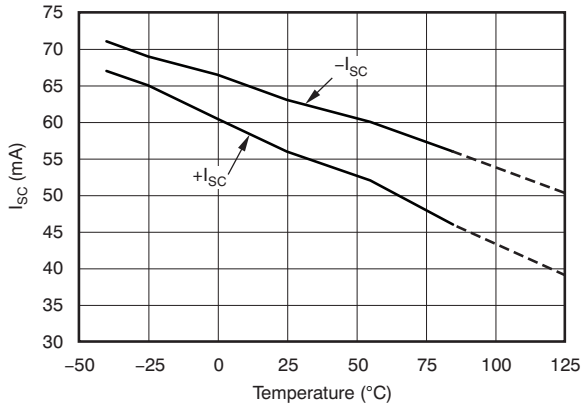


Figure 26. Short-Circuit Current vs Temperature

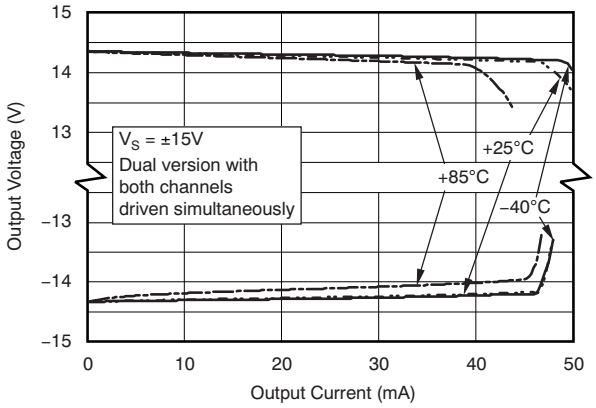


Figure 27. Output Voltage vs Output Current

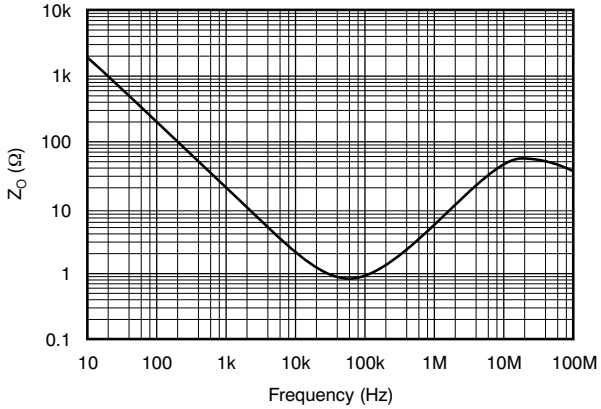


Figure 28. Open-Loop Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The OPA161x family of bipolar-input operational amplifiers achieve very low 1.1-nV/√Hz noise density with an ultralow distortion of 0.000015% at 1 kHz. The rail-to-rail output swing, within 600 mV with a 2-kΩ load, increases headroom and maximizes dynamic range. These devices also have a high output drive capability of ±40 mA. The wide supply range of ±2.25 V to ±18 V, on only 3.6 mA of supply current per channel, makes them applicable to both 5V systems and 36V audio applications. The OPA1611 and OPA1612 op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

7.2 Functional Block Diagram

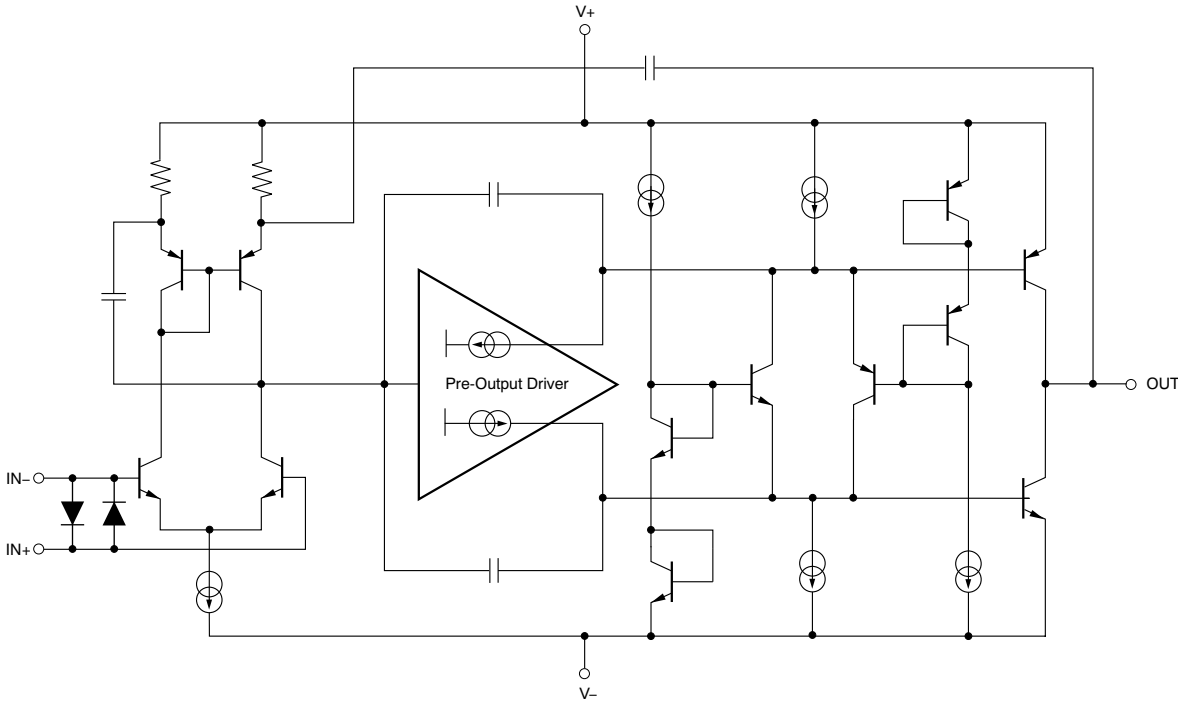


Figure 29. OPA1611 Simplified Schematic

7.3 Feature Description

7.3.1 Power Dissipation

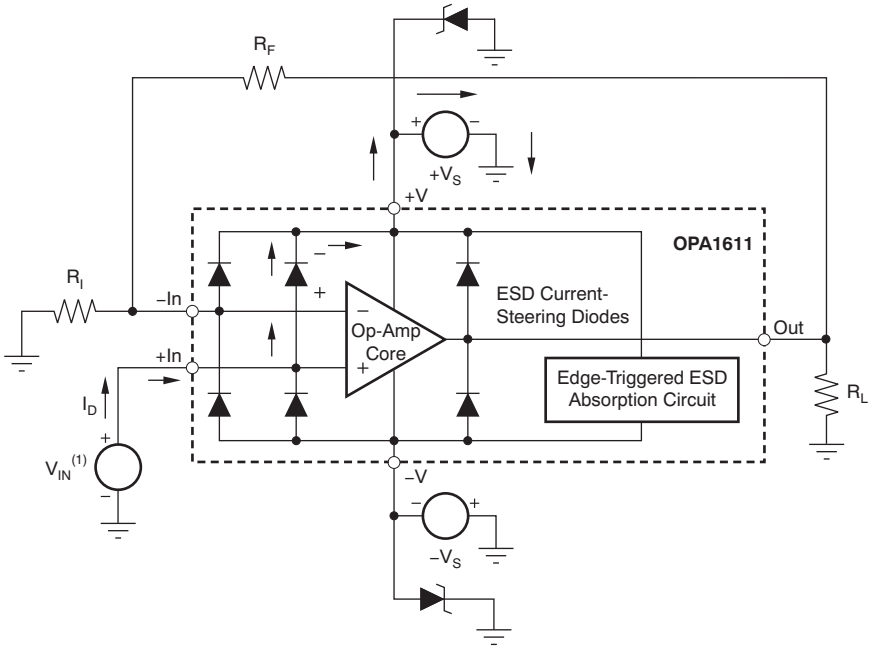
The OPA1611 and OPA1612 series op amps are capable of driving 2-kΩ loads with a power-supply voltage up to ±18 V. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA1611 and OPA1612 series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

7.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Feature Description (continued)

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 30 shows the ESD circuits contained in the OPA161x series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) $V_{IN} = +V_S + 500$ mV.

Figure 30. Equivalent Internal ESD Circuitry and its Relation to a Typical Circuit Application

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse when discharged through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage to the core. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device internal to the OPA1611 triggers when a fast ESD voltage pulse is impressed across the supply pins. Once triggered, the absorption device quickly activates and clamps the ESD pulse to a safe voltage level.

When the operational amplifier connects into a circuit such as the one Figure 30 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, some of the internal ESD protection circuits may possibly be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 30 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

Feature Description (continued)

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, the result depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins; see Figure 30. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener diode voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

7.3.3 Operating Voltage

The OPA161x series op amps operate from ±2.25-V to ±18-V supplies while maintaining excellent performance. The OPA161x series can operate with as little as +4.5 V between the supplies and with up to +36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA161x series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of T_A = –40°C to +85°C. Parameters that vary with operating voltage or temperature are shown in the Typical Characteristics.

7.3.4 Input Protection

The input terminals of the OPA1611 and the OPA1612 are protected from excessive differential voltage with back-to-back diodes, as Figure 31 shows. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 17 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) or a feedback resistor (R_F) can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA1611 and is examined in the *Noise Performance* section. Figure 31 shows an example configuration when both current-limiting input and feedback resistors are used.

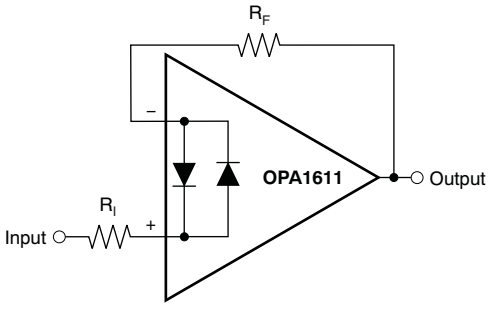


Figure 31. Pulsed Operation

8 Application and Implementation

8.1 Application Information

The OPA1611 and OPA1612 are unity-gain stable, precision op amps with very low noise; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Noise Performance

Figure 32 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA1611 (GBW = 40 MHz, G = +1) is shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the OPA161x series op amps makes them a good choice for use in applications where the source impedance is less than 1 kΩ.

8.2.1 Detailed Design Procedure

The equation in Figure 32 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

8.2.2 Application Curve

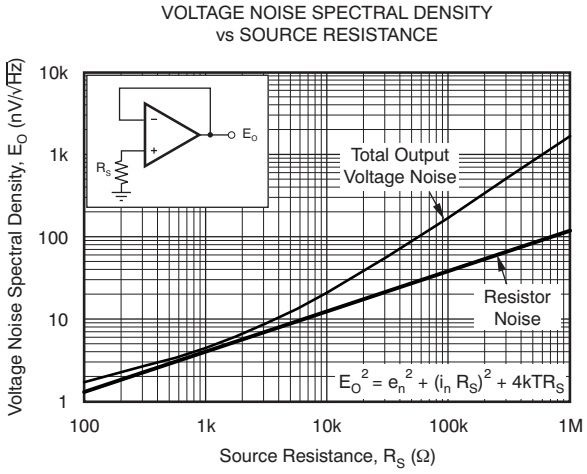


Figure 32. Noise Performance of the OPA1611 In Unity-Gain Buffer Configuration

8.2.3 Basic Noise Calculations

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

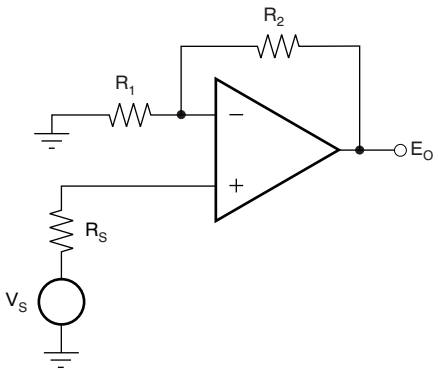
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 32 plots this function. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Noise Performance (continued)

Figure 33 shows both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise.

The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

Noise in Noninverting Gain Configuration



Noise at the output:

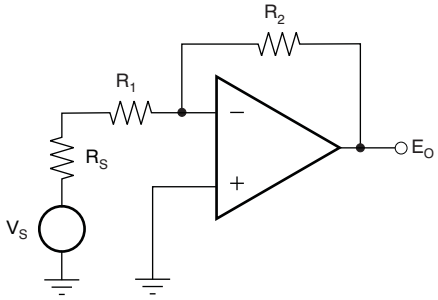
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA161x series op amps at 1 kHz, e_n = 1.1 nV/$\sqrt{Hz}$ and i_n = 1.7 pA/$\sqrt{Hz}$.

Figure 33. Noise Calculation in Gain Configurations

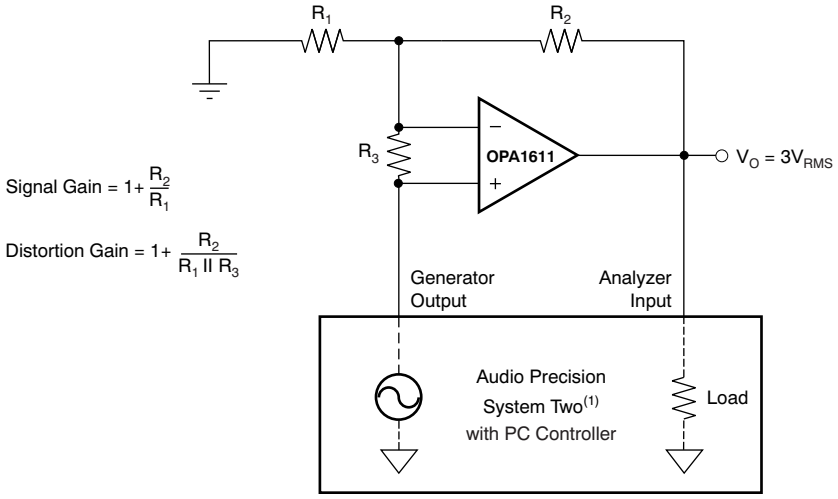
8.3 Total Harmonic Distortion Measurements

The OPA161x series op amps have excellent distortion characteristics. THD + noise is below 0.00008% (G = +1, V_O = 3 V_{RMS}, BW = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see Figure 7 for characteristic performance).

The distortion produced by OPA1611 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 34 shows) can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 34 shows a circuit that causes the op amp distortion to be 101 times (or approximately 40 dB) greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. Keep the value of R_3 small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an audio precision system two distortion and noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
–1	101	4.99kΩ	4.99kΩ	49.9Ω
+10	110	549Ω	4.99kΩ	49.9Ω

(1) For measurement bandwidth, see Figure 7 through Figure 12.

Figure 34. Distortion Test Circuit

8.4 Capacitive Loads

The dynamic characteristics of the OPA1611 and OPA1612 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 19 and Figure 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. Also, refer to Applications Bulletin AB-028, *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from the TI web site, for details of analysis techniques and application circuits.

8.5 Application Circuit

Figure 35 shows how to use the OPA1611 as an amplifier for professional audio headphones. The circuit shows the left side stereo channel. An identical circuit is used to drive the right side stereo channel.

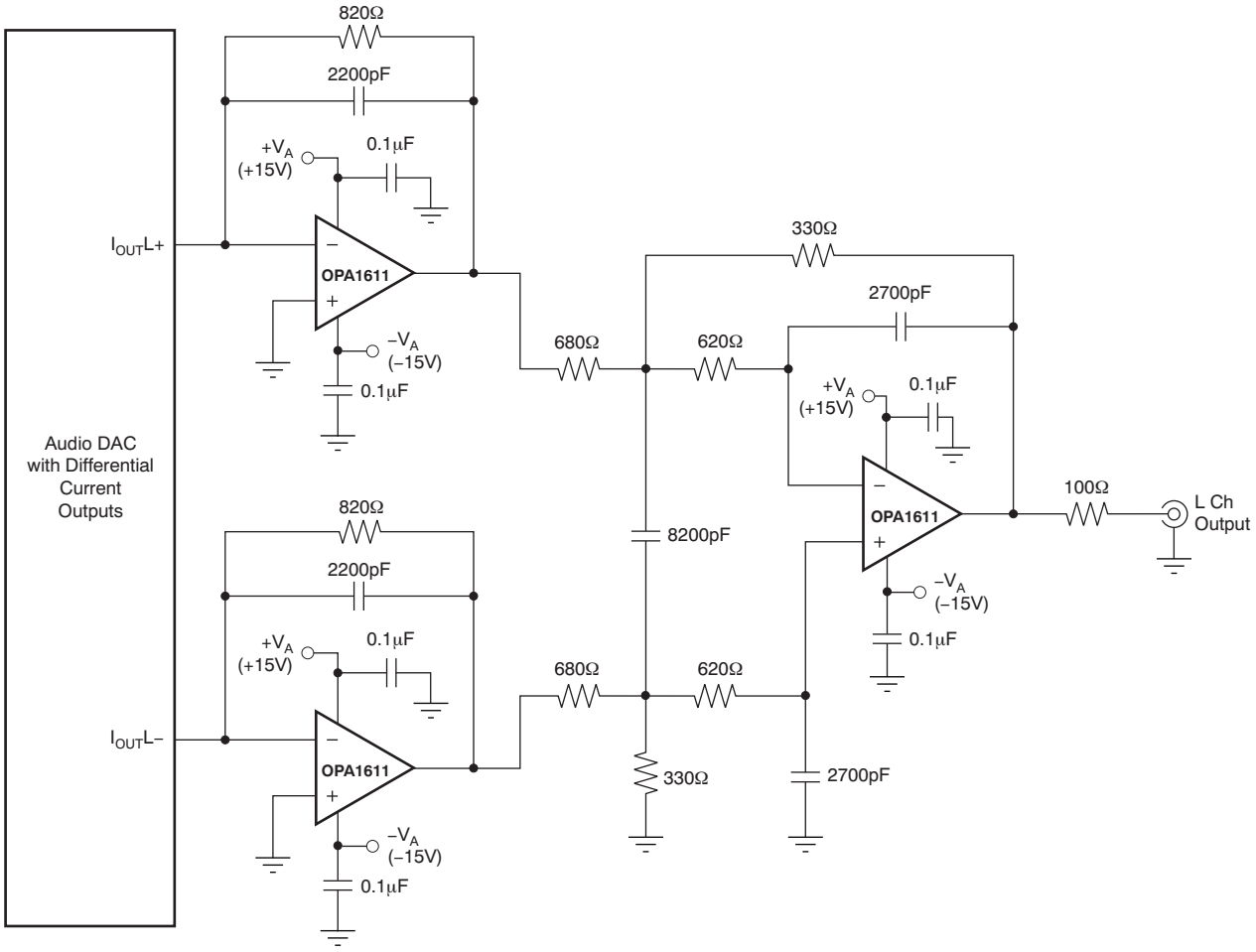


Figure 35. Audio DAC Post Filter (I/V Converter and Low-Pass Filter)

9 Power-Supply Recommendations

The OPA161x is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Typical Characteristics* section.

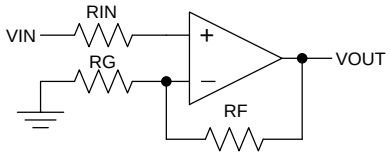
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds while paying attention to the flow of the ground current. For more detailed information, refer to the application report *Circuit Board Layout Techniques* (SLOA089).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be keep them separate, crossing the sensitive trace perpendicular as opposed to in parallel with the noisy trace is the preferred method.
- Place the external components as close to the device as possible. As shown in Figure 36, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



(Schematic Representation)

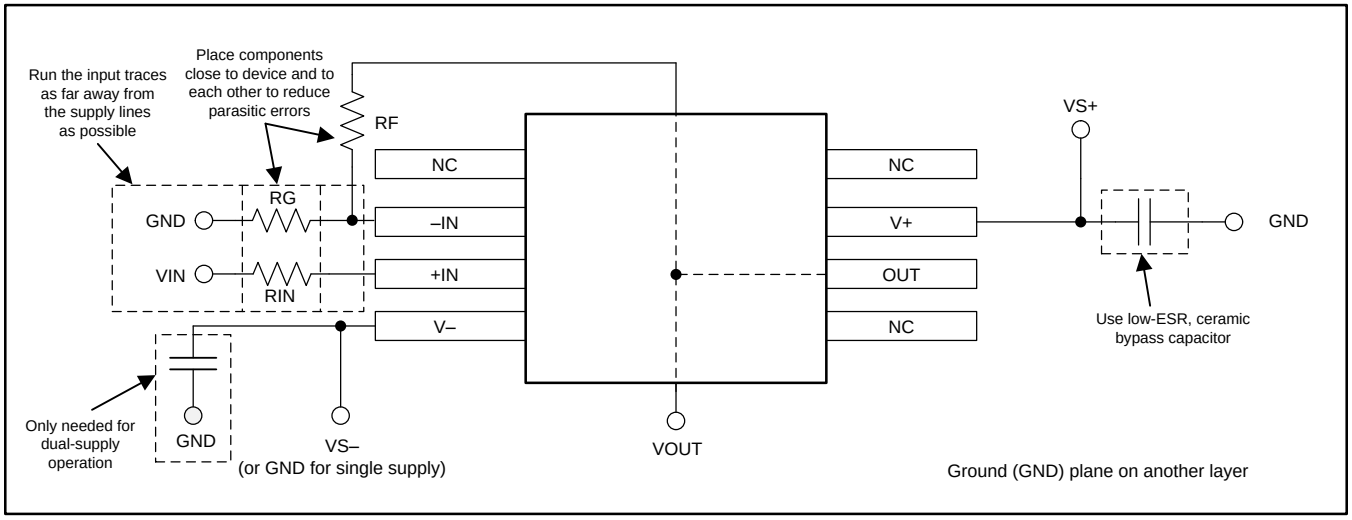


Figure 36. Operational Amplifier Board Layout for a Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Feedback Plots Define Op Amp AC Performance* , SBOA015
- *Circuit Board Layout Techniques*, SLOA089

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA1611	Click here	Click here	Click here	Click here	Click here
OPA1612	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

SoundPlus is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1611AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 1611A	Samples
OPA1611AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 1611A	Samples
OPA1612AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 1612A	Samples
OPA1612AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 1612A	Samples
OPA1612AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OVII	Samples
OPA1612AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OVII	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

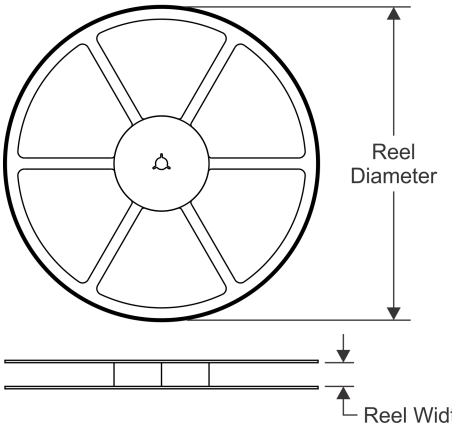
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

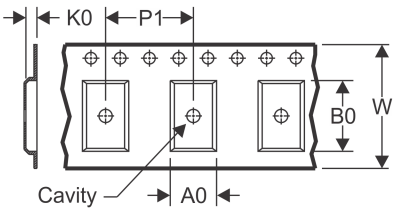
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

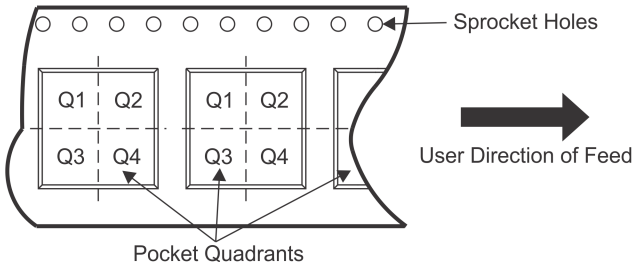


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

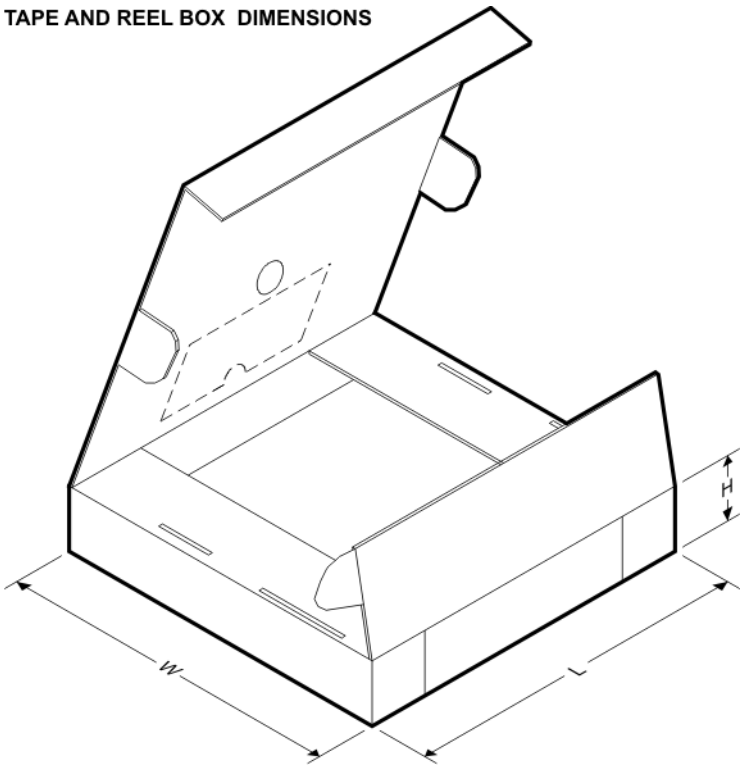
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1611AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1612AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1612AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1612AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

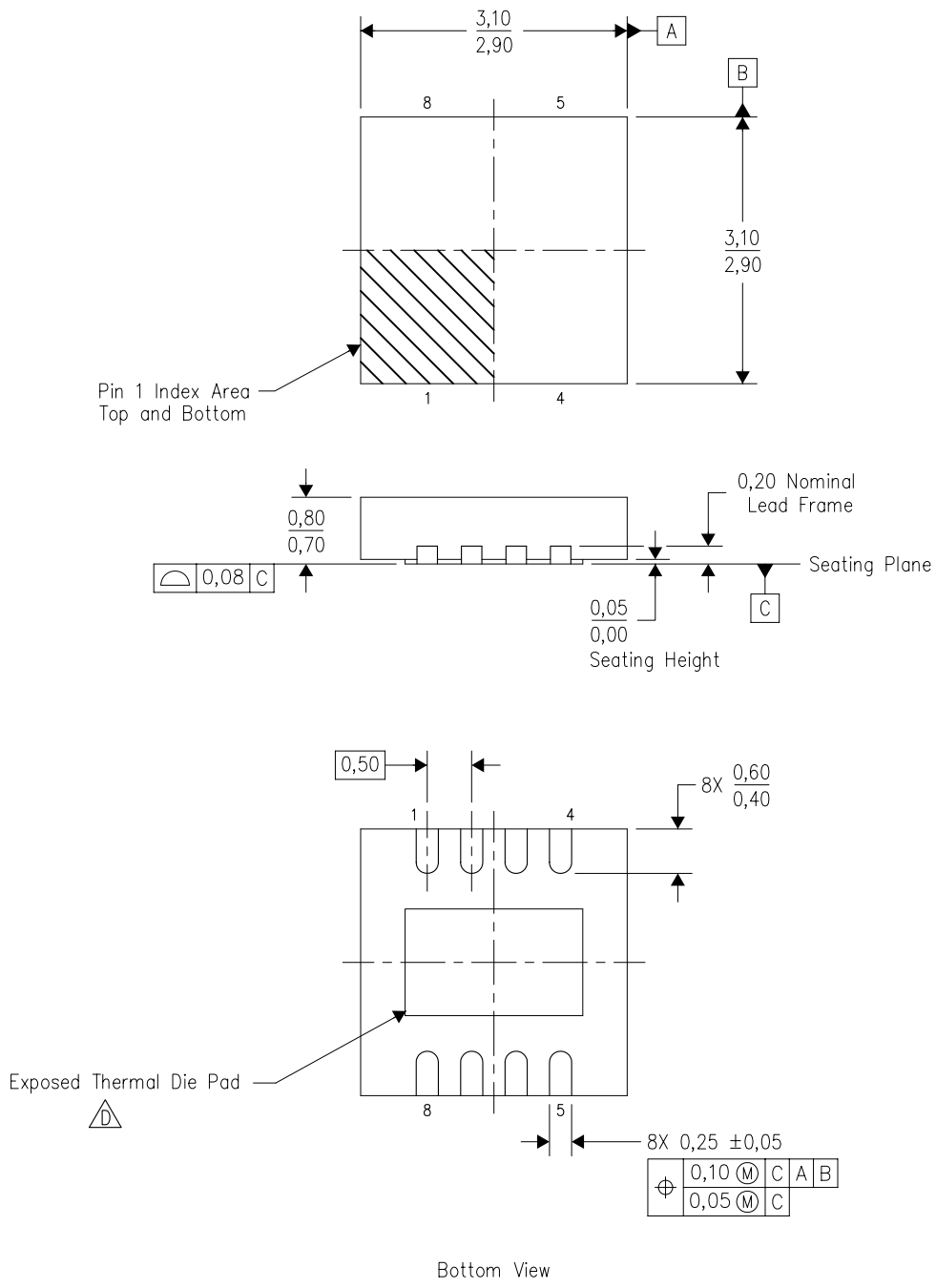
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1611AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA1612AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA1612AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA1612AIDRGT	SON	DRG	8	250	210.0	185.0	35.0

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

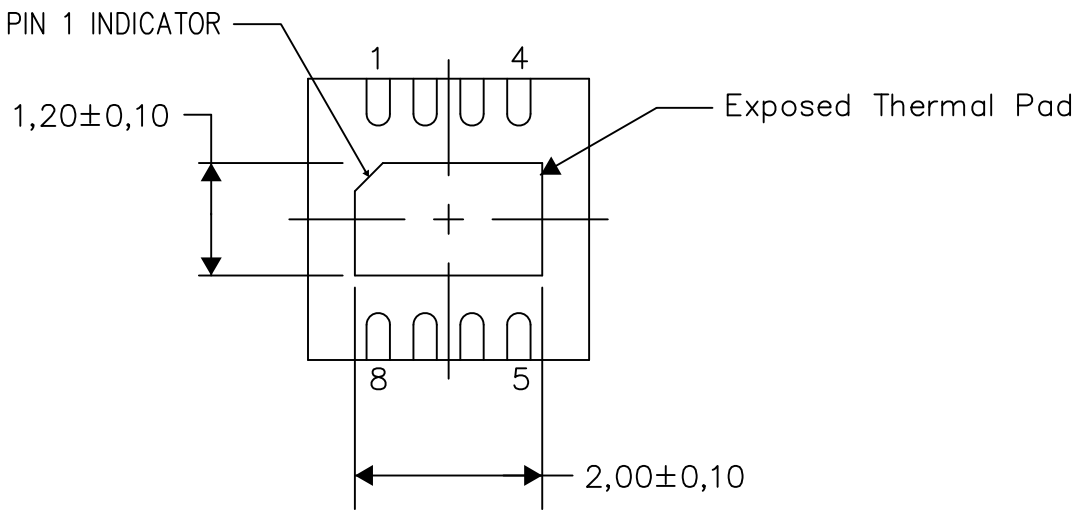
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



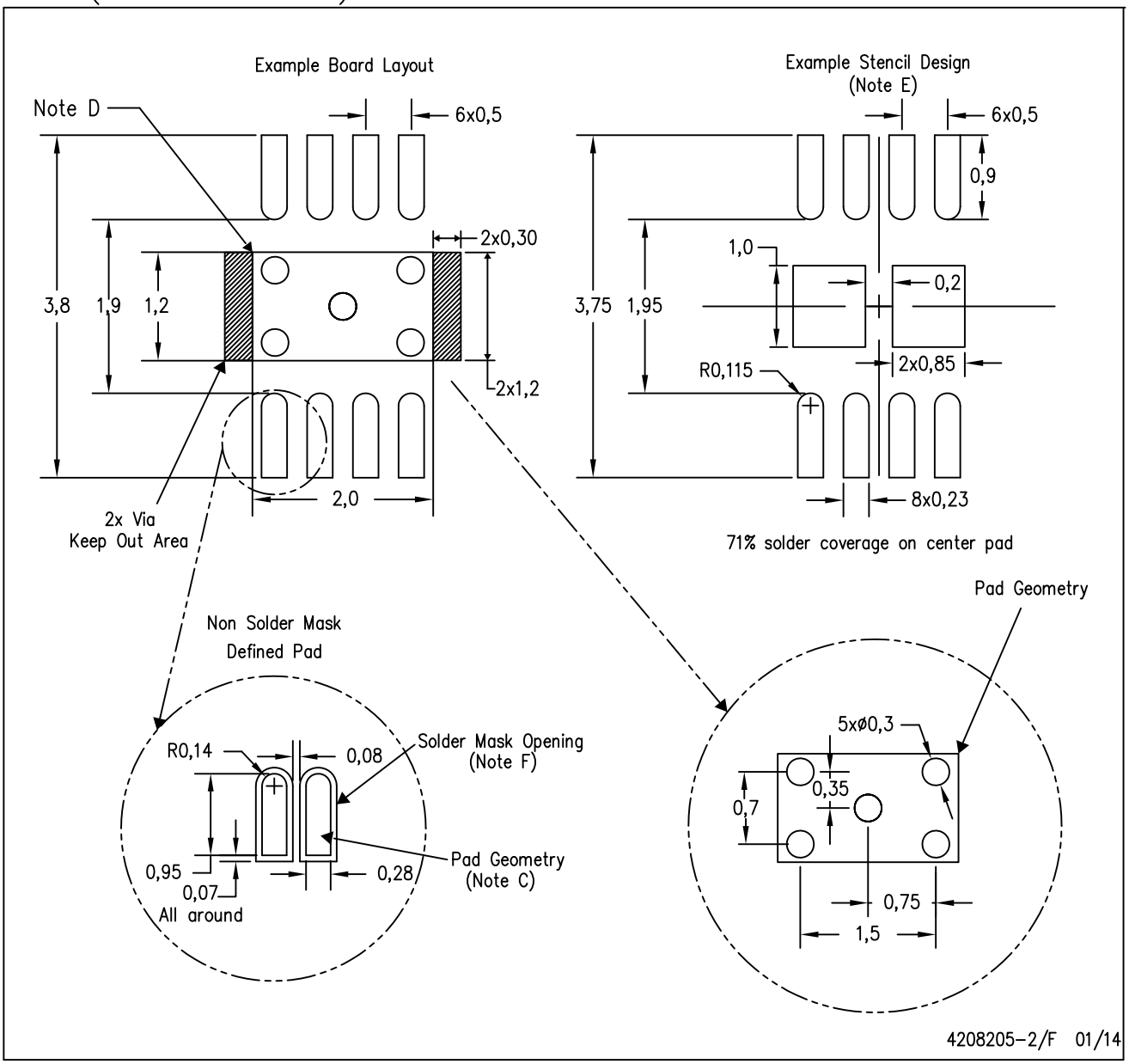
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/H 12/13

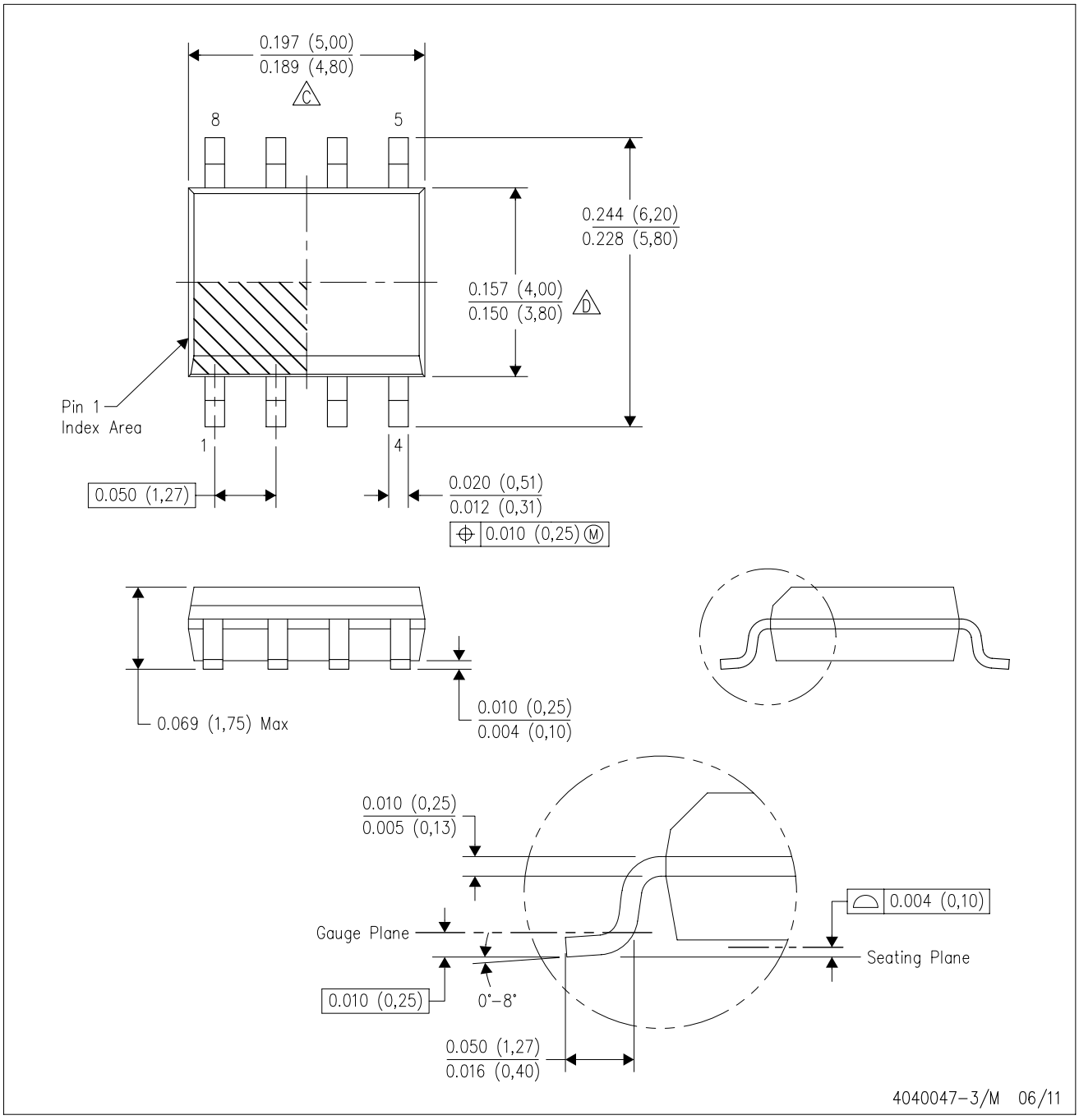
NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



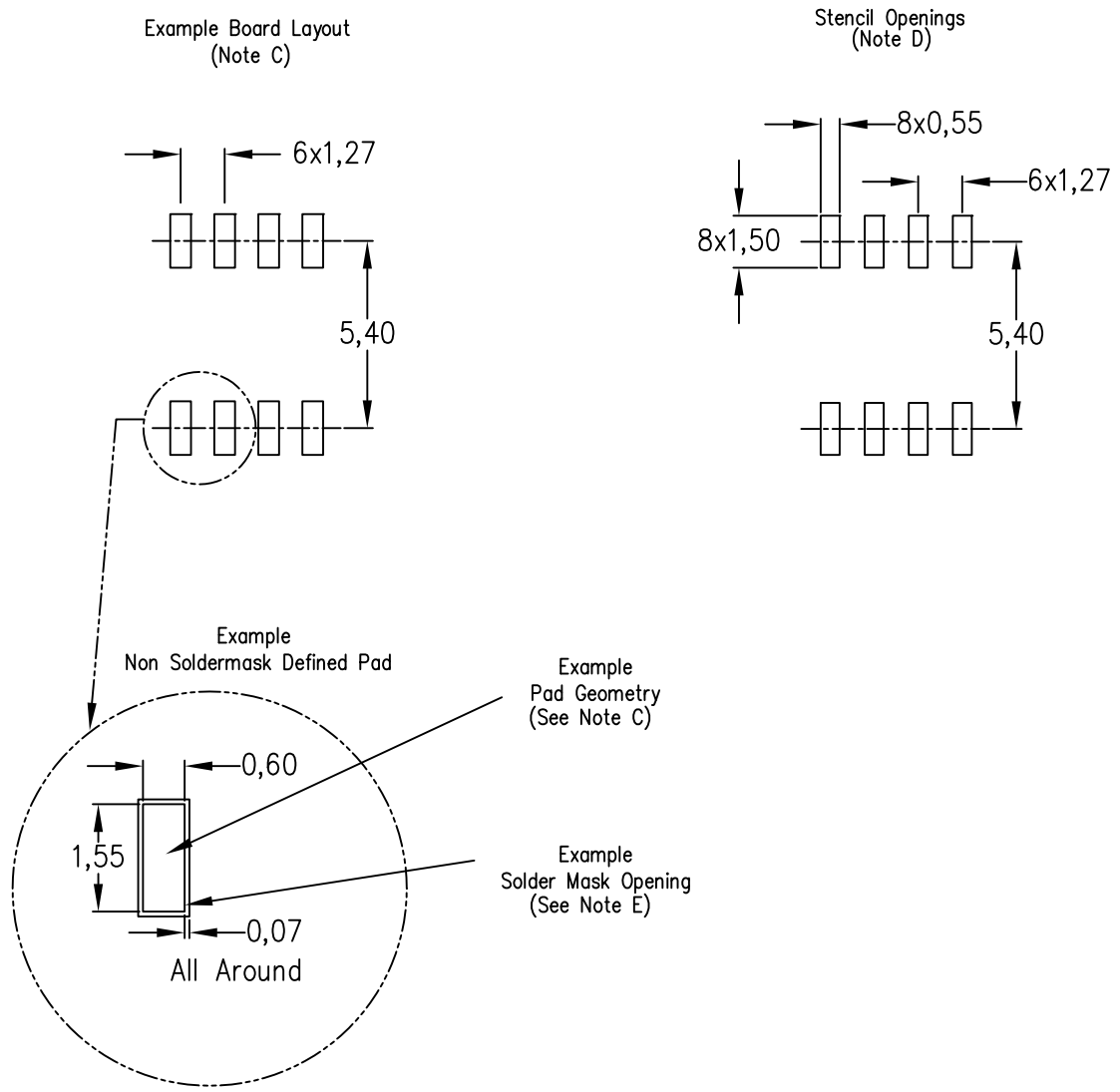
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TEXAS INSTRUMENTS

OPA209, OPA2209, OPA4209

SBOS426D – NOVEMBER 2008 – REVISED OCTOBER 2016

OPAx209 2.2-nV/√Hz, Low-Power, 36-V Operational Amplifier

1 Features

- Low Voltage Noise: 2.2 nV/√Hz at 1 kHz
- 0.1-Hz to 10-Hz Noise: 130 nV_{PP}
- Low Quiescent Current: 2.5 mA/Ch (Maximum)
- Low Offset Voltage: 150 µV (Maximum)
- Gain Bandwidth Product: 18 MHz
- Slew Rate: 6.4 V/µs
- Wide Supply Range:
  ±2.25 V to ±18 V, 4.5 V to 36 V
- Rail-to-Rail Output
- Short-Circuit Current: ±65 mA
- Available in 5-Pin SOT-23, 8-Pin MSOP, 8-Pin SOIC, and 14-Pin TSSOP Packages

2 Applications

- PLL Loop Filters
- Low-Noise, Low-Power Signal Processing
- Low-Noise Instrumentation Amplifiers
- High-Performance ADC Drivers
- High-Performance DAC Output Amplifiers
- Active Filters
- Ultrasound Amplifiers
- Professional Audio Preamplifiers
- Low-Noise Frequency Synthesizers
- Infrared Detector Amplifiers
- Hydrophone Amplifiers

3 Description

The OPA209 series of precision operational amplifiers achieve very low voltage noise density (2.2 nV/√Hz) with a supply current of only 2.5 mA (maximum). This series also offers rail-to-rail output swing, which helps to maximize dynamic range.

In precision data acquisition applications, the OPA209 provides fast settling time to 16-bit accuracy, even for 10-V output swings. This excellent ac performance, combined with only 150 µV (maximum) of offset and low drift over temperature, makes the OPA209 very suitable for fast, high-precision applications.

The OPA209 is specified over a wide dual power-supply range of ±2.25 V to ±18 V, or single-supply operation from 4.5 V to 36 V.

The OPA209 is available in the 5-pin SOT-23, 8-pin VSSOP, and the standard 8-pin SOIC packages. The dual OPA2209 comes in both 8-pin VSSOP and 8-pin SOIC packages. The quad OPA4209 is available in the 14-pin TSSOP package.

The OPA209 series is specified from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA209	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA2209	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA4209	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

0.1-Hz to 10-Hz Noise

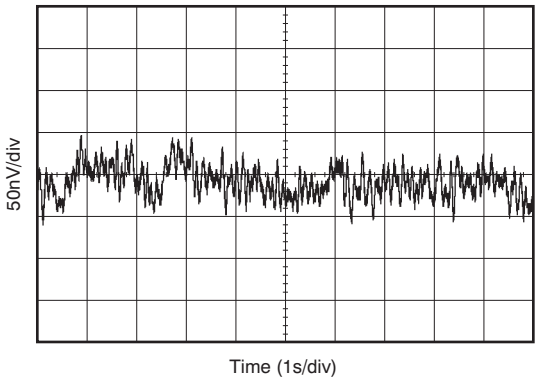


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2013) to Revision D **Page**

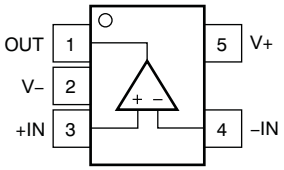
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Moved specified voltage, specified temperature, and operating temperature from *Electrical Characteristics* to *Recommended Operating Conditions* ... 5
- Updated values in the *Thermal Information* tables to align with JEDEC standards ... 5

Changes from Revision B (August 2010) to Revision C **Page**

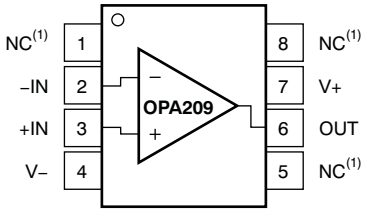
- Deleted device graphic ... 1
- Changed y-axis units label in Figure 2 ... 8

5 Pin Configuration and Functions

OPA209: DBV Package
5-Pin SOT-23
Top View



OPA209: D or DGK Packages
8-Pin SOIC or VSSOP
Top View

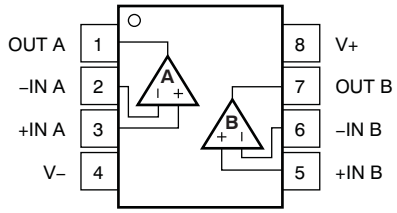


(1) NC = no internal connection

Pin Functions: OPA209

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC, VSSOP		
–IN	4	2	I	Inverting input
+IN	3	3	I	Noninverting input
NC	—	1, 5, 8	—	No internal connection
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) power supply
V+	5	7	—	Positive (highest) power supply

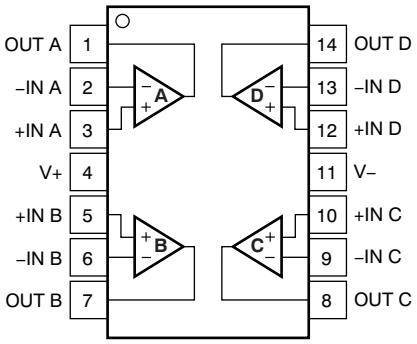
OPA2209: D or DGK Packages
8-Pin SOIC or VSSOP
Top View



Pin Functions: OPA2209

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4209: PW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4209

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		40	V
	Signal input pins(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input pins(2)	–10	10	mA
	Output short circuit(3)	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		200	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For input voltages beyond the power-supply rails, voltage or current must be limited.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Specified voltage	±2.25	±18	V
	Specified temperature	–40	125	°C
T_A	Operating temperature	–55	150	°C

6.4 Thermal Information: OPA209

THERMAL METRIC(1)		OPA209			UNIT
		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.9	135.5	142.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	200	73.7	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	113.1	61.9	63.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.2	19.7	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	104.9	54.8	62.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2209

THERMAL METRIC(1)		OPA2209		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.1	38.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.7	52.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	52.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4209

THERMAL METRIC(1)		OPA4209	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at V_S = ±2.25 V to ±18 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±15 V, V_{CM} = 0 V			±35	±150	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			1	3	µV/°C
PSRR	vs power supply	V_S = ±2.25 V to ±18 V	T_A = 25°C		0.05	0.5	µV/V
			T_A = –40°C to 125°C			1	
	Channel separation	DC (dual and quad versions)			1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		±1	±4.5	nA
			T_A = –40°C to 85°C			±8	
			T_A = –40°C to 125°C			±15	
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		±0.7	±4.5	nA
			T_A = –40°C to 85°C			±8	
			T_A = –40°C to 125°C			±15	
NOISE							
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz			0.13		μV_{PP}
	Noise density	f = 10 Hz			3.3		nV/√Hz
		f = 100 Hz			2.25		
		f = 1 kHz			2.2		
I_n	Input current noise density	f = 1 kHz			500		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 1.5		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to 125°C		120	130		dB

Electrical Characteristics (continued)

at V_S = ±2.25 V to ±18 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
	Differential				200 || 4		kΩ || pF
	Common-mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	T_A = 25°C	126	132		dB
			T_A = –40°C to 125°C	120			
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 600 Ω(1)	T_A = 25°C	114	120		
			T_A = –40°C to 125°C	110			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				18		MHz
SR	Slew rate				6.4		V/µs
Φm	Phase margin	R_L = 10 kΩ, C_L = 25 pF			80		°
t_S	Settling time	0.1%, G = –1, 10-V step, C_L = 100 pF			2.1		µs
		0.0015% (16-bit), G = –1, 10-V step, C_L = 100 pF			2.6		
	Overload recovery time	G = –1			< 1		µs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 20 V_{PP}, 600 Ω			0.000025%		
OUTPUT							
	Voltage output swing	R_L = 10 kΩ, A_{OL} > 130 dB		(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} > 114 dB		(V–) + 0.6		(V+) – 0.6	
		R_L = 10 kΩ, A_{OL} > 120 dB, T_A = –40°C to 125°C		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_{LOAD}	Capacitive load drive (stable operation)			See *Typical Characteristics*			
Z_O	Open-loop output impedance			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0 A	T_A = 25°C		2.2	2.5	mA
			T_A = –40°C to 125°C			3.25	

(1) See *Absolute Maximum Ratings* for additional information.

6.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

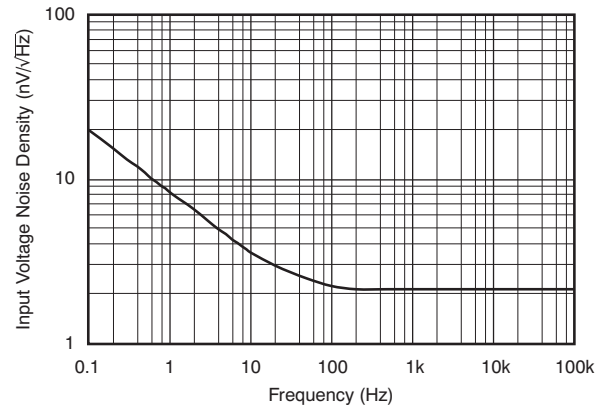


Figure 1. Input Voltage Noise Density vs Frequency

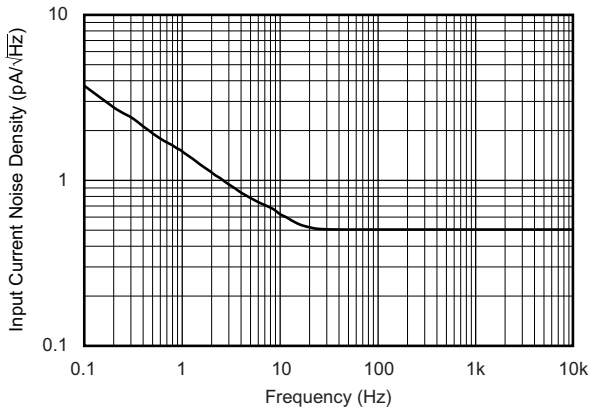


Figure 2. Input Current Noise Density vs Frequency

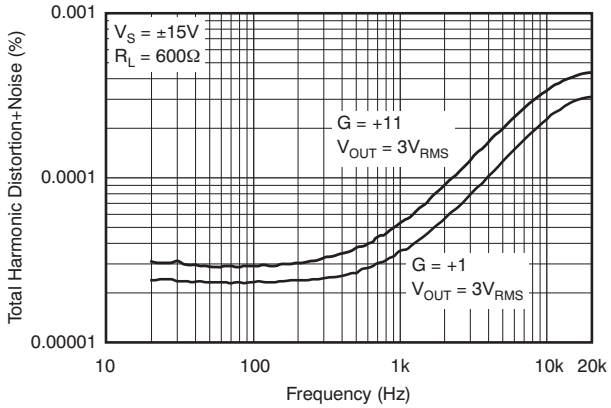


Figure 3. Total Harmonic Distortion + Noise Ratio vs Frequency

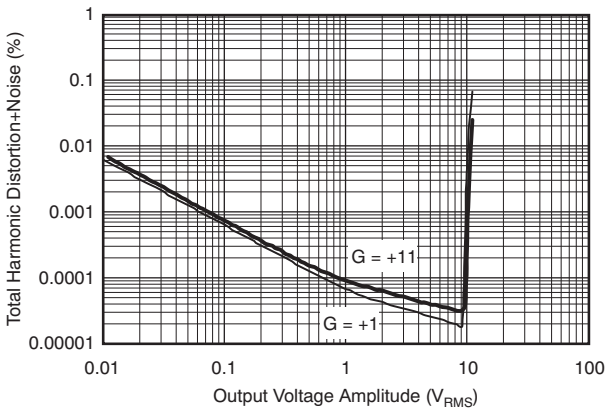


Figure 4. Total Harmonic Distortion + Noise Ratio vs Amplitude

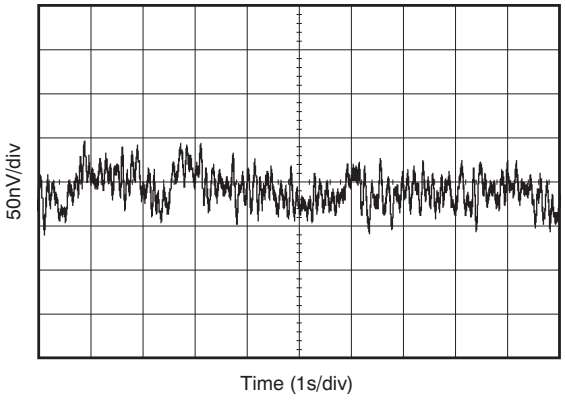


Figure 5. 0.1-Hz to 10-Hz Noise

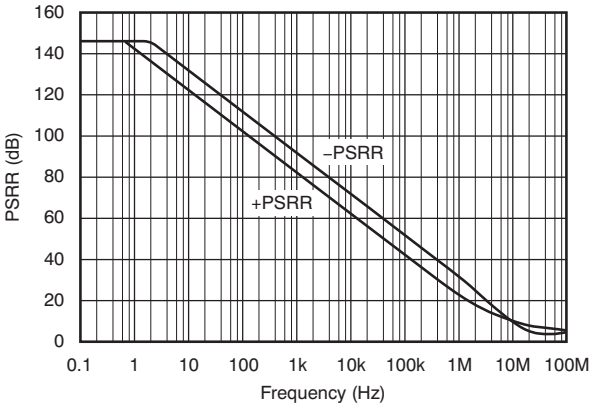


Figure 6. Power-Supply Rejection Ratio vs Frequency (Referred to Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

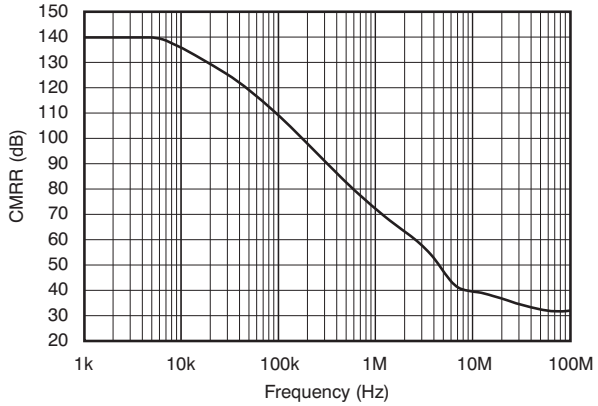


Figure 7. Common-Mode Rejection Ratio vs Frequency

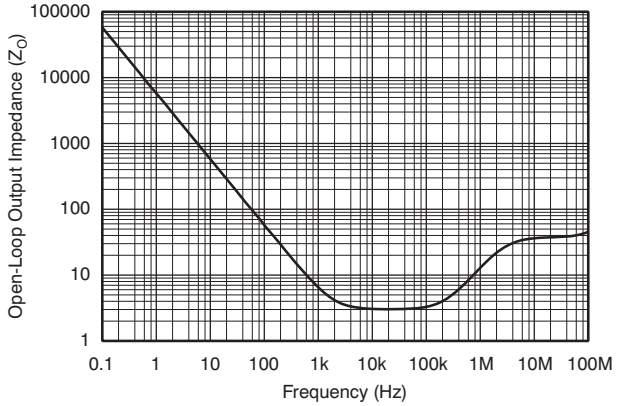


Figure 8. Open-Loop Output Impedance vs Frequency

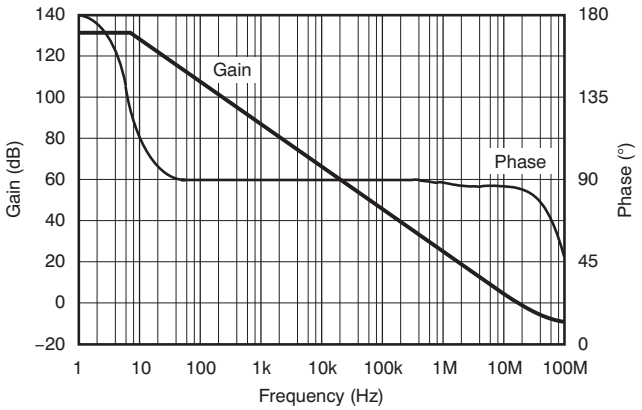


Figure 9. Open-Loop Gain and Phase vs Frequency

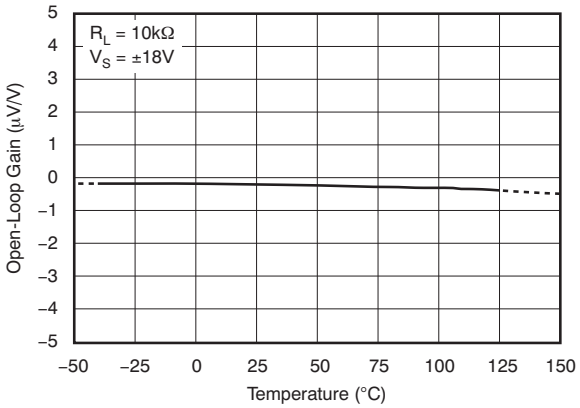


Figure 10. Open-Loop Gain vs Temperature

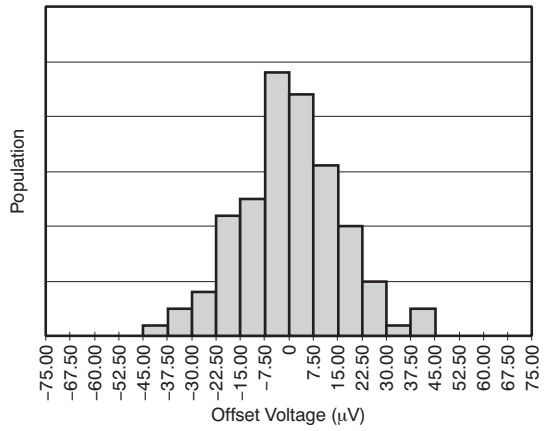


Figure 11. Offset Voltage Production Distribution

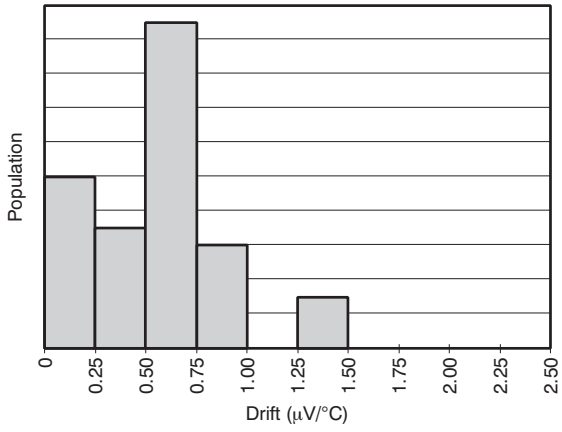


Figure 12. Offset Voltage Drift Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

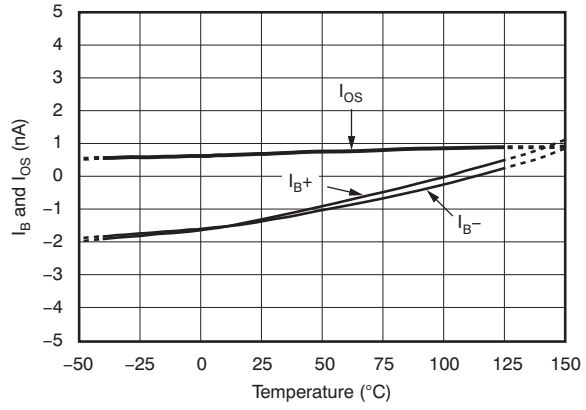


Figure 13. Input Bias and Input Offset Currents vs Temperature

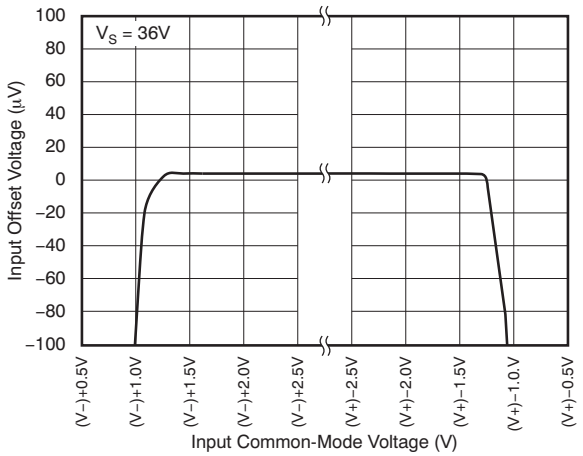


Figure 14. Input Offset Voltage vs Common-Mode Voltage

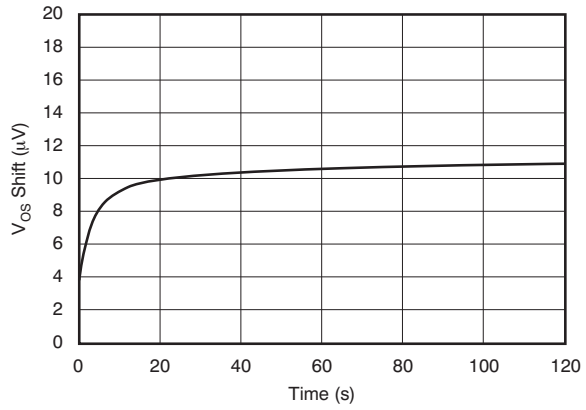


Figure 15. Input Offset Voltage vs Time

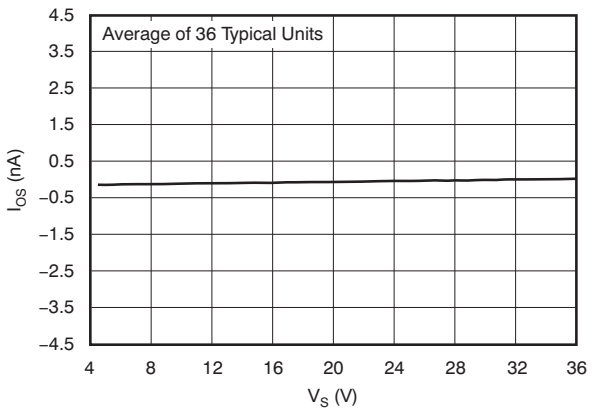


Figure 16. Input Offset Current vs Supply Voltage

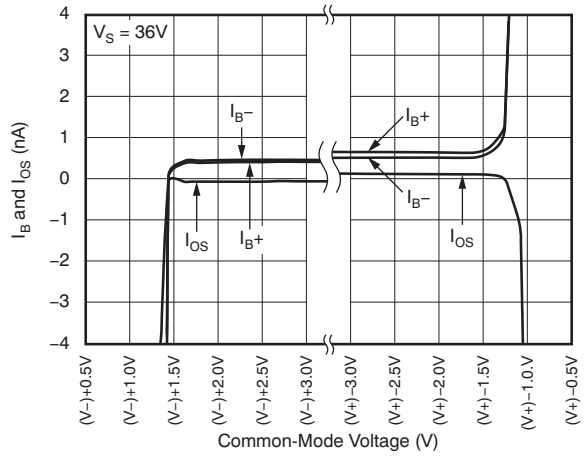


Figure 17. Input Bias and Input Offset Currents vs Common-Mode Voltage

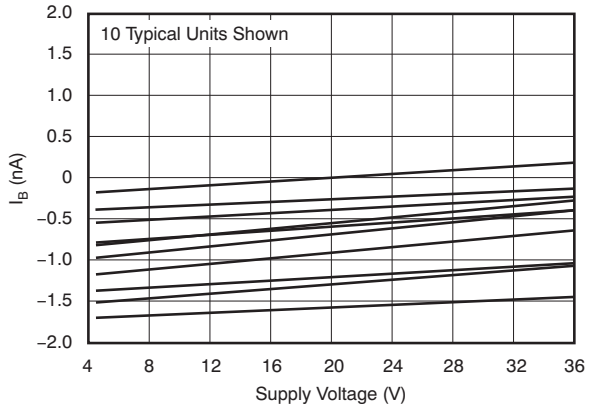


Figure 18. Input Bias Current vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

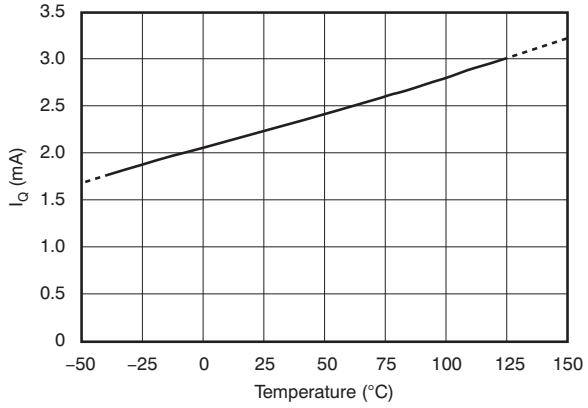


Figure 19. Quiescent Current vs Temperature

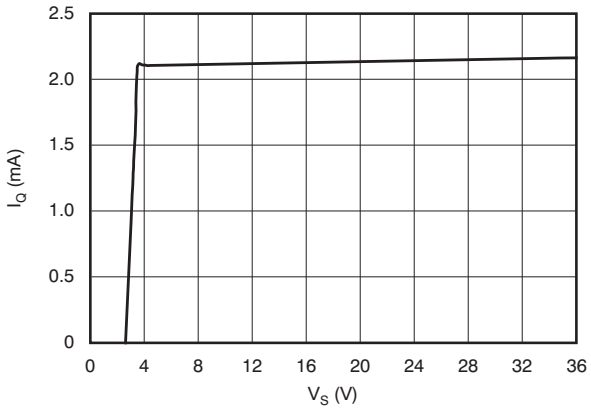


Figure 20. Quiescent Current vs Supply Voltage

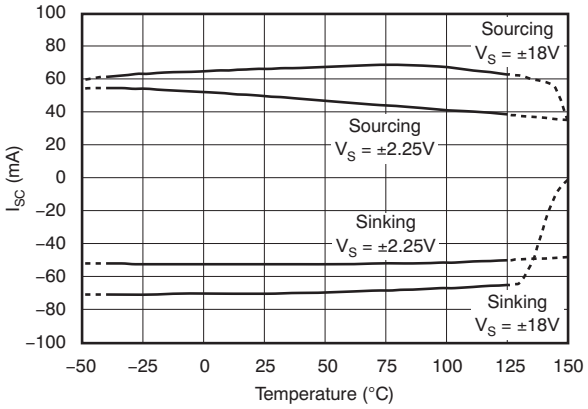


Figure 21. Short-Circuit Current vs Temperature

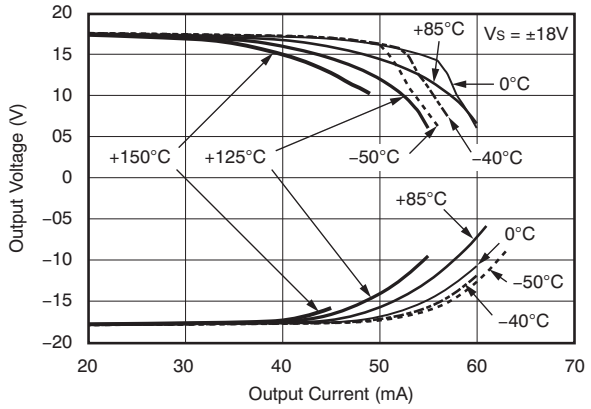


Figure 22. Output Voltage vs Output Current

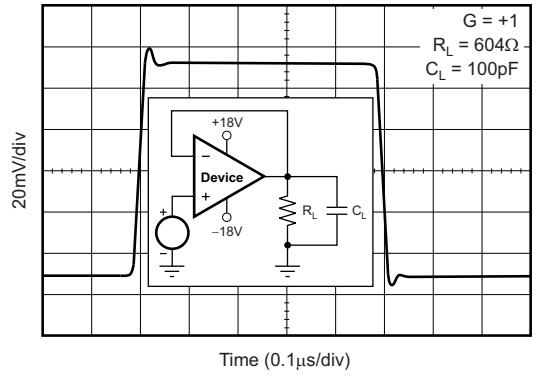


Figure 23. Small-Signal Step Response

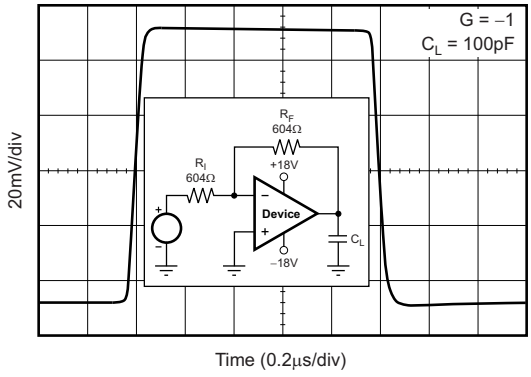


Figure 24. Small-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

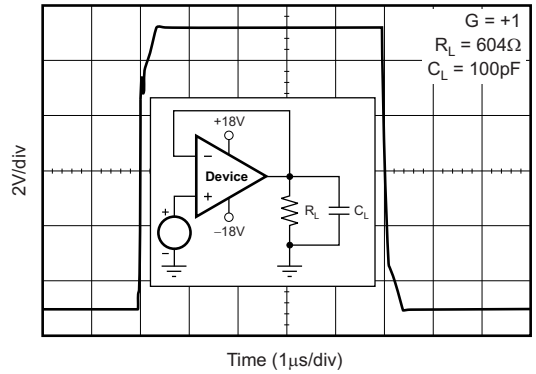


Figure 25. Large-Signal Step Response

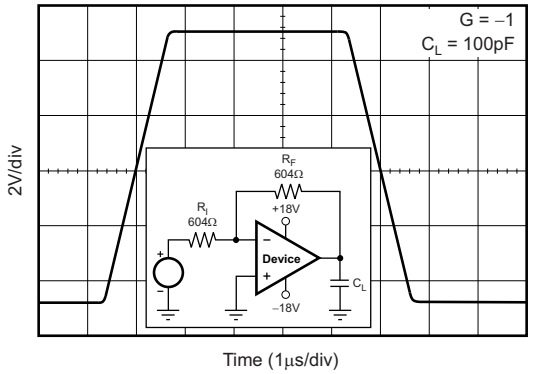


Figure 26. Large-Signal Step Response

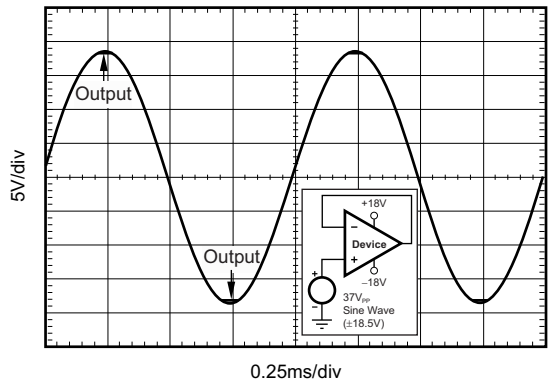


Figure 27. No Phase Reversal

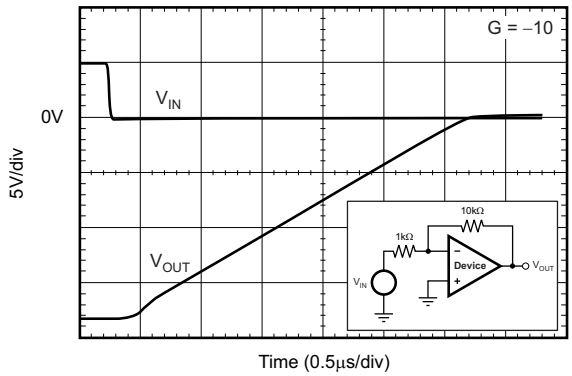


Figure 28. Negative Overload Recovery

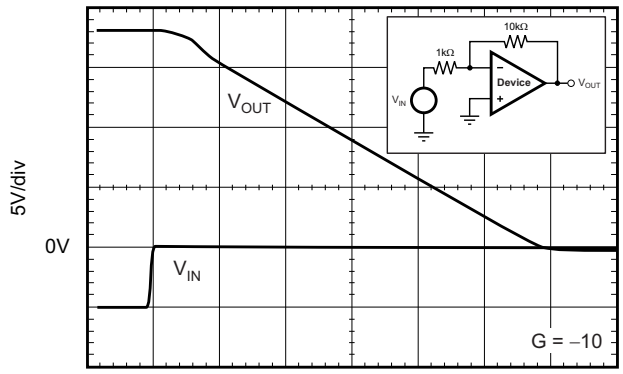


Figure 29. Positive Overvoltage Recovery

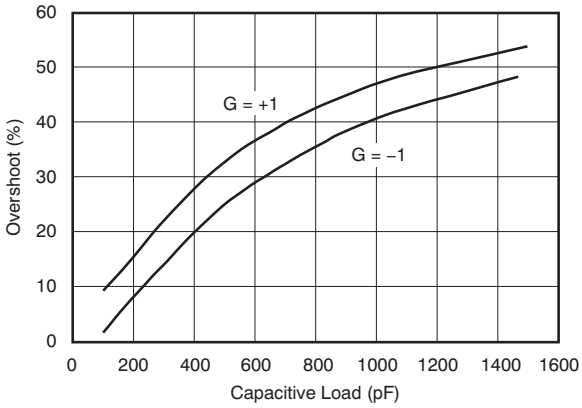


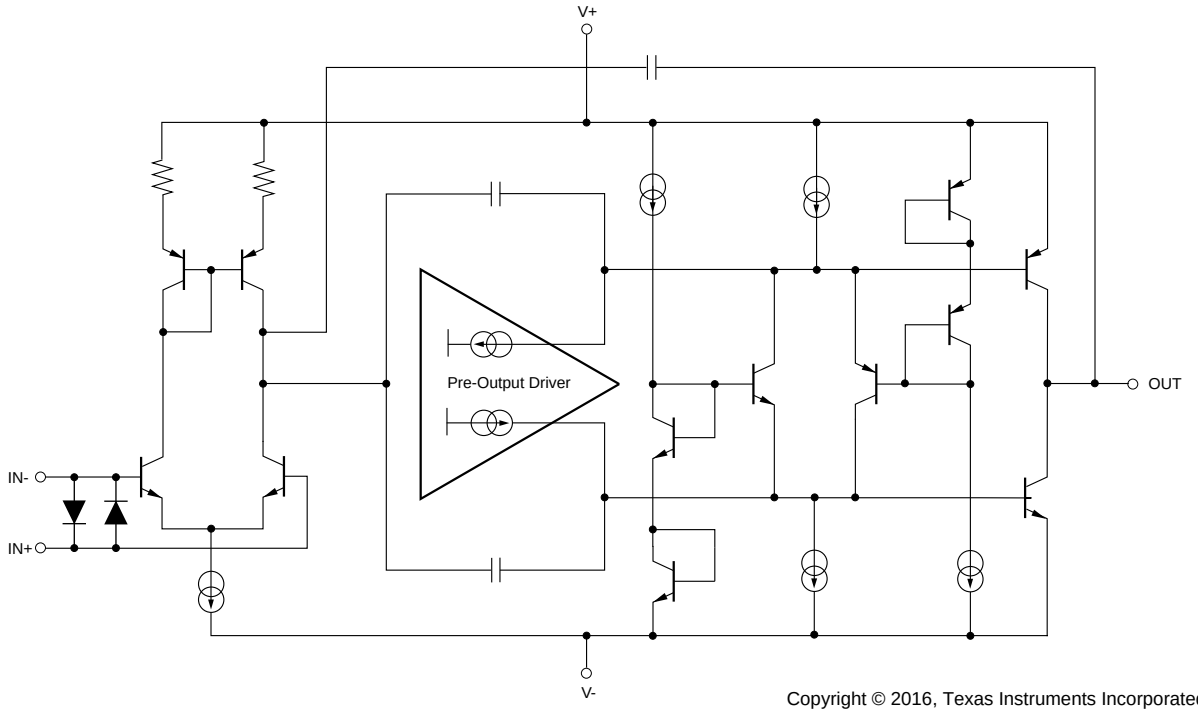
Figure 30. Small-Signal Overshoot vs Capacitive Load

7 Detailed Description

7.1 Overview

The OPA209 series of precision operational amplifiers are unity-gain stable, and free from unexpected output and phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. The *Functional Block Diagram* shows a simplified schematic of the OPA209. This die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA209 series of op amps can be used with single or dual supplies within an operating range of V_S = 4.5 V (±2.25 V) up to 36 V (±18 V). Supply voltages higher than 40 V total can permanently damage the device (see *Absolute Maximum Ratings*).

In addition, key parameters are assured over the specified temperature range, T_A = –40°C to 125°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

7.3.2 Input Protection

The input terminals of the OPA209 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 31. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 25 and Figure 26 in *Typical Characteristics*. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA209. See *Noise Performance* for further information on noise performance.

Feature Description (continued)

Figure 31 shows an example configuration that implements a current-limiting feedback resistor.

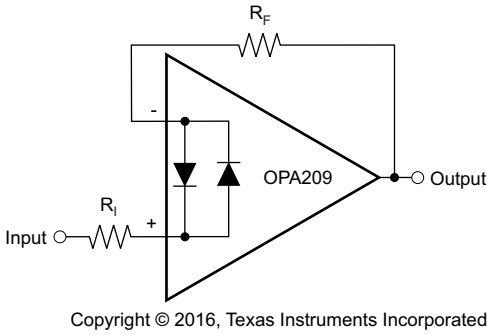


Figure 31. Pulsed Operation

7.3.3 Noise Performance

Figure 32 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with the total circuit noise calculated. The OPA209 has very low voltage noise, making it ideal for low source impedances (less than 2 kΩ). As a comparable precision FET-input op amp (very low current noise), the OPA827 has somewhat higher voltage noise, but lower current noise. It provides excellent noise performance at moderate to high source impedance (10 kΩ and up). For source impedance lower than 300 Ω, the OPA211 may provide lower noise.

The equation in Figure 32 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise,
- i_n = current noise,
- R_S = source impedance,
- k = Boltzmann's constant = 1.38×10^{-23} J/K, and
- T = temperature in Kelvins

For more details on calculating noise, see *Basic Noise Calculations*.

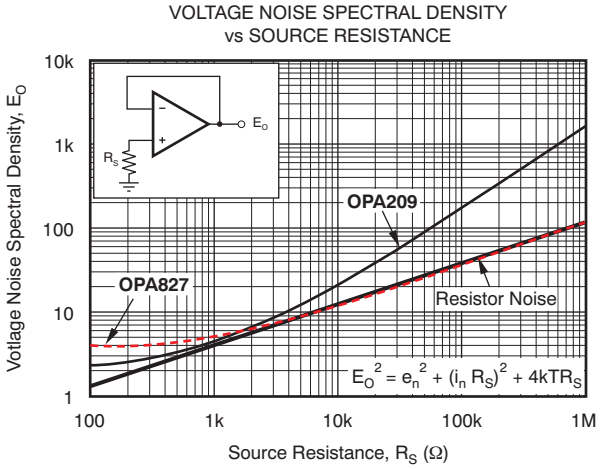


Figure 32. Noise Performance of the OPA209 and OPA827 in Unity-Gain Buffer Configuration

Feature Description (continued)

7.3.4 Basic Noise Calculations

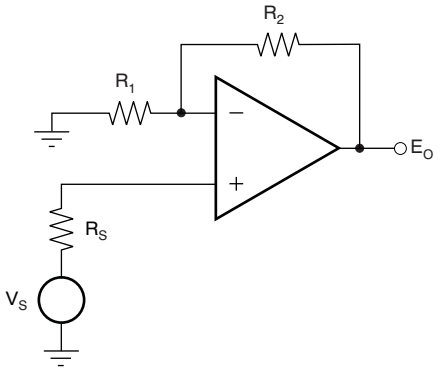
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combinations of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is illustrated in Figure 32. The source impedance is usually fixed; consequently, select the appropriate op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 33 illustrates both noninverting (Figure 33a) and inverting (Figure 33b) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low-impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

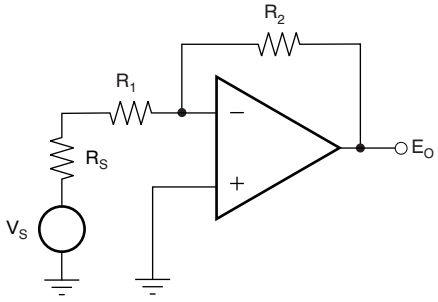
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA209 series op amps at 1 kHz, e_n = 2.2 nV/$\sqrt{Hz}$ and I_n = 530 fA/$\sqrt{Hz}$.

Figure 33. Noise Calculation in Gain Configurations

Feature Description (continued)

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See Figure 34 for an illustration of the ESD circuits contained in the OPA209 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA209 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one Figure 34 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 34 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

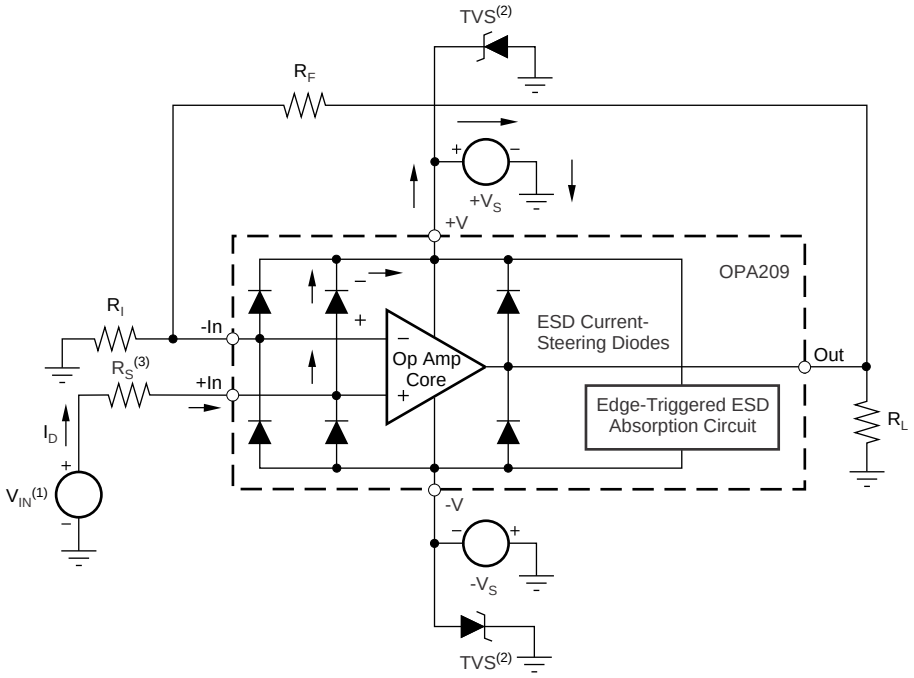
Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0 V.

Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 34. The Zener voltage must be selected such that the diode does not turn on during normal operation.

However, its Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

Feature Description (continued)



(1) $V_{IN} = +V_S + 500$ mV

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1 kΩ

Figure 34. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

7.4 Device Functional Modes

The OPAx209 is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the OPAx209 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx209 are unity-gain stable, precision operational amplifiers with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Application

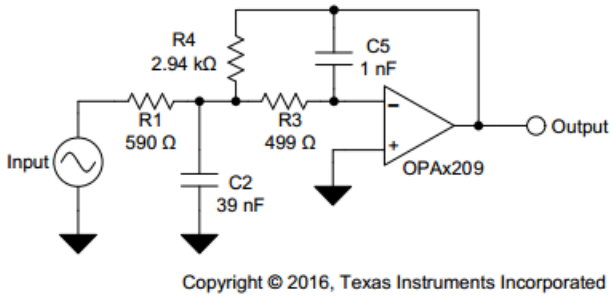


Figure 35. Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx209 are ideally suited to construct high-speed, high-precision active filters. Figure 35 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 35. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Typical Application (continued)

8.2.3 Application Curve

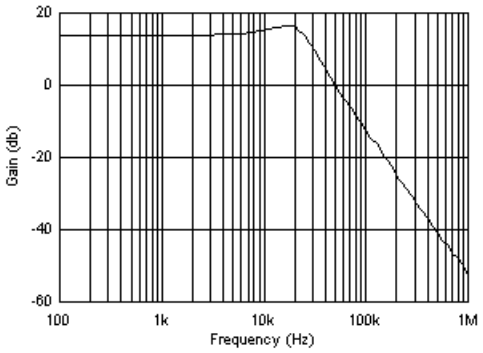


Figure 36. OPAx209 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

9 Power Supply Recommendations

The OPAx209 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

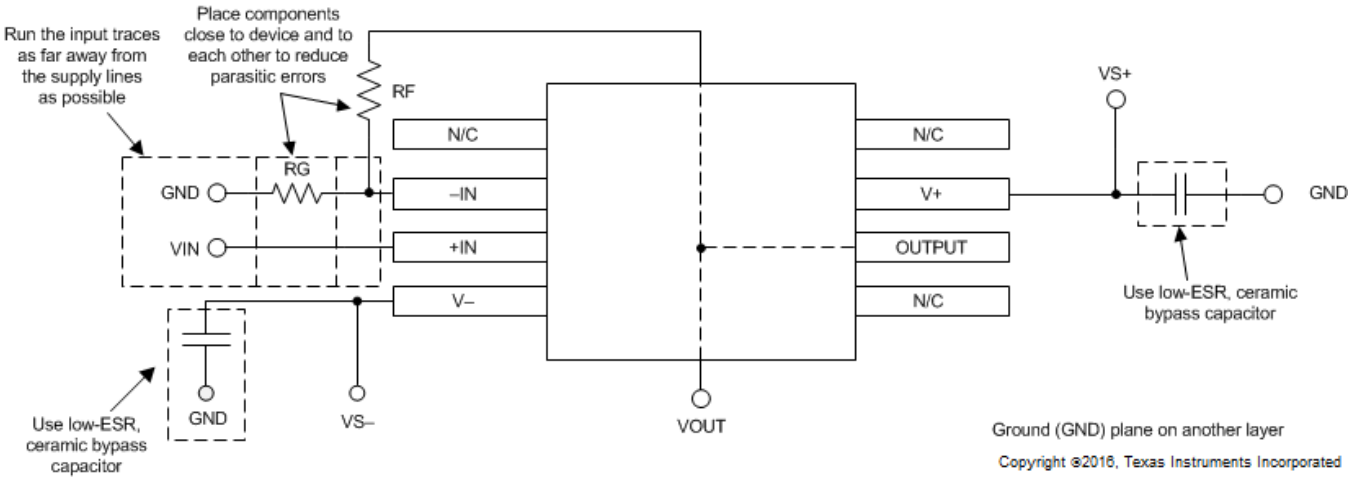


Figure 37. OPAx209 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP, and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPAx209 and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- *OPA827 Low-Noise, High-Precision, JFET-Input Operational Amplifier* (SBOS376)
- *OPA2x11 1.1-nv/√Hz Noise, Low Power, Precision Operational Amplifier* (SBOS377)
- *OPA209, OPA2209, OPA4209 EMI Immunity Performance* (SBOZ020)
- *Microcontroller PWM to 12-bit Analog Out* (TIDU027)
- *Capacitive Load Drive Solution Using an Isolation Resistor* (TIDU032)
- *Noise Measurement Post Amp* (TIDU016)
- *Diagnostic Patient Monitoring and Therapy Guide* (SLYB147)

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA209	Click here	Click here	Click here	Click here	Click here
OPA2209	Click here	Click here	Click here	Click here	Click here
OPA4209	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA209AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 209A	Samples
OPA209AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOBQ	Samples
OPA209AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOBQ	Samples
OPA209AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OOAQ	Samples
OPA209AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OOAQ	Samples
OPA209AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 209A	Samples
OPA2209AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2209	Samples
OPA2209AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOJI	Samples
OPA2209AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOJI	Samples
OPA2209AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2209	Samples
OPA4209AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(OP4209A ~ OPA) 4209	Samples
OPA4209AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(OP4209A ~ OPA) 4209	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

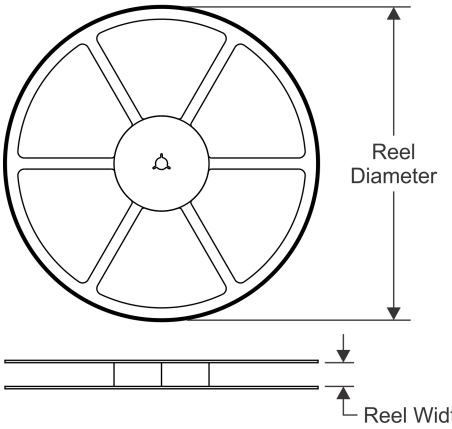
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

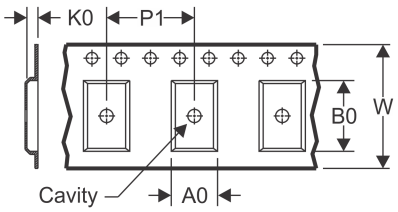
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

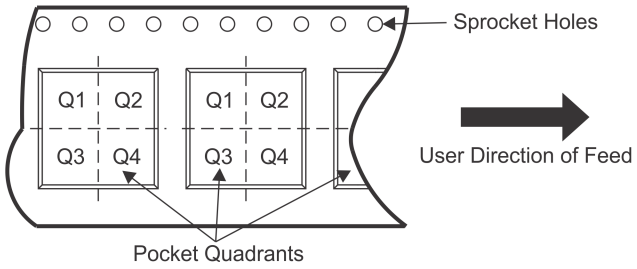


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

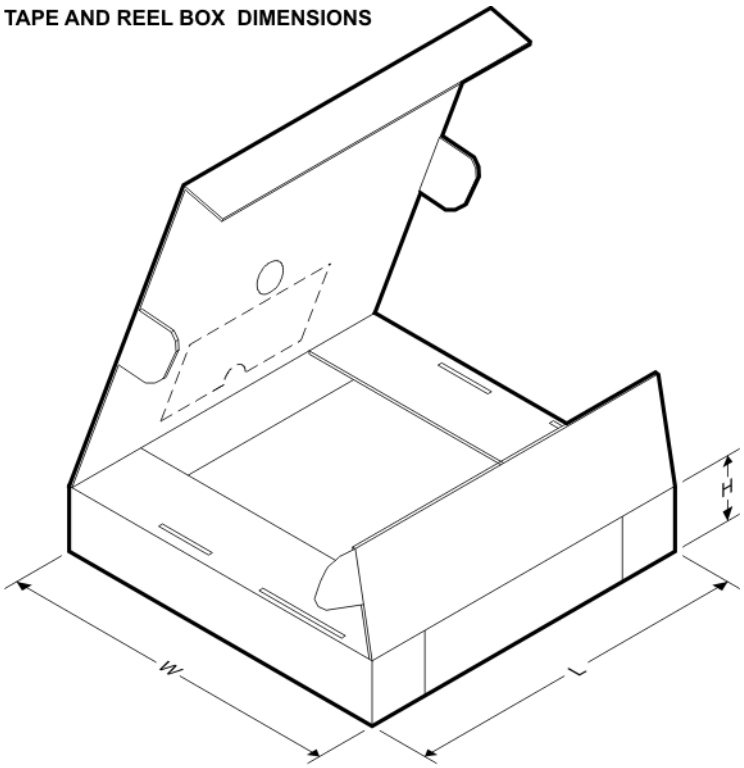
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA209AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA209AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA209AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA209AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA209AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2209AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2209AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2209AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4209AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

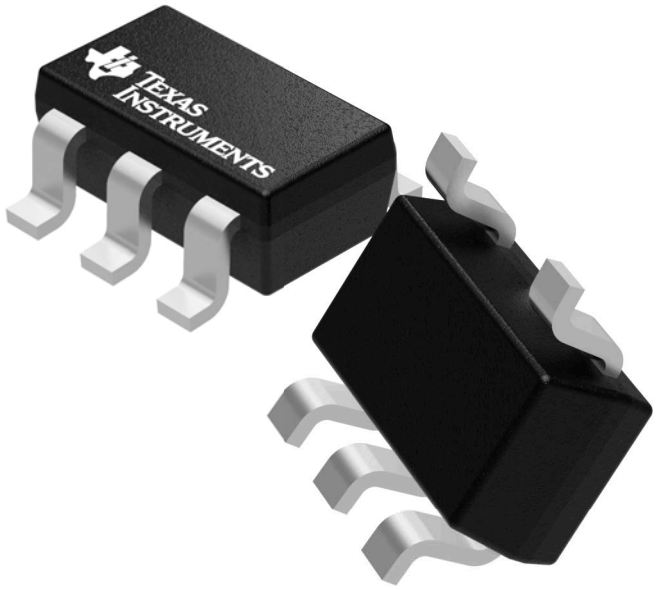


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA209AIDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA209AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA209AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA209AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA209AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2209AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2209AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2209AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4209AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



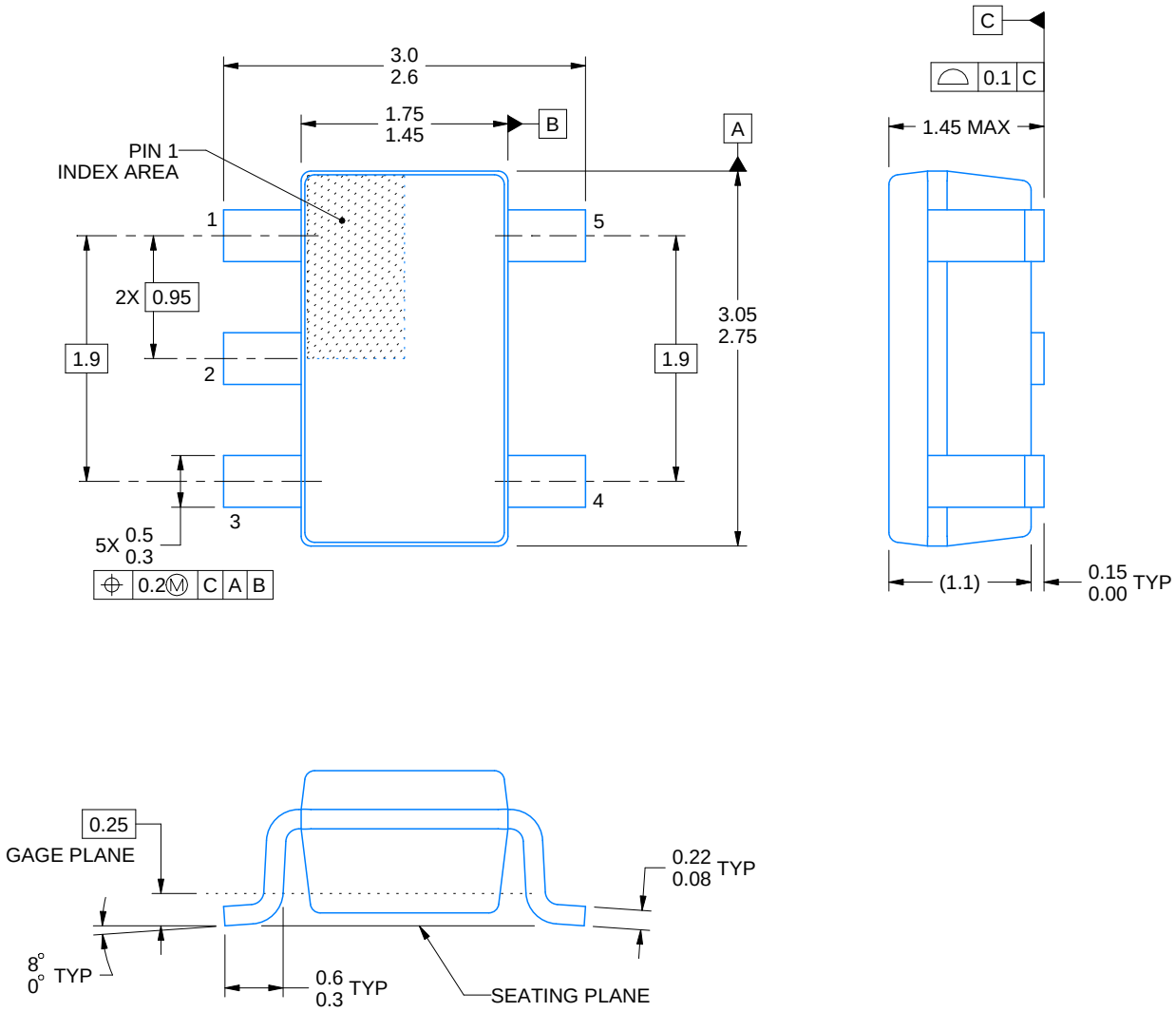
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

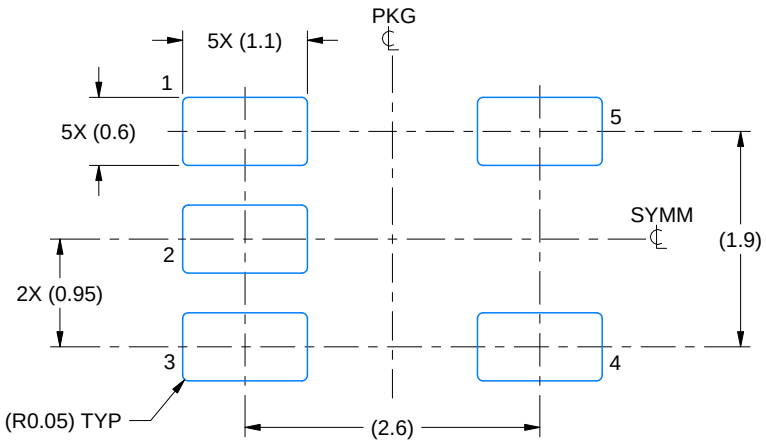
SMALL OUTLINE TRANSISTOR



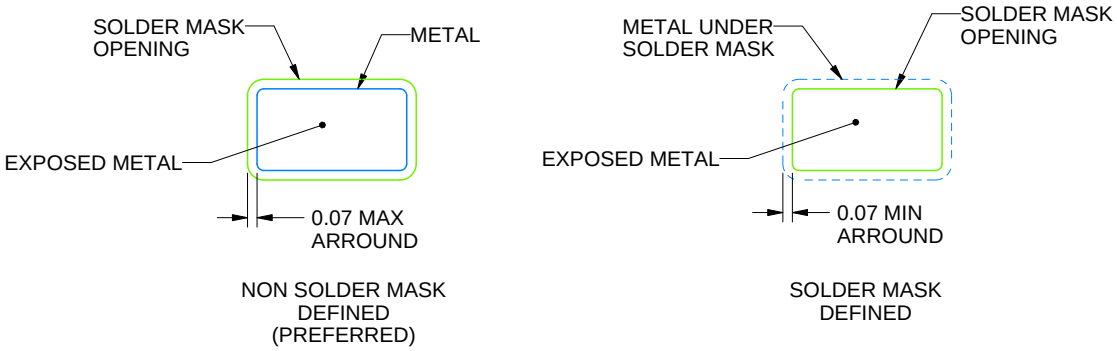
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

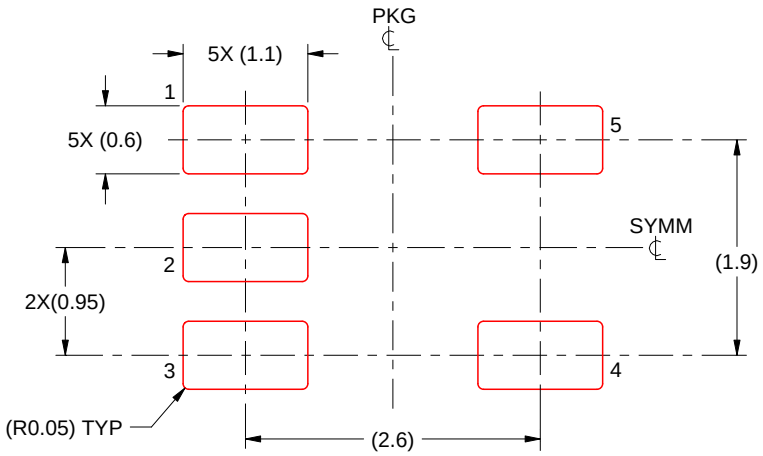


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

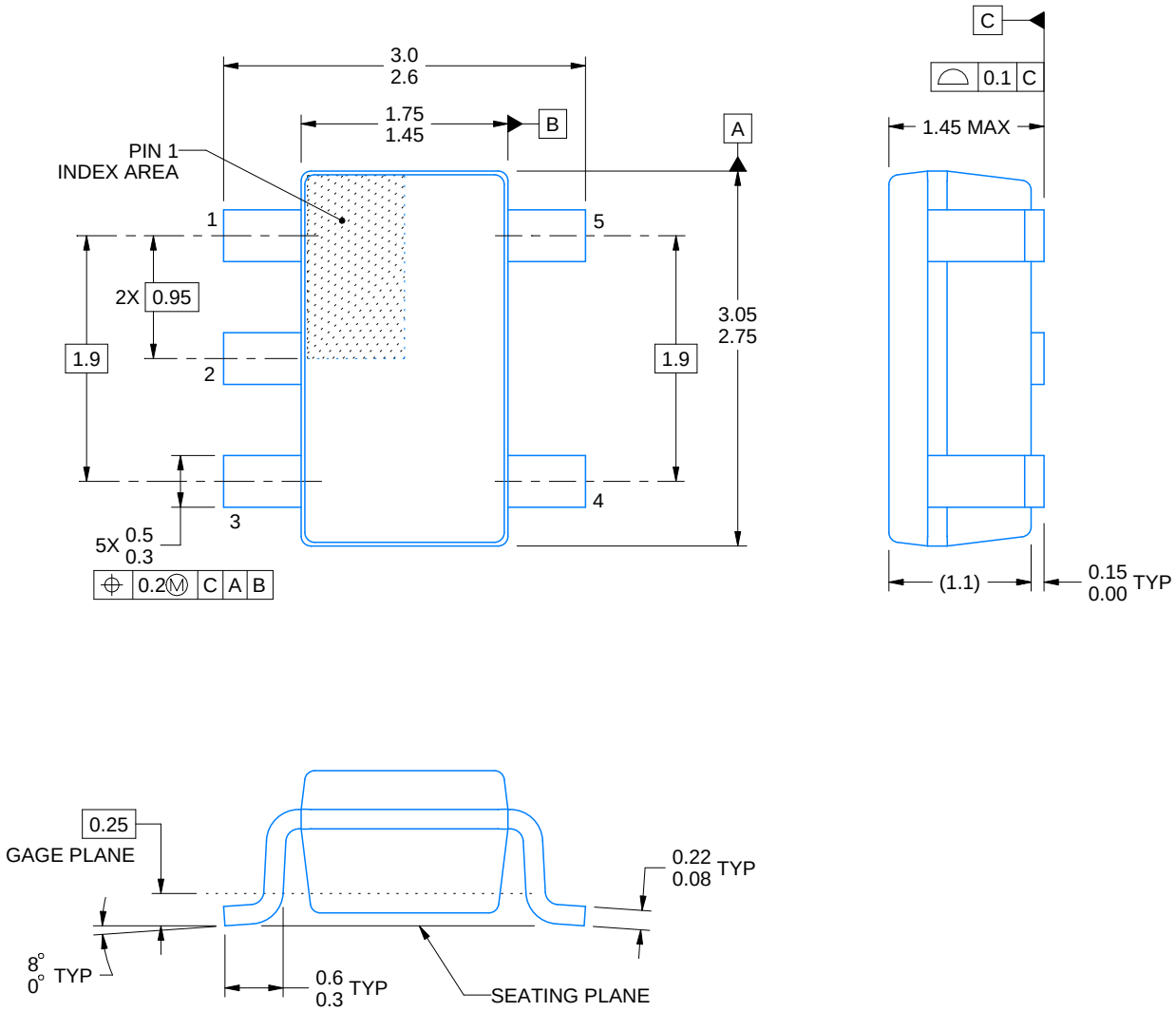
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

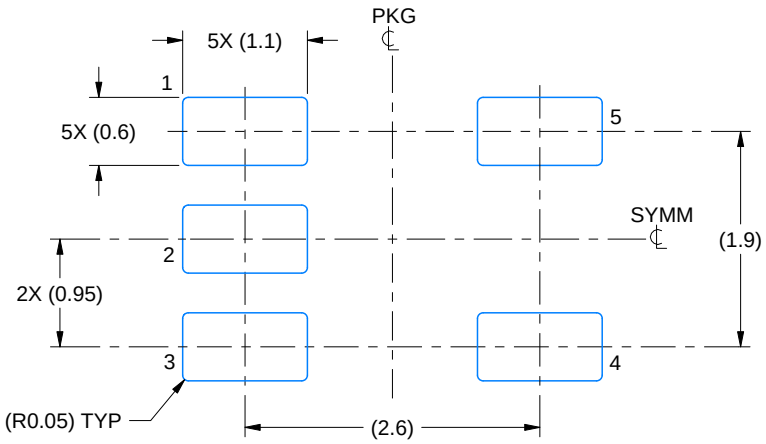
SMALL OUTLINE TRANSISTOR



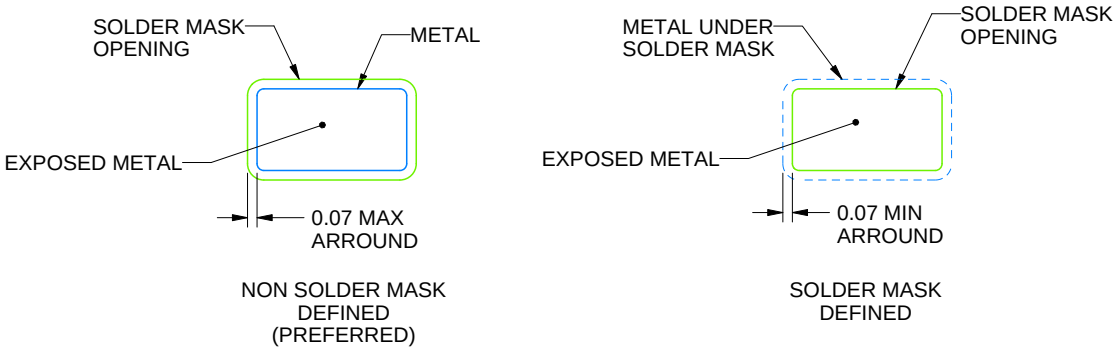
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

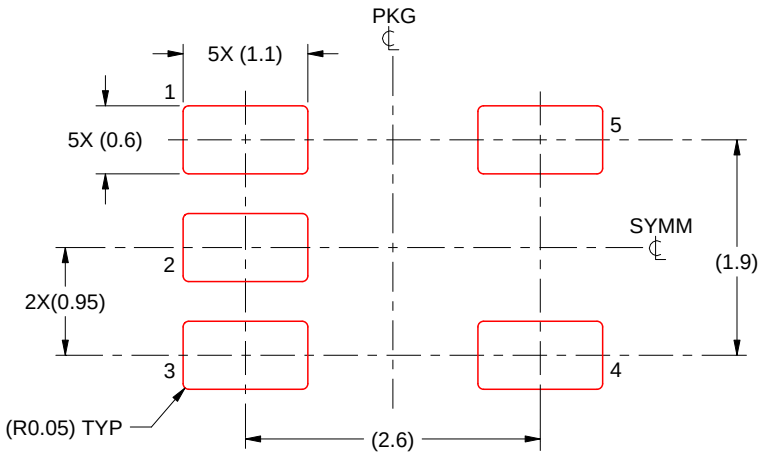


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



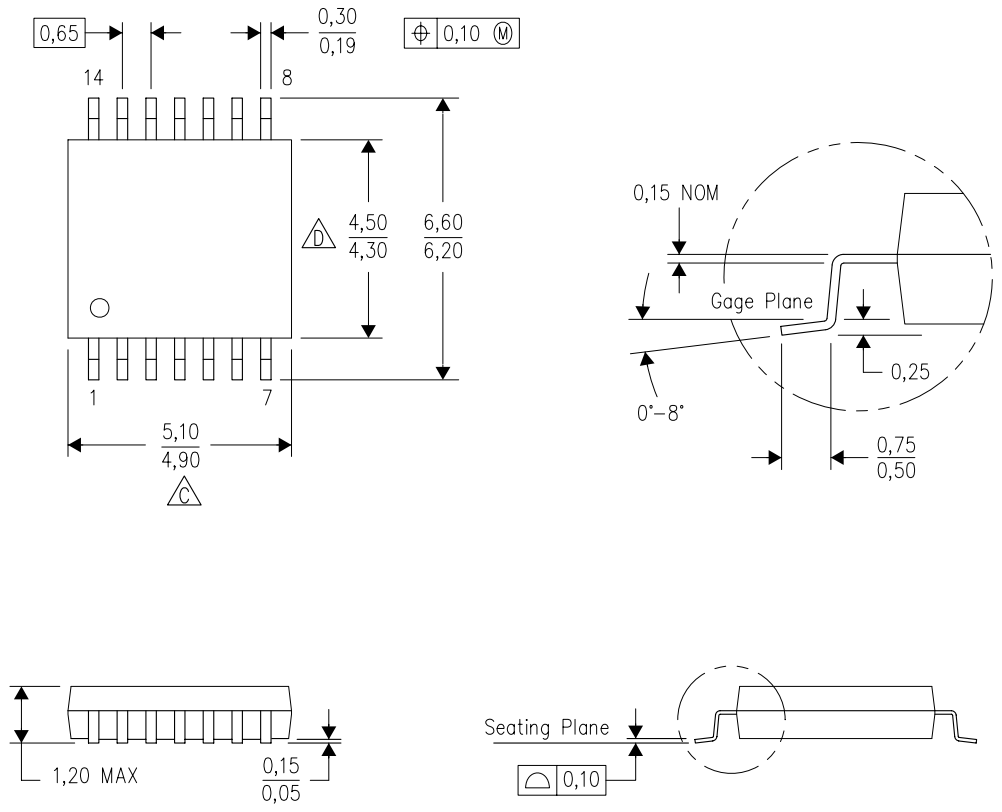
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

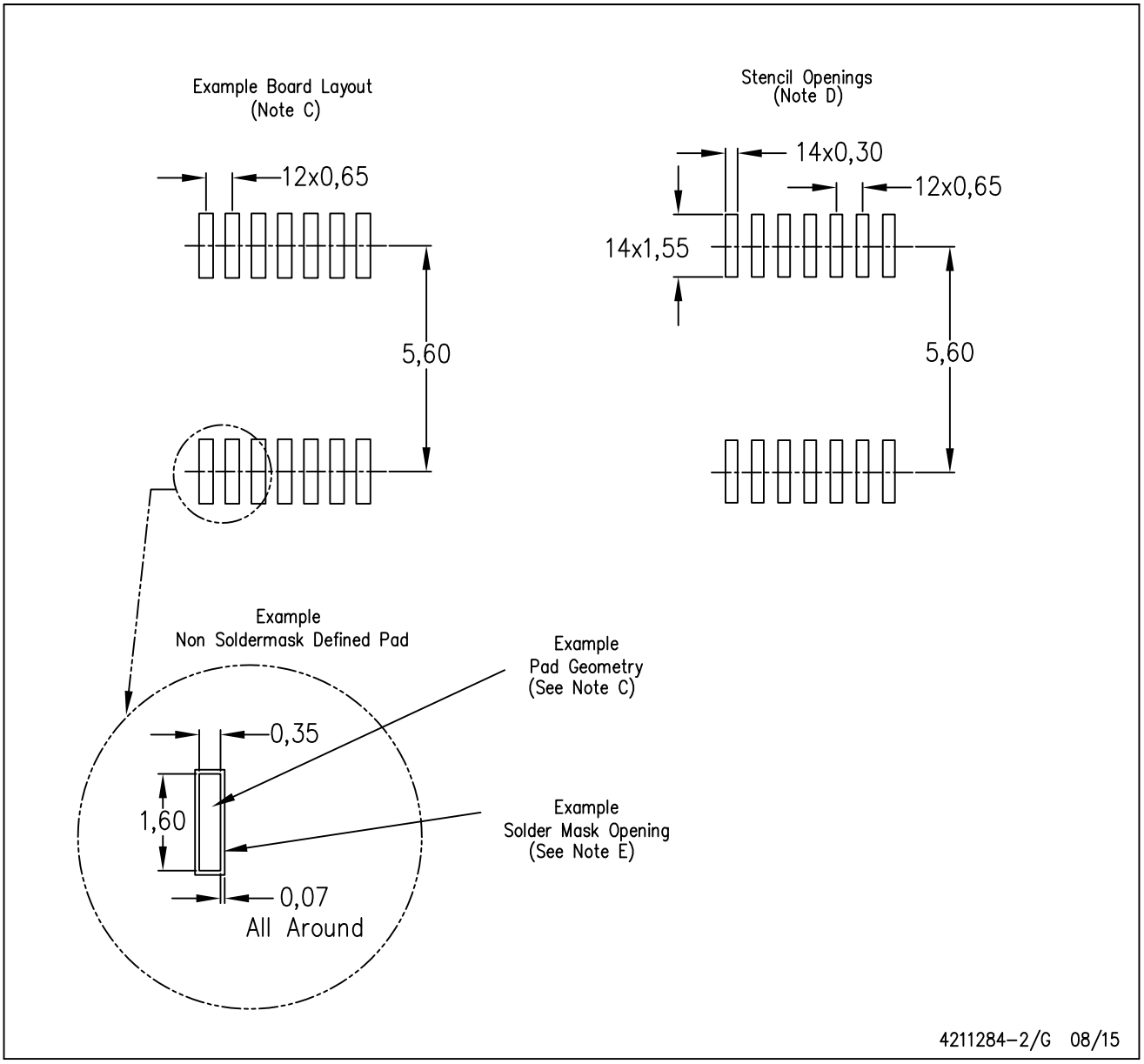
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

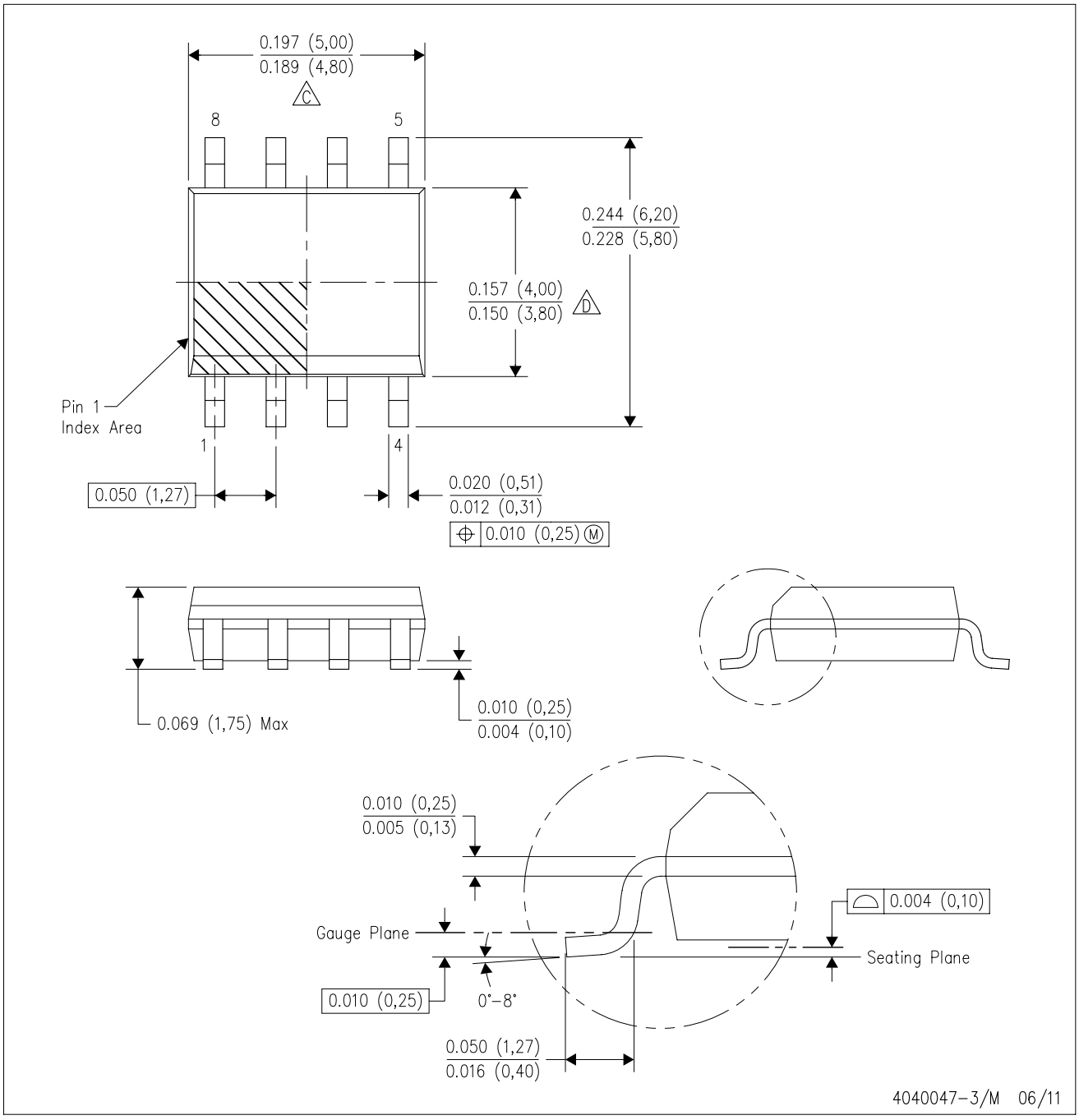
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



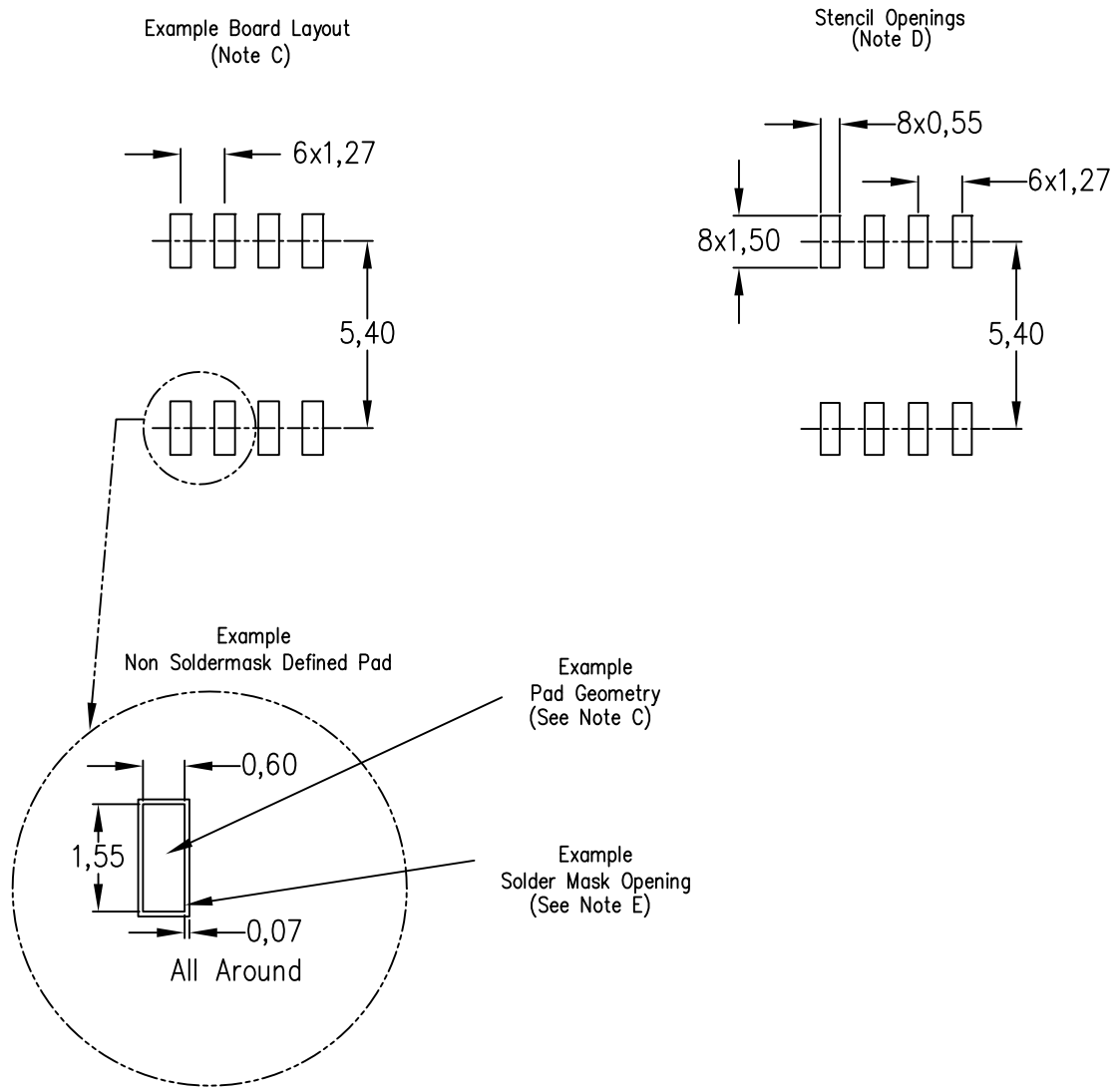
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



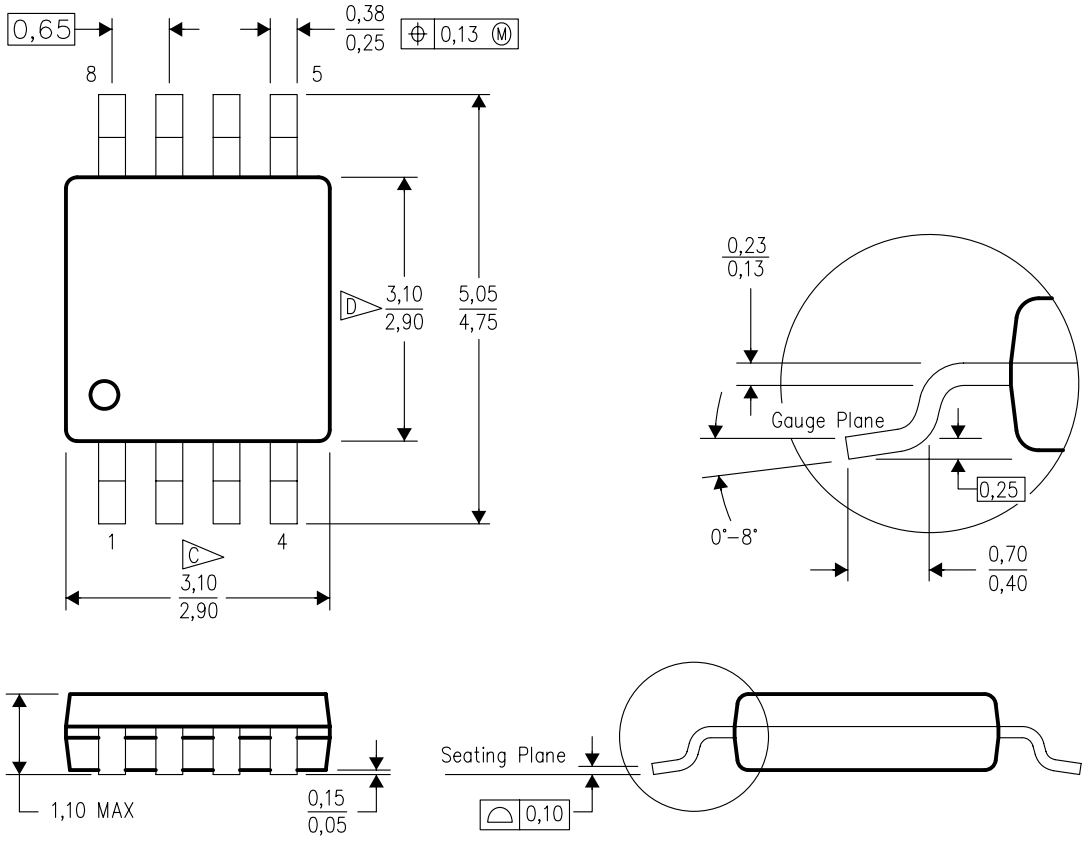
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

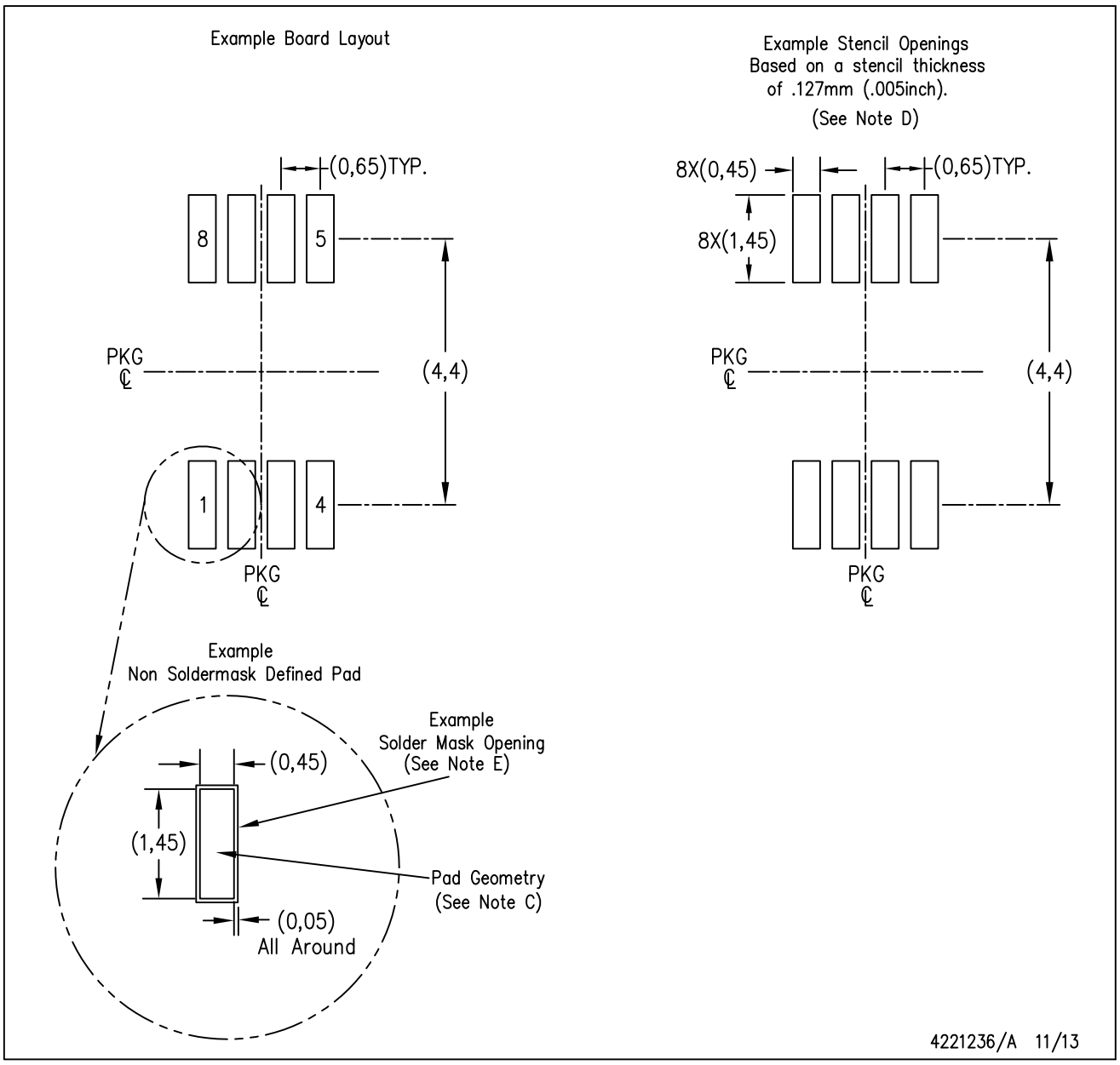
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

SBAS357A – SEPTEMBER 2006 – REVISED OCTOBER 2007

LOW-POWER, 12-Bit ANALOG-TO-DIGITAL CONVERTER with I²C™ INTERFACE

FEATURES

- **Complete 12-Bit Data Acquisition System in a Tiny SOT-23 Package**
- **Low Current Consumption: Only 90µA**
- **Integral Nonlinearity: 1LSB Max**
- **Single-Cycle Conversion**
- **Programmable Gain Amplifier Gain = 1, 2, 4, or 8**
- **128SPS Data Rate**
- **I²C Interface with Two Available Addresses**
- **Power Supply: 2.7V to 5.5V**
- **Pin- and Software-Compatible with 16-Bit ADS1100**

APPLICATIONS

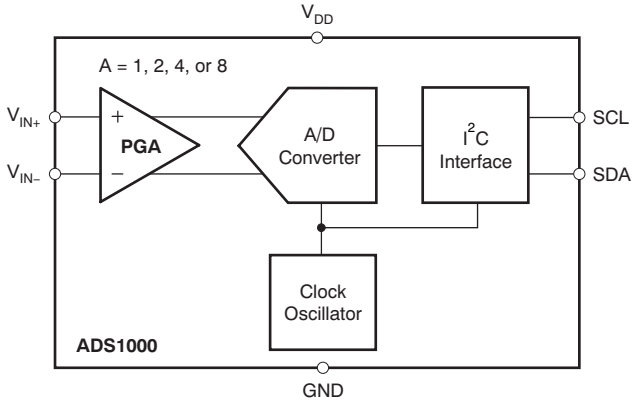
- **Voltage Monitors**
- **Battery Management**
- **Industrial Process Control**
- **Consumer Goods**
- **Temperature Measurement**

DESCRIPTION

The ADS1000 is an I²C-compatible serial interface Analog-to-Digital (A/D) converter with differential inputs and 12 bits of resolution in a tiny SOT23-6 package. Conversions are performed ratiometrically, using the power supply as the reference voltage. The ADS1000 operates from a single power supply ranging from 2.7V to 5.5V.

The ADS1000 performs conversions at a rate of 128 samples per second (SPS). The onboard programmable gain amplifier (PGA), which offers gains of up to 8, allows smaller signals to be measured with high resolution. In single-conversion mode, the ADS1000 automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The ADS1000 is designed for applications where space and power consumption are major considerations. Typical applications include portable instrumentation, consumer goods, and voltage monitoring.



PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	ADS1000	UNIT
V_{DD} to GND	–0.3 to +6	V
Input Current (Momentary)	100	mA
Input Current (Continuous)	10	mA
Voltage to GND, V_{IN+}, $V_{IN–}$	–0.3 to V_{DD} to +0.3	V
Voltage to GND, SDA, SCL	–0.5 to +6	V
Maximum Junction Temperature, T_J	+150	°C
Operating Temperature	–40 to +125	°C
Storage Temperature	–60 to +150	°C
Lead Temperature (soldering, 10s)	+300	°C

(1) Stresses above those listed under ***Absolute Maximum Ratings*** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

NOTE: Marking text direction indicates pin 1. Marking text depends on I^2C address; see Package Option Addendum.

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +85°C, V_{DD} = 5V, GND = 0V, and all PGAs, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1000			UNIT
		MIN	TYP	MAX	
ANALOG INPUT					
Full-Scale Input Voltage	$(V_{IN+}) – (V_{IN–})$		$\pm V_{DD}/PGA$ (1)		V
Analog Input Voltage	V_{IN+}, $V_{IN–}$ to GND	GND – 0.2		V_{DD} + 0.2	V
Differential Input Impedance			2.4/PGA		MΩ
Common-Mode Input Impedance			8		MΩ
SYSTEM PERFORMANCE					
Resolution	No Missing Codes	12			Bits
Data Rate		104	128	184	SPS
Integral Nonlinearity (INL)			±0.1	1	LSB
Offset Error			1	±2	LSB
Gain Error			0.01	0.1	%
DIGITAL INPUT/OUTPUT					
Logic Level					
V_{IH}		0.7 VDD		6	V
V_{IL}		GND – 0.5		0.3 V_{DD}	V
V_{OL}	I_{OL} = 3mA	GND		0.4	V
Input Leakage					
I_{IH}	V_{IH} = 5.5V			10	µA
I_{IL}	V_{IL} = GND	– 10			µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	V_{DD}	2.7		5.5	V
Supply Current	Power-Down		0.05	2	µA
	Active		90	150	µA
Power Dissipation					µA
	V_{DD} = 5.0V		450	750	µW
	V_{DD} = 3.0V		210		µW

(1) Each input, V_{IN+} and $V_{IN–}$, must meet the absolute input voltage specifications.

TYPICAL CHARACTERISTICS

At T_A = 25°C and V_{DD} = 5V, unless otherwise indicated.

SUPPLY CURRENT vs TEMPERATURE

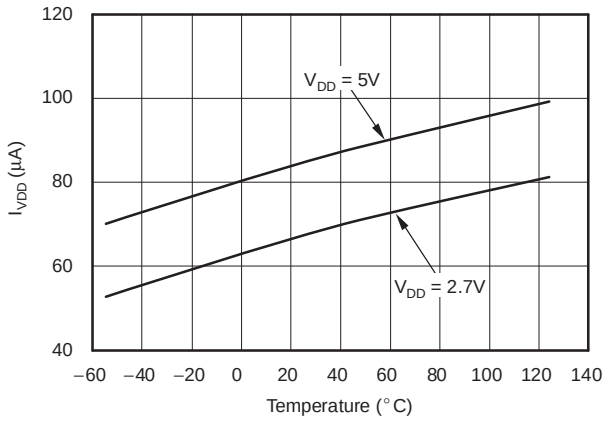


Figure 1.

SUPPLY CURRENT vs I²C BUS FREQUENCY

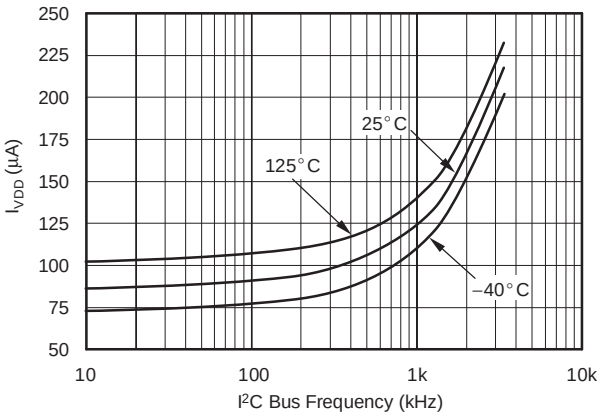


Figure 2.

OFFSET ERROR vs TEMPERATURE

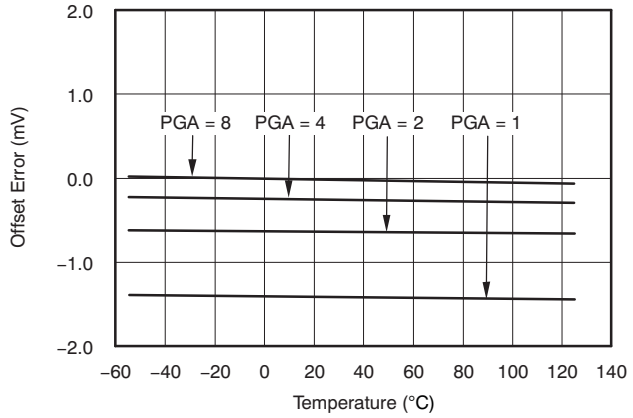


Figure 3.

GAIN ERROR vs TEMPERATURE

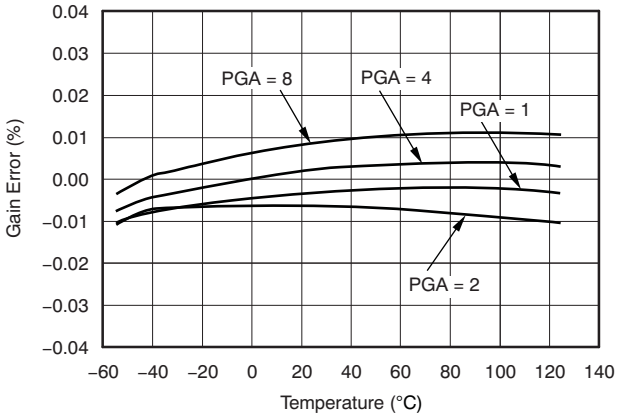


Figure 4.

DATA RATE vs TEMPERATURE

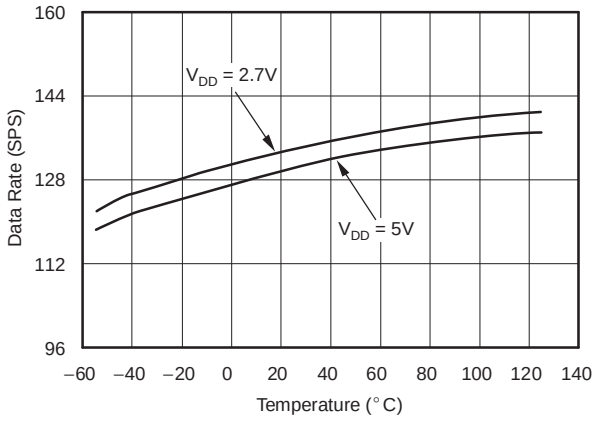


Figure 5.

THEORY OF OPERATION

The ADS1000 is a fully differential, 12-bit A/D converter. The ADS1000 allows users to obtain precise measurements with a minimum of effort, and the device is extremely easy to design with and configure.

The ADS1000 consists of an A/D converter core with adjustable gain, a clock generator, and an I^2C interface. Each of these blocks are described in detail in the sections that follow.

ANALOG-TO-DIGITAL CONVERTER

The ADS1000 uses a switched-capacitor input stage. To external circuitry, it looks roughly like a resistance. The resistance value depends on the capacitor values and the rate at which they are switched. The switching clock is generated by the onboard clock generator, so its frequency, nominally 275kHz, is dependent on supply voltage and temperature. The capacitor values depend on the PGA setting.

The common-mode and differential input impedances are different. For a gain setting of PGA, the differential input impedance is typically 2.4MΩ/PGA.

The common-mode impedance is typically 8MΩ.

OUTPUT CODE CALCULATION

The ADS1000 outputs codes in binary two's complement format. The output code is confined to the range of numbers: –2048 to 2047, and is given by:

$$\text{Output Code} = 2048(\text{PGA})\left(\frac{V_{IN+} - V_{IN-}}{V_{DD}}\right)$$

CLOCK GENERATOR

The ADS1000 features an onboard clock generator. The Typical Characteristics show variations in data rate over supply voltage and temperature. It is not possible to operate the ADS1000 with an external clock.

USING THE ADS1000

OPERATING MODES

The ADS1000 operates in one of two modes: continuous conversion and single conversion.

In continuous conversion mode, the ADS1000 continuously performs conversions. Once a conversion has been completed, the ADS1000 places the result in the output register, and immediately begins another conversion. When the ADS1000 is in continuous conversion mode, the ST/BSY bit in the configuration register always reads '1'.

In single conversion mode, the ADS1000 waits until the ST/BSY bit in the conversion register is set to '1'. When this happens, the ADS1000 powers up and performs a single conversion. After the conversion completes, the ADS1000 places the result in the output register, resets the ST/BSY bit to '0' and powers down. Writing a '1' to ST/BSY while a conversion is in progress has no effect.

When switching from continuous conversion mode to single conversion mode, the ADS1000 will complete the current conversion, reset the ST/BSY bit to '0' and power-down the device.

RESET AND POWER-UP

When the ADS1000 powers up, it automatically performs a reset. As part of the reset, the ADS1000 sets all of the bits in the configuration register to their respective default settings.

The ADS1000 responds to the I^2C General Call Reset command. When the ADS1000 receives a General Call Reset, it performs an internal reset, exactly as though it had just been powered on.

I^2C INTERFACE

The ADS1000 communicates through an I^2C (Inter-Integrated Circuit) interface. The I^2C interface is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines low, by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pull-up resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the ADS1000 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the bit level while SCL is low (a Low on SDA indicates the bit is '0'; a High indicates the bit is '1'). Once the SDA line has settled, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1000 never drives SCL, because it cannot act as a master. On the ADS1000, SCL is an input only.

Most of the time the bus is idle, no communication takes place, and both lines are high. When communication takes place, the bus is active. Only master devices can start a communication. They do this by causing a start condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a *start* condition or its counterpart, a *stop* condition. A start condition is when the clock line is high and the data line goes from high to low. A stop condition is when the clock line is high and the data line goes from low to high.

After the master issues a start condition, it sends a byte that indicates with which slave device it wants to communicate. This byte is called the *address byte*. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it be address or data, is acknowledged with an *acknowledge* bit. When a master has finished sending a byte, eight data bits, to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA low to acknowledge to the slave that it has finished reading the byte. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A *not-acknowledge* is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not-acknowledge because no device is present at that address to pull the line low.

When a master has finished communicating with a slave, it may issue a stop condition. When a stop condition is issued, the bus becomes idle again. A master may also issue another start condition. When a start condition is issued while the bus is active, it is called a *repeated start condition*.

A timing diagram for an ADS1000 I^2C transaction is shown in Figure 6. Table 1 gives the parameters for this diagram.

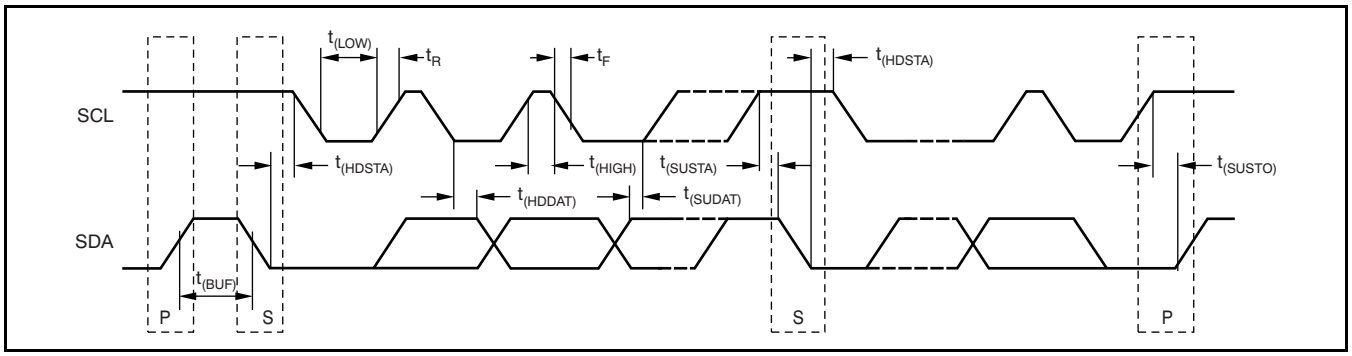


Figure 6. I²C Timing Diagram

Table 1. Timing Diagram Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCLK Operating Frequency	$f_{(SCLK)}$		0.4		3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold Time After Repeated START Condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	600		160		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	600		160		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	600		160		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCLK Clock Low Period	$t_{(LOW)}$	1300		160		ns
SCLK Clock High Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns

ADS1000 I²C ADDRESSES

The ADS1000 I²C address is either 1001000 or 1001001, set at the factory. The address is identified with an A0 or an A1 within the orderable name.

The two different I²C variants are also marked differently. Devices with an I²C address of 1001000 have packages marked **BD0**, while devices with an I²C address of 1001001 are marked with **BD1**. See the Package/Ordering Information Table for a complete listing of the ADS1000 I²C addresses and tape and reel size.

I²C GENERAL CALL

The ADS1000 responds to General Call Reset, which is an address byte of 00h followed by a data byte of 06h. The ADS1000 acknowledges both bytes.

On receiving a General Call Reset, the ADS1000 performs a full internal reset, just as though it had been powered off and then on. If a conversion is in process, it is interrupted; the output register is set to zero, and the configuration register returns to its default setting.

The ADS1000 always acknowledges the General Call address byte of 00h, but it does not acknowledge any General Call data bytes other than 04h or 06h.

I²C DATA RATES

The I²C bus operates in one of three speed modes: *Standard*, which allows a clock frequency of up to 100kHz; *Fast*, which allows a clock frequency of up to 400kHz; and *High-speed* mode (also called Hs mode), which allows a clock frequency of up to 3.4MHz. The ADS1000 is fully compatible with all three modes.

No special action needs to be taken to use the ADS1000 in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001XXX following the start condition, where the ***XXX*** bits are unique to the Hs-capable master. This byte is called the *Hs master code*. (Note that this is different from normal address bytes; the low bit does not indicate read/write status.) The ADS1000 will not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. On receiving a master code, the ADS1000 will switch on its High-speed mode filters, and will communicate at up to 3.4MHz. The ADS1000 switches out of Hs mode with the next stop condition.

For more information on High-speed mode, consult the I²C specification.

REGISTERS

The ADS1000 has two registers that are accessible via its I²C port. The output register contains the result of the last conversion; the configuration register allows users to change the ADS1000 operating mode and query the status of the device.

OUTPUT REGISTER

The 16-bit output register contains the result of the last conversion in binary two's complement format. Since the port yields 12 bits of data, the ADS1000 outputs right-justified and sign-extended codes. This output format makes it possible to perform averaging using a 16-bit accumulator.

Following reset or power-up, the output register is cleared to '0'; it remains zero until the first conversion is completed. Therefore, if a user reads the ADS1000 just after reset or power-up, the output register will read '0'.

The output register format is shown in Table 2.

Table 2. OUTPUT REGISTER

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15(1)	D14(1)	D13(1)	D12(1)	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) D15–D12 are sign extensions of 12-bit data.

CONFIGURATION REGISTER

A user controls the ADS1000 operating mode and PGA settings via the 8-bit configuration register. The configuration register format is shown in Table 3. The default setting is 80H.

Table 3. CONFIGURATION REGISTER

7	6	5	4	3	2	1	0
ST/BSY	0	0	SC	0	0	PGA1	PGA0

Bit 7: ST/BSY

The meaning of the ST/BSY bit depends on whether it is being written to or read from.

In single conversion mode, writing a '1' to the ST/BSY bit causes a conversion to start, and writing a '0' has no effect. In continuous conversion mode, the ADS1000 ignores the value written to ST/BSY.

When read in single conversion mode, ST/BSY indicates whether the A/D converter is busy taking a conversion. If ST/BSY is read as '1', the A/D converter is busy, and a conversion is taking place; if '0', no conversion is taking place, and the result of the last conversion is available in the output register.

In continuous mode, ST/BSY is always read as '1'.

Bits 6 - 5: Reserved

Bits 6 and 5 must be set to zero.

Bit 4: SC

SC controls whether the ADS1000 is in continuous conversion or single conversion mode. When SC is '1', the ADS1000 is in single conversion mode; when SC is '0', the ADS1000 is in continuous conversion mode. The default setting is '0'.

Bits 3 - 2: Reserved

Bits 3 and 2 must be set to zero.

Bits 1 - 0: PGA

Bits 1 and 0 control the ADS1000 gain setting; see Table 4.

Table 4. PGA Bits

PGA1	PGA0	GAIN
0(1)	0(1)	1(1)
0	1	2
1	0	4
1	1	8
(1) Default setting.		

READING FROM THE ADS1000

A user can read the output register and the contents of the configuration register from the ADS1000. To do this, address the ADS1000 for reading, and read three bytes from the device. The first two bytes are the output register contents; the third byte is the configuration register contents.

A user does not always have to read three bytes from the ADS1000. If only the contents of the output register are needed, read only two bytes.

Reading more than three bytes from the ADS1000 has no effect. All of the bytes beginning with the fourth byte will be FFh. See Figure 7 for a timing diagram of an ADS1000 read operation.

WRITING TO THE ADS1000

A user can write new contents into the configuration register (the contents of the output register cannot change). To do this, address the ADS1000 for writing, and write one byte to it. This byte is written into the configuration register.

Writing more than one byte to the ADS1000 has no effect. The ADS1000 ignores any bytes sent to it after the first one, and will only acknowledge the first byte. See Figure 8 for a timing diagram of an ADS1000 write operation.

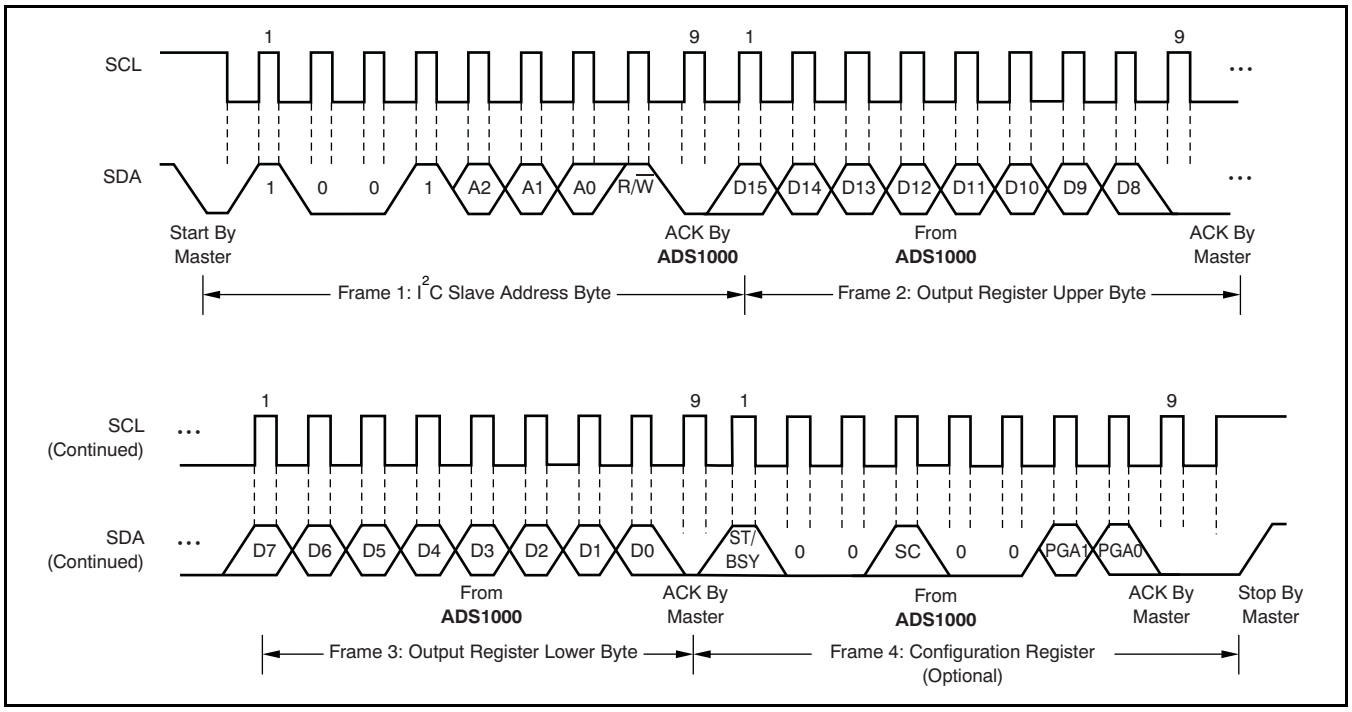


Figure 7. Timing Diagram for Reading from the ADS1000

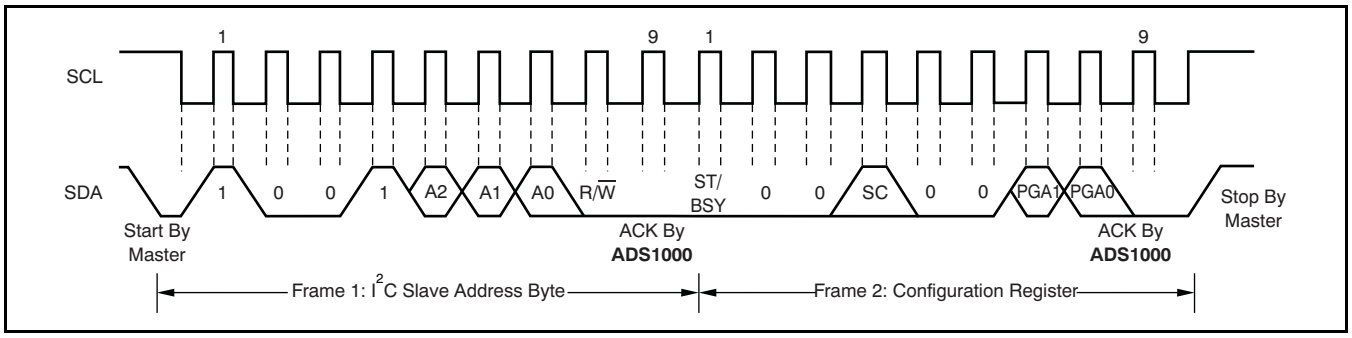


Figure 8. Timing Diagram for Writing to the ADS1000

APPLICATION INFORMATION

BASIC CONNECTIONS

For many applications, connecting the ADS1000 is extremely simple. A basic connection diagram for the ADS1000 is shown in Figure 9.

The fully differential voltage input of the ADS1000 is ideal for connection to differential sources with moderately low source impedance, such as bridge sensors and thermistors. Although the ADS1000 can read bipolar differential signals, it cannot accept negative voltages on either input. It may be helpful to think of the ADS1000 positive voltage input as noninverting, and of the negative input as inverting.

When the ADS1000 is converting, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1000 interfaces directly to standard mode, fast mode, and high-speed mode I^2C controllers. Any microcontroller I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, will work with the ADS1000. The ADS1000 does not perform clock-stretching (that is, it never pulls the clock line low), so it is not necessary to provide for this unless other devices are on the same I^2C bus.

Pull-up resistors are necessary on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

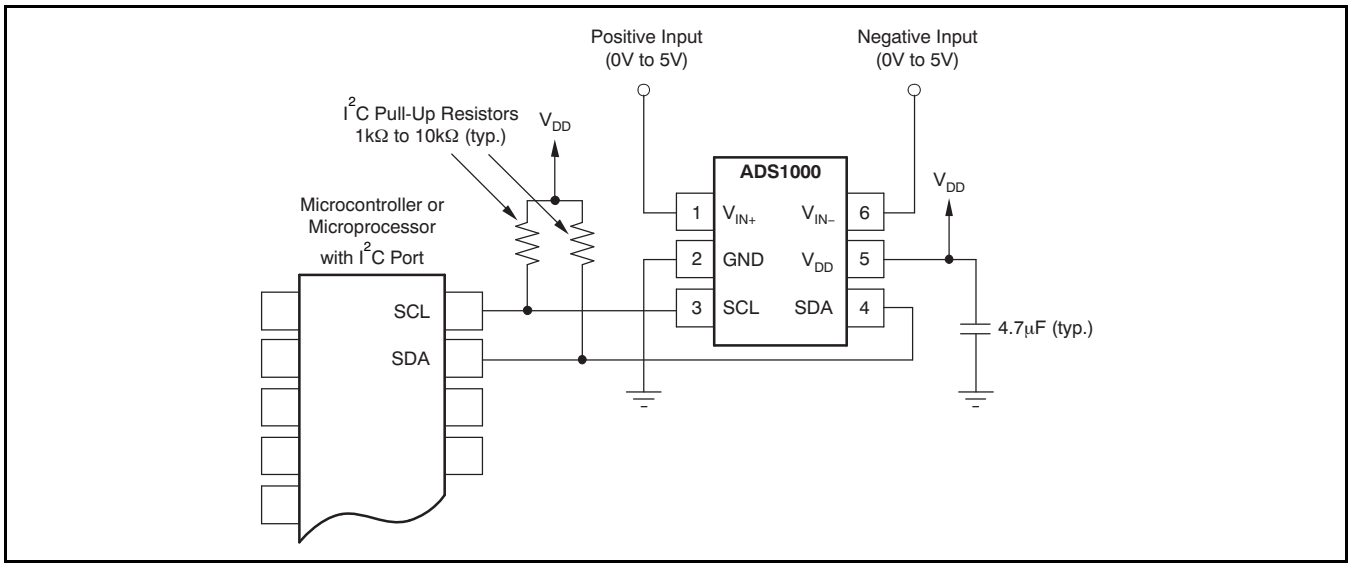


Figure 9. Typical Connections of the ADS1000

CONNECTING MULTIPLE DEVICES

Connecting two ADS1000s to a single bus is almost trivial. An example showing two ADS1000s and one ADS1100 connected on a single bus is shown in Figure 10. Multiple devices can be connected to a single bus (provided that their addresses are different).

Note that only one set of pull-up resistors is needed per bus. A user might find that he or she needs to lower the pull-up resistor values slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

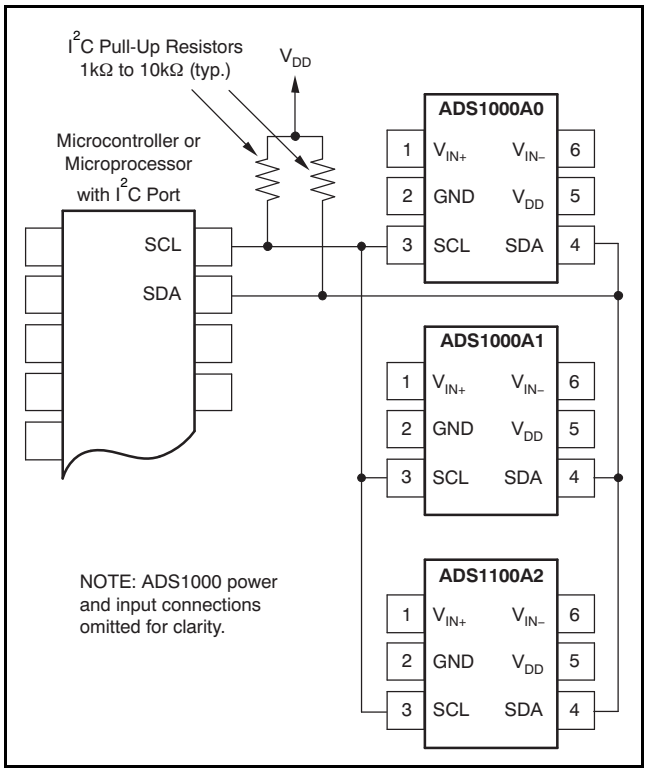


Figure 10. Connecting Multiple ADS1000s

USING GPIO PORTS FOR I²C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the ADS1000 can be connected to GPIO pins, and the I²C bus protocol simulated, or bit-banged, in software. An example of this for a single ADS1000 is shown in Figure 11.

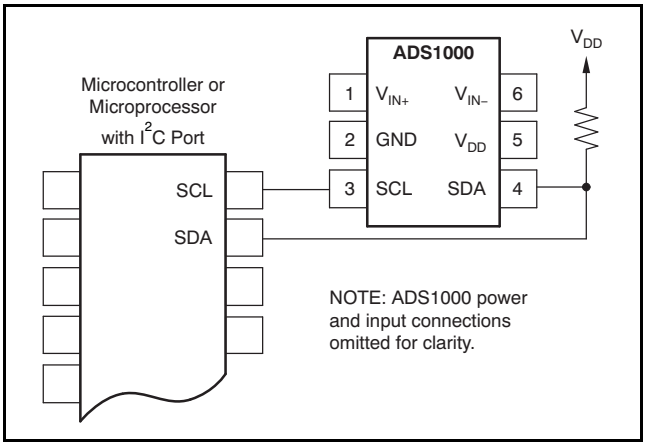


Figure 11. Using GPIO with a Single ADS1000

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output a '0'; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this device will read as a '0' in the port input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to '1' or '0' as appropriate. It can do this because the ADS1000 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption resulting from the absence of a resistive pull-up.

If there are any devices on the bus that may drive their clock lines low, the above method should not be used; the SCL line should be high-Z or zero and a pull-up resistor provided as usual. Note also that this cannot be done on the SDA line in any case, because the ADS1000 does drive the SDA line low from time to time, as all I²C devices do.

Some microcontrollers have selectable strong pull-up circuits built into the GPIO ports. In some cases, these can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I²C communication. If there is any doubt about the matter, test the circuit before committing it to production.

SINGLE-ENDED INPUTS

Although the ADS1000 has a fully differential input, it can easily measure single-ended signals. A simple single-ended connection scheme is shown in Figure 12. The ADS1000 is configured for single-ended measurement by grounding either of its input pins, usually V_{IN-}, and applying the input signal to V_{IN+}. The single-ended signal can range from –0.2V to V_{DD} + 0.3V. The ADS1000 loses no linearity anywhere in its input range. Negative voltages cannot be applied to this circuit because the ADS1000 inputs can only accept positive voltages.

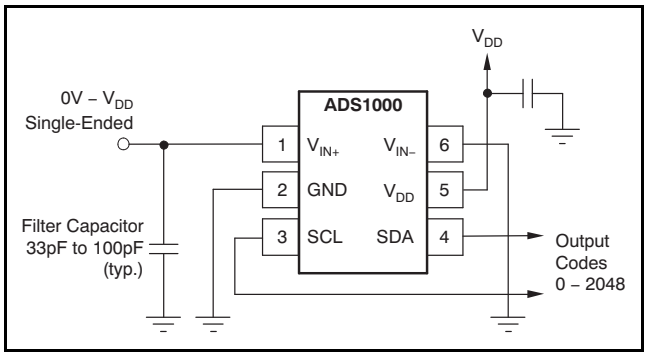


Figure 12. Measuring Single-Ended Inputs

The ADS1000 input range is bipolar differential with respect to the reference, that is, V_{DD}. The single-ended circuit shown in Figure 12 covers only half the ADS1000 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost. The DRV134 balanced line driver can be employed to regain this bit for single-ended signals.

Negative input voltages must be level-shifted. A good candidate for this function is the THS4130 differential amplifier, which can output fully differential signals. This device can also help recover the lost bit noted previously for single-ended positive signals. Level-shifting can also be performed using the DRV134.

LOW-SIDE CURRENT MONITOR

Figure 13 shows a circuit for a low-side shunt-type current monitor. The circuit reads the voltage across a shunt resistor, which is sized as small as possible while still giving a readable output voltage. This voltage is amplified by an OPA335 low-drift op-amp, and the result is read by the ADS1000.

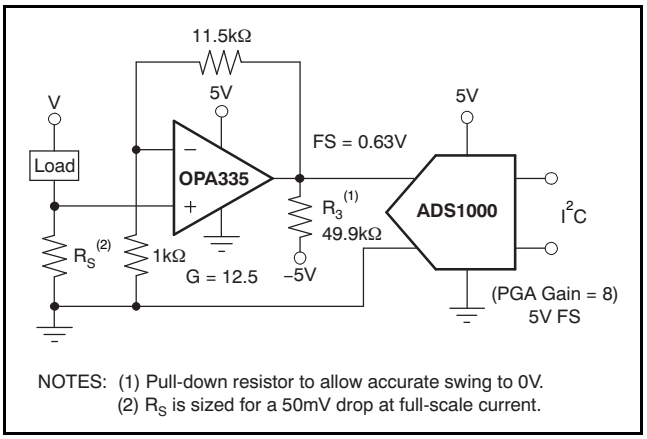


Figure 13. Low-Side Current Measurement

It is recommended that the ADS1000 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 8, the op amp should be configured to give a maximum output voltage of no greater than 0.75V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1000 is 0.63V.

ADDITIONAL RECOMMENDATIONS

The ADS1000 is fabricated in a small-geometry low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1000 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1000 analog inputs can withstand momentary currents of as large as 10mA.

The previous paragraph does not apply to the I^2C ports, which can both be driven to 6V regardless of the supply.

If the ADS1000 is driven by an op amp with high voltage supplies, such as ±12V, protection should be provided, even if the op amp is configured so that it will not output out-of-range voltages. Many op amps seek to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1000. Sometimes this damage is incremental and results in slow, long-term failure—which can be distastrous for permanently installed, low-maintenance systems.

If using an op amp or other front-end circuitry with the ADS1000, be sure to take the performance characteristics of this circuitry into account; a chain is only as strong as its weakest link.

Any data converter is only as good as its reference. For the ADS1000, the reference is the power supply, and the power supply must be clean enough to achieve the desired performance. If a power-supply filter capacitor is used, it should be placed close to the V_{DD} pin, with no vias placed between the capacitor and the pin. The trace leading to the pin should be as wide as possible, even if it must be necked down at the device.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2006) to Revision A	Page
• Changed logic level min value from (0.7GND) to (0.7VDD)	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1000A0IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A0IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A0IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A0IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A1IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD1	Samples
ADS1000A1IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD1	Samples
ADS1000A1IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS1000 :

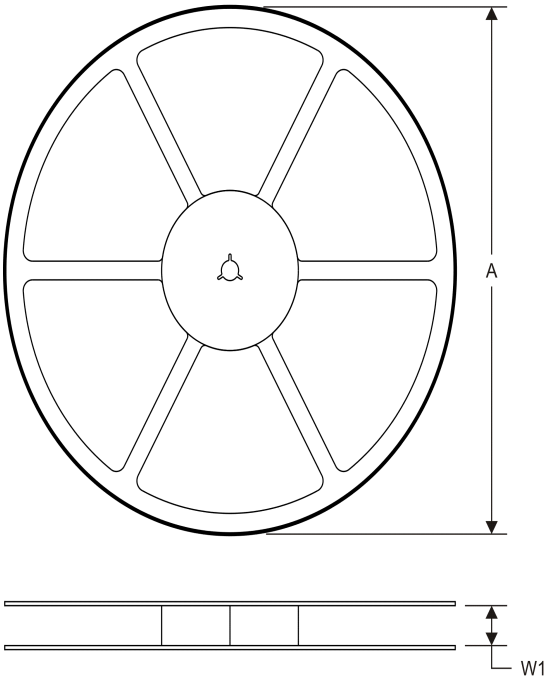
- Automotive: ADS1000-Q1

NOTE: Qualified Version Definitions:

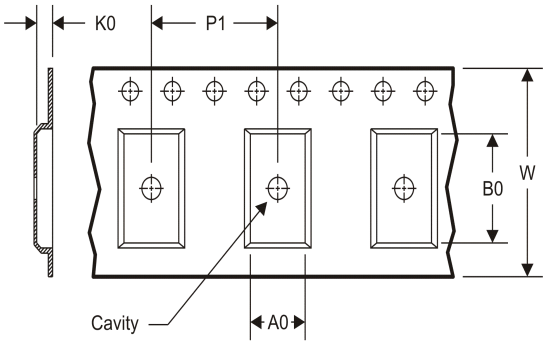
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



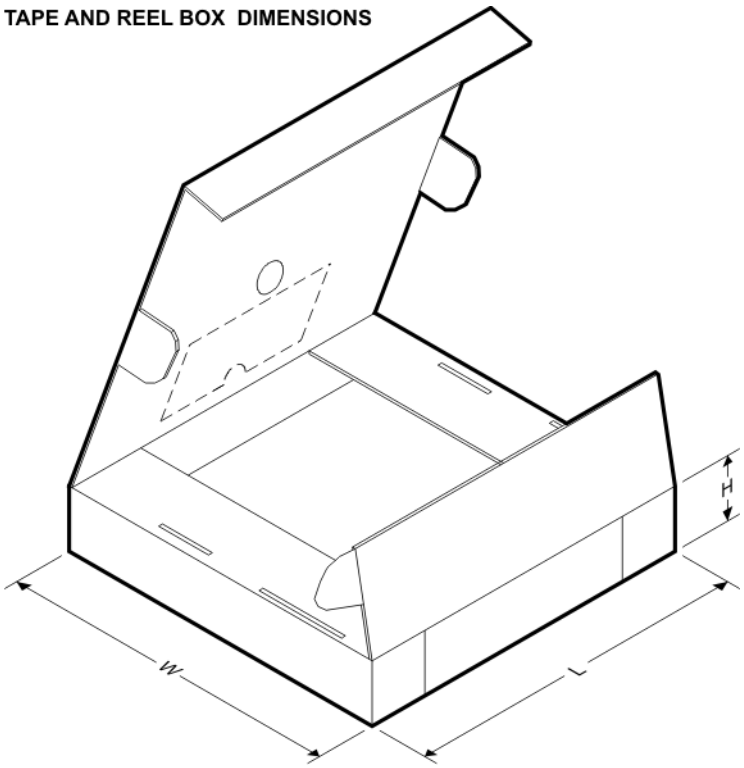
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1000A0IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1000A0IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1000A1IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1000A1IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

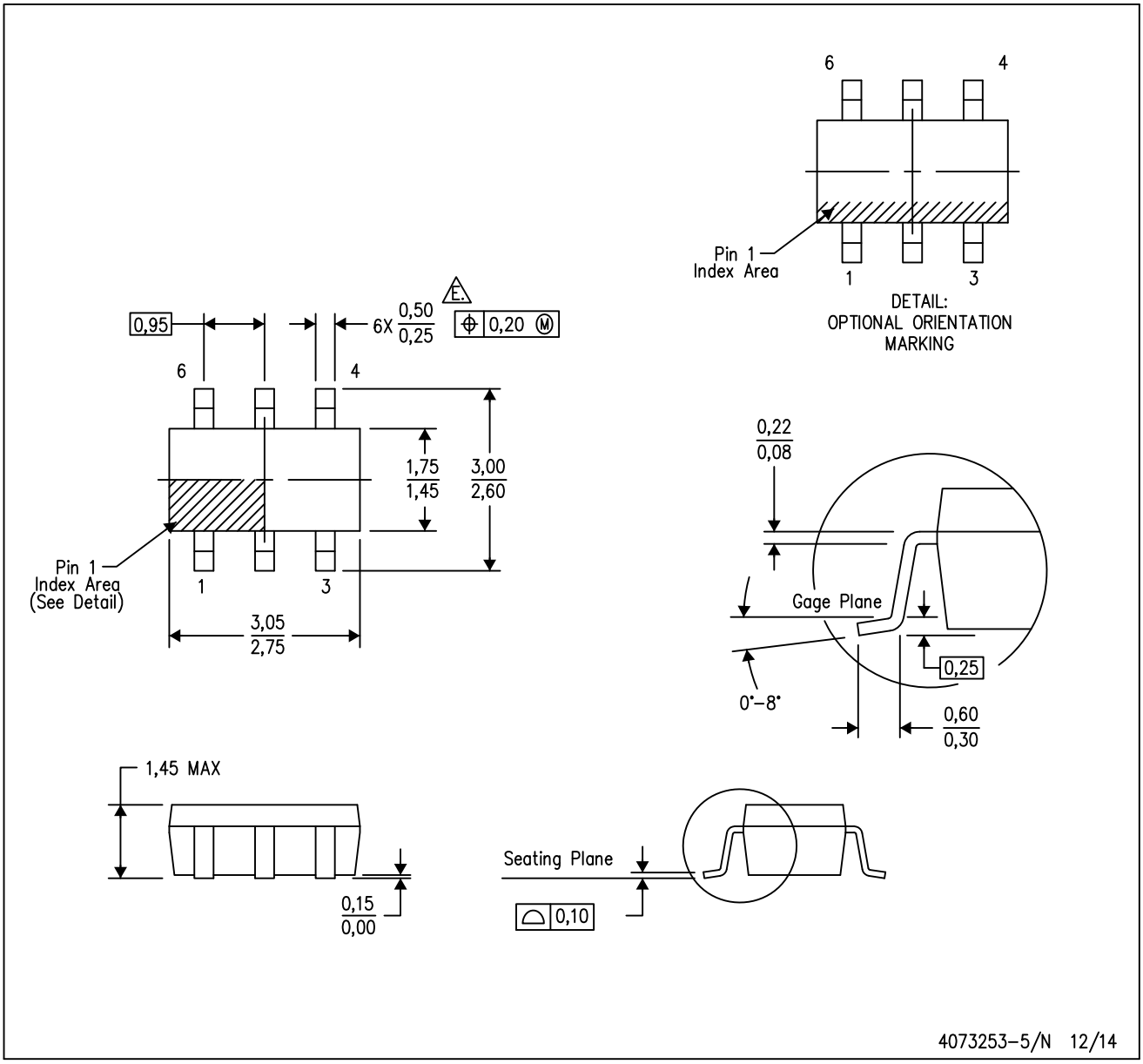
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

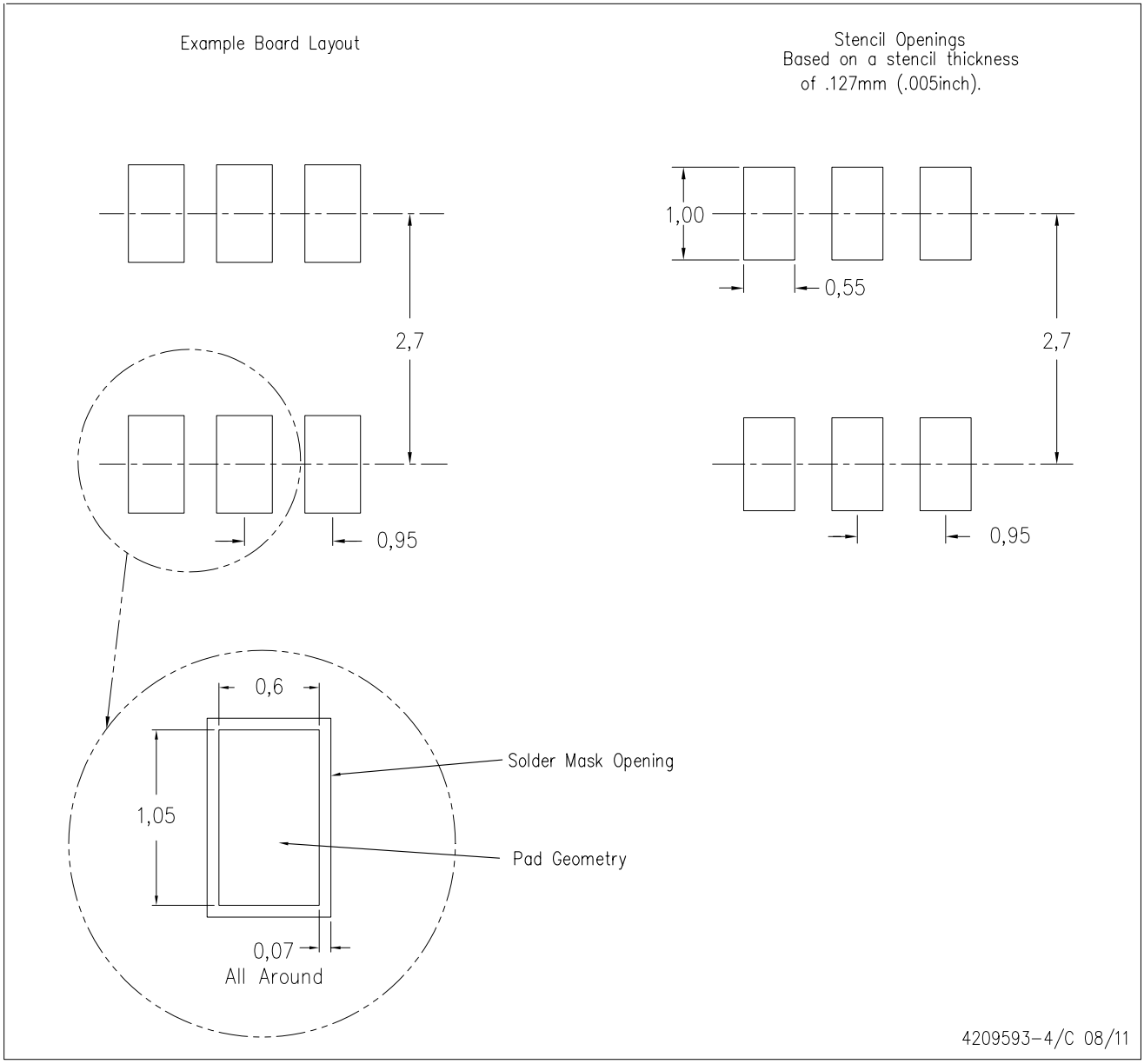
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1000A0IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1000A0IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1000A1IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1000A1IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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TPS7A49 36-V, 150-mA, Ultralow-Noise, Positive Linear Regulator

1 Features

- Input Voltage Range: 3 V to 36 V
- Noise:
  - 12.7 μV_{RMS} (20 Hz to 20 kHz)
  - 15.4 μV_{RMS} (10 Hz to 100 kHz)
- Power-Supply Ripple Rejection:
  - 72 dB (120 Hz)
  - ≥ 52 dB (10 Hz to 400 kHz)
- Adjustable Output: 1.194 V to 33 V
- Output Current: 150 mA
- Dropout Voltage: 260 mV at 100 mA
- Stable with Ceramic Capacitors ≥ 2.2 µF
- CMOS Logic-Level-Compatible Enable Pin
- Fixed Current-Limit and Thermal Shutdown Protection
- Packages: 8-Pin HVSSOP PowerPAD™ and 3-mm × 3-mm VSON
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry
- Audio
- Post DC-DC Converter Regulation and Ripple Filtering
- Test and Measurement
- Rx, Tx, and PA Circuitry
- Industrial Instrumentation
- Base Stations and Telecom Infrastructure

3 Description

The TPS7A49 series of devices are positive, high-voltage (36 V), ultralow-noise (15.4 μV_{RMS}, 72-dB PSRR) linear regulators that can source a 150-mA load.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other available features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A49 family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A49 family of linear regulators is suitable for post dc-dc converter regulation. By filtering out the output voltage ripple inherent to dc-dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

For applications where positive and negative high-performance rails are required, consider TI's TPS7A30xx family of negative high-voltage, ultralow-noise linear regulators as well.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A49	HVSSOP PowerPAD (8)	3.00 mm × 3.00 mm
	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Post DC-DC Converter Regulation for High-Performance Analog Circuitry

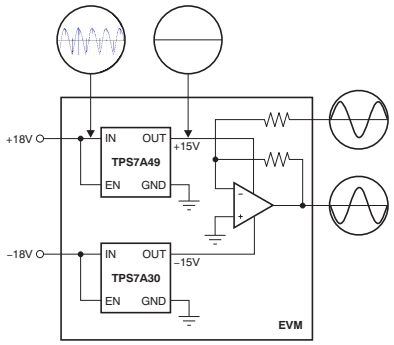


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2015) to Revision E — **Page**

- Added DRB package to document ... 1
- Added TI Design ... 1
- Changed Shutdown Protection *Features* bullet: removed *Integrated* ... 1
- Changed *Packages* Features bullet ... 1
- Added VSON row to *Device Information* table ... 1
- Added DRB package to *Pin Configuration and Functions* section ... 4
- Changed *Pin Functions* table: changed EN (changed $V_{EN} \le V_{EN(low)}$) and FB (deleted *control-loop* from first sentence) pin descriptions ... 4
- Added DRB column to *Thermal Information* table ... 6
- Changed 35°C to 45°C in *Thermal Protection* section ... 13
- Changed T_J value for disabled mode in Table 1 to match *Electrical Characteristics* table ... 13
- Changed first sentence of *Application Information* section ... 14
- Changed first sentence of *Post DC-DC Converter Filtering* section ... 15
- Changed Equation 3 ... 17
- Changed *1.27 kΩ* to *100 kΩ* in description of R_2 setting in the *Detailed Design Procedure* section ... 17
- Added third paragraph and Figure 36 to *Power Dissipation* section ... 20
- Changed capacitor size value in footnote of Figure 37 ... 21

Changes from Revision C (December 2013) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed 9th bullet in *Features* list ... 1
- Removed pin drawing from front page of data sheet ... 1
- Revised *Thermal Information* table values ... 6

- Added statement about typical value measurement temperature to *Electrical Characteristics* conditions 6
- Added footnote to *Internal reference* specification 6
- Added *Feedback voltage (V_{FB})* parameter to *Electrical Characteristics* 6
- Changed *Line regulation* typical specification from 0.11 to 0.086 %V_{OUT} 6
- Changed *Ground current* typical specification for I_{OUT} = 0 mA from 61 to 49 µA 6
- Changed C_{BYP} to C_{FF} throughout data sheet 6
- Changed footnote in *Electrical Characteristics* describing C_{FF} (C_{BYP}) capacitor 6
- Added statement about typical value measurement temperature to *Typical Characteristics* conditions 7
- Changed Figure 1 to show correct device performance 7
- Changed Figure 14; changed C_{BYP} to C_{FF} 8
- Changed Figure 16; changed C_{BYP} to C_{FF} 8
- Changed Figure 18; changed C_{BYP} to C_{FF} 8
- Moved Figure 25, Figure 26, and Figure 27 to end of *Typical Characteristics* section 11
- Changed Equation 1; corrected notation on $C_{NR/SS}$ 12
- Changed Equation 2 14
- Changed paragraph 1 of *Noise Reduction and Feed-Forward Capacitor Requirements* 14
- Changed Figure 29; changed C_{BYP} to C_{FF} 16

Changes from Revision B (January 2010) to Revision C **Page**

- Changed V_{REF} parameter typical specification in *Electrical Characteristics* table 6

Changes from Revision A (September 2010) to Revision B **Page**

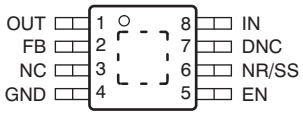
- Changed HBM max value from 500V to 1500V 5

Changes from Original (August 2010) to Revision A **Page**

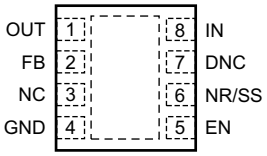
- Revised *Features* list 1
- Changed *Description* text (paragraph 1) to remove description of maximum load 1
- Changed description of NC pin (pin 3) in *Pin Descriptions* table 4
- Revised *shutdown supply current, feedback current,* and *enable current* specifications; rounded typical performance values 6
- Updated Figure 1 to show correct device performance 7
- Revised *Functional Block Diagram* for clarification 12

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP PowerPAD
Top View



DRB Package
VSON-8
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DNC	7	—	Do not connect. Do not route this pin to any electrical net, not even GND or IN.
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN(high)}$, the regulator is enabled. If $V_{EN} \leq V_{EN(low)}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $V_{EN} \leq V_{IN}$.
FB	2	I	This pin is the input to the error amplifier. FB is used to set the output voltage of the device.
GND	4	—	Ground
IN	8	I	Input supply
NC	3	—	Not internally connected. This pin can either be left open or tied to GND.
NR/SS	6	—	Noise-reduction pin. Connecting an external capacitor to this pin bypasses noise generated by the internal band gap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.
OUT	1	O	Regulator output. A capacitor ≥ 2.2 µF must be tied from this pin to ground to ensure stability.
PowerPAD		—	Must either be left open or tied to ground. Solder to the printed-circuit-board (PCB) plane to enhance thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	36	V
	OUT pin to GND pin	–0.3	33	V
	OUT pin to IN pin	–36	0.3	V
	FB pin to GND pin	–0.3	2	V
	FB pin to IN pin	–36	0.3	V
	EN pin to IN pin	–36	0.3	V
	EN pin to GND pin	–0.3	36	V
	NR/SS pin to IN pin	–36	0.3	V
	NR/SS pin to GND pin	–0.3	2	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	3		35	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Output voltage	V_{FB}		33	V
I_{OUT}	Output current	0		150	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	2.2	10		µF
C_{OUT}	Output capacitor	2.2	10		µF
C_{NR}	Noise reduction capacitor	0	10		nF
C_{FF}	Feed-forward capacitor	0	10		nF
R_2	Lower feedback resistor			237	kΩ

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A49		UNIT
		DGN (HVSSOP PowerPAD)	DRB (VSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	47.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53	55.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	13.5	7.0	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		35	V
V_{REF}	Internal reference[1]	T_J = 25°C, $V_{NR/SS}$ = V_{REF}	1.176	1.188	1.212	V
V_{FB}	Feedback voltage			1.185		V
V_{OUT}	Output voltage range[2]	V_{IN} ≥ $V_{OUT(nom)}$ + 1 V	V_{REF}		33	V
	Nominal accuracy	T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V	–1.5		1.5	$\%V_{OUT}$
	Overall accuracy	$V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 35 V, 1 mA ≤ I_{OUT} ≤ 150 mA	–2.5		2.5	$\%V_{OUT}$
$\frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}}$	Line regulation	T_J = 25°C, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 35 V		0.086		$\%V_{OUT}$
$\frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}}$	Load regulation	T_J = 25°C, 1 mA ≤ I_{OUT} ≤ 150 mA		0.04		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 100 mA		260		mV
		V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 150 mA		333	600	mV
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(nom)}$	220	309	500	mA
I_{GND}	Ground current	I_{OUT} = 0 mA		49	100	µA
		I_{OUT} = 100 mA		800		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		0.8	3	µA
I_{FB}	Feedback current[3]			3	100	nA
I_{EN}	Enable current	V_{EN} = V_{IN} = $V_{OUT(nom)}$ + 1 V		0.02	1	µA
		V_{EN} = V_{IN} = 35 V		0.2	1	µA
$V_{EN(high)}$	Enable high-level voltage		2.1		V_{IN}	V
$V_{EN(low)}$	Enable low-level voltage		0		0.4	V
V_n	Output noise voltage	V_{IN} = 3 V, $V_{OUT(nom)}$ = V_{REF}, C_{OUT} = 10 µF, $C_{NR/SS}$ = 10 nF, BW = 10 Hz to 100 kHz		15.4		μV_{RMS}
		V_{IN} = 6.2 V, $V_{OUT(nom)}$ = 5 V, C_{OUT} = 10 µF, $C_{NR/SS}$ = C_{FF}[4] = 10 nF, BW = 10 Hz to 100 kHz		21.15		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 6.2 V, $V_{OUT(nom)}$ = 5 V, C_{OUT} = 10 µF, $C_{NR/SS}$ = C_{FF}[4] = 10 nF, f = 120 Hz		72		dB
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_J	Operating junction temperature		–40		125	°C

(1) V_{REF} is measured at the NR/SS pin.
(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 µA is required.
(3) I_{FB} > 0 flows out of the device.
(4) C_{FF} refers to a feed-forward capacitor connected to the FB and OUT pins.

6.6 Typical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

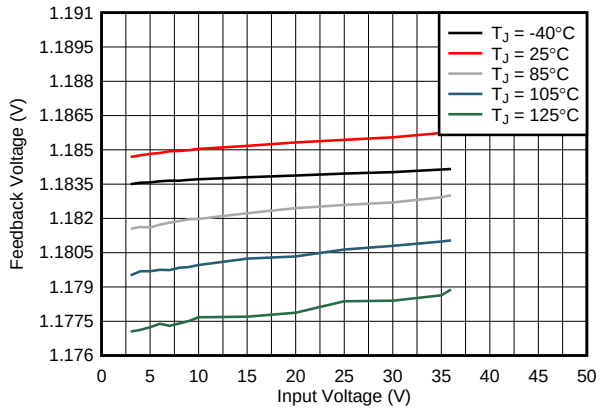


Figure 1. Feedback Voltage vs Input Voltage

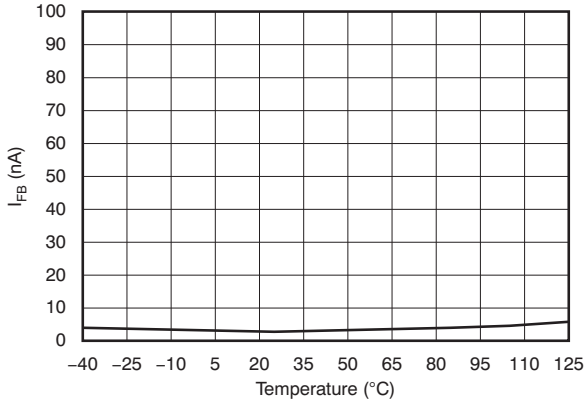


Figure 2. Feedback Current vs Temperature

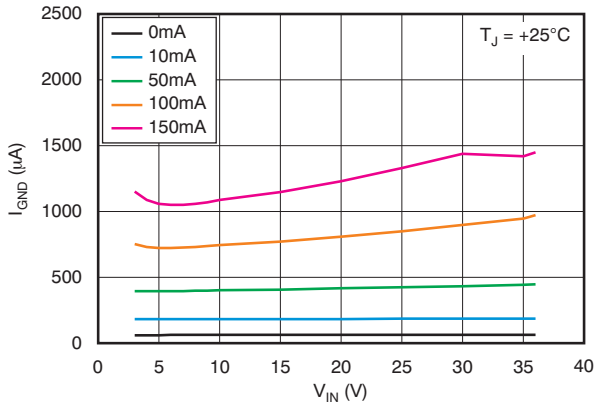


Figure 3. Ground Current vs Input Voltage

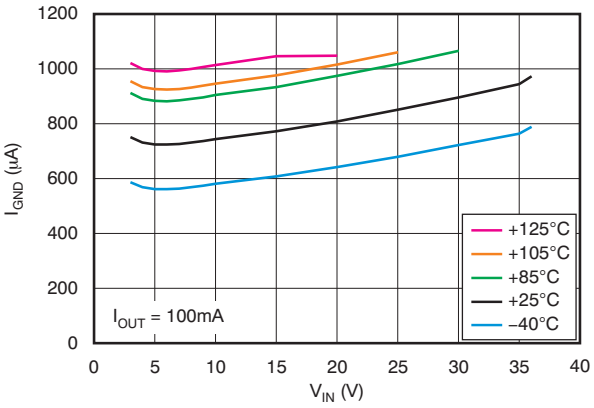


Figure 4. Ground Current vs Input Voltage

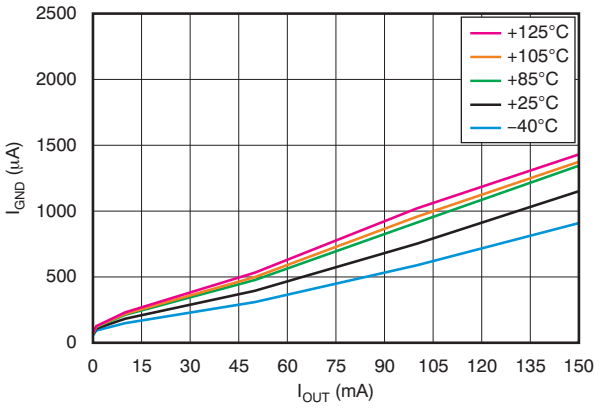


Figure 5. Ground Current vs Output Current

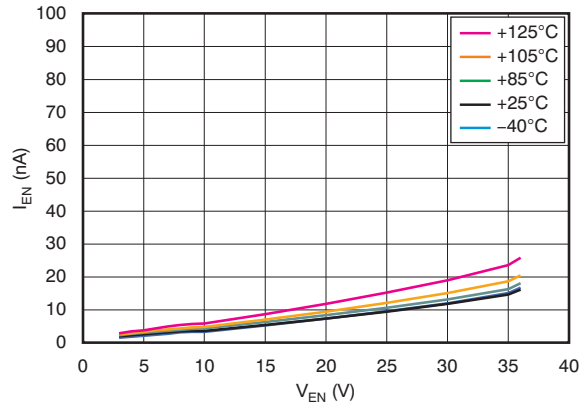


Figure 6. Enable Current vs Enable Voltage

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

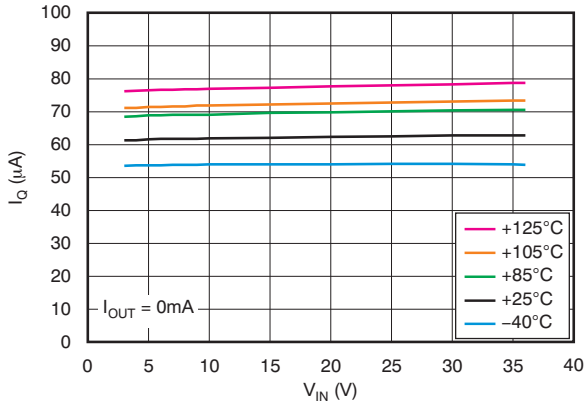


Figure 7. Quiescent Current vs Input Voltage

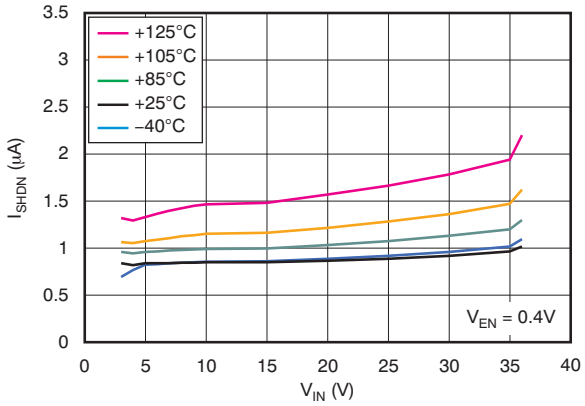


Figure 8. Shutdown Current vs Input Voltage

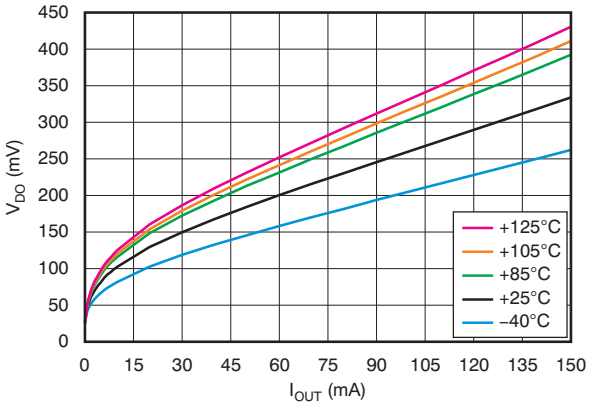


Figure 9. Dropout Voltage vs Output Current

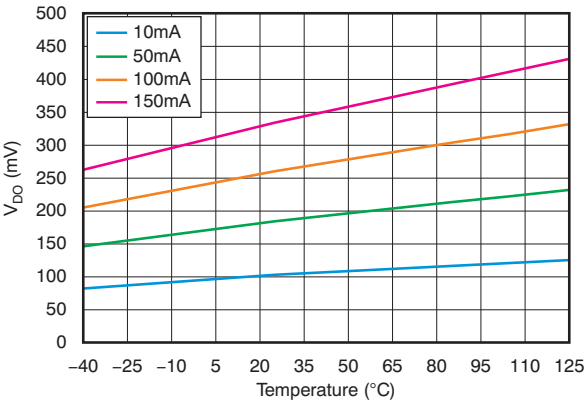


Figure 10. Dropout Voltage vs Temperature

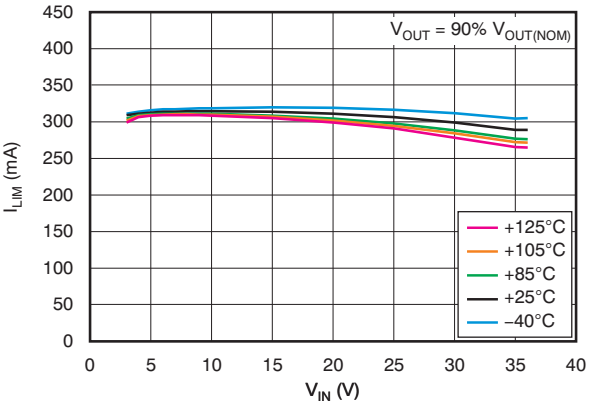


Figure 11. Current Limit vs Input Voltage

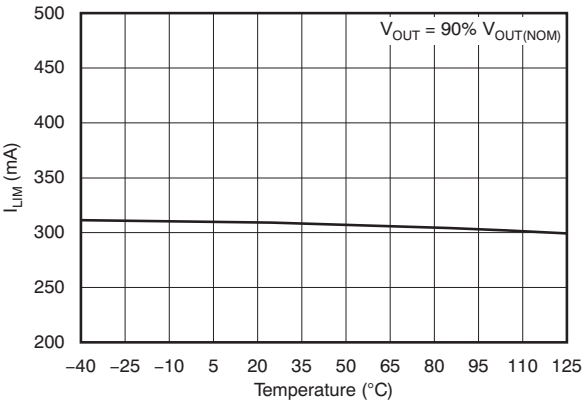


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

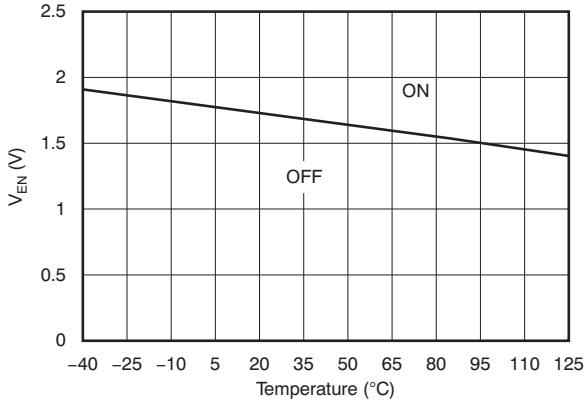


Figure 13. Enable Threshold Voltage vs Temperature

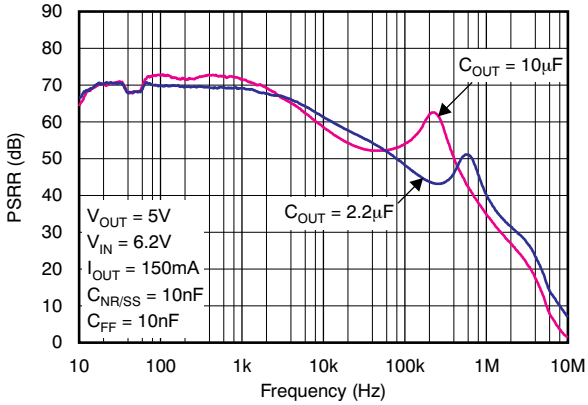


Figure 14. Power-Supply Rejection Ratio vs C_{OUT}

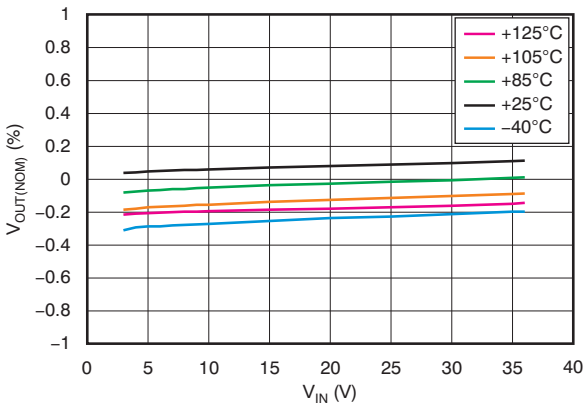


Figure 15. Line Regulation

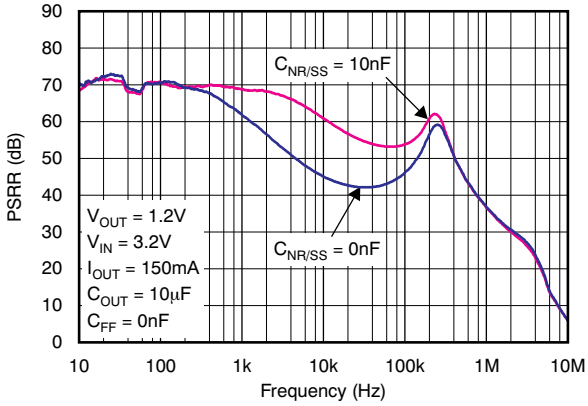


Figure 16. Power-Supply Rejection Ratio vs $C_{NR/SS}$

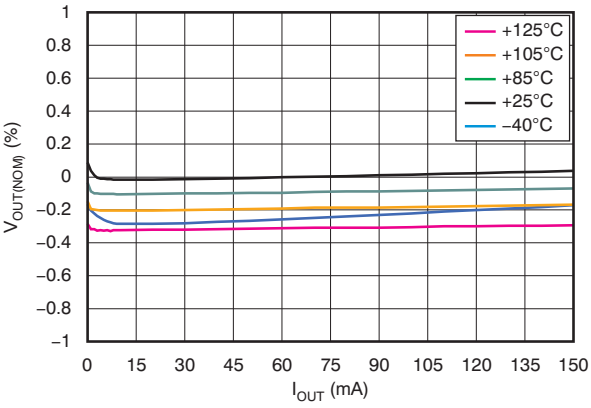


Figure 17. Load Regulation

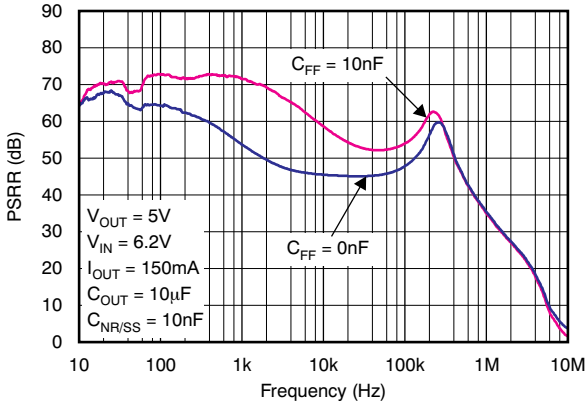


Figure 18. Power-Supply Rejection Ratio vs C_{FF}

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

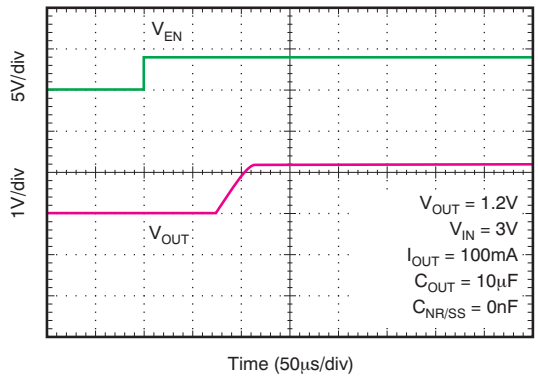


Figure 19. Capacitor-Programmable Soft-Start

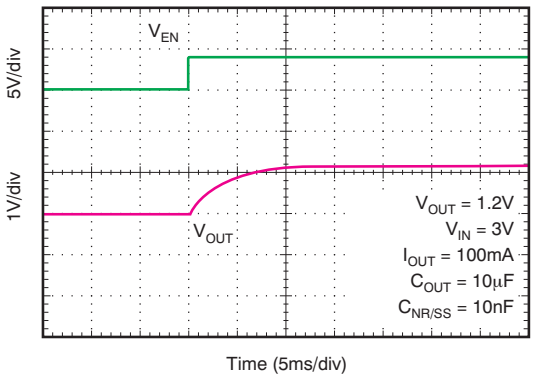


Figure 20. Capacitor-Programmable Soft-Start

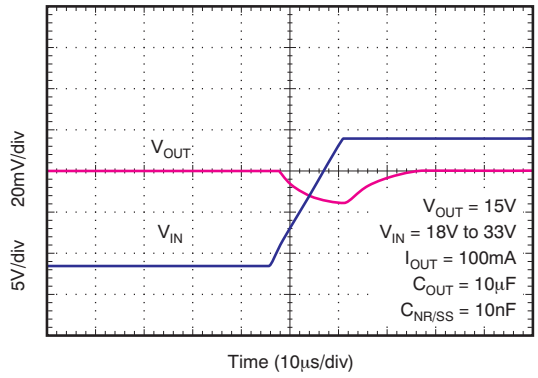


Figure 21. Line Transient Response

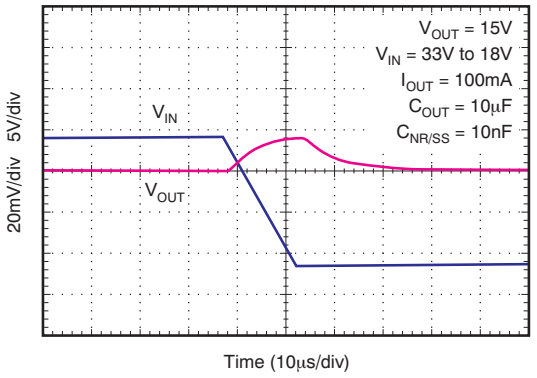


Figure 22. Line Transient Response

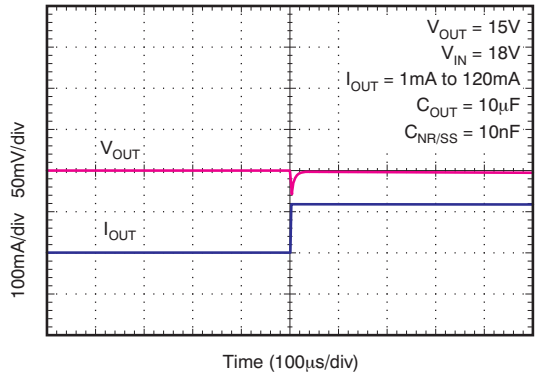


Figure 23. Load Transient Response

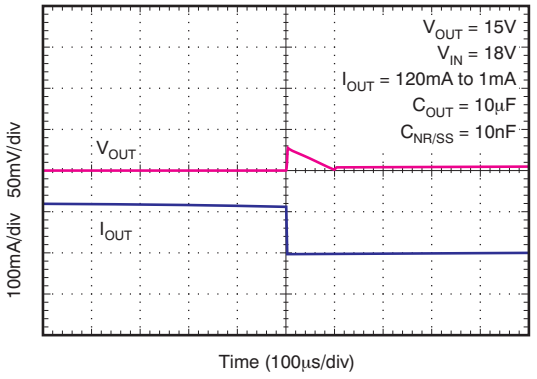
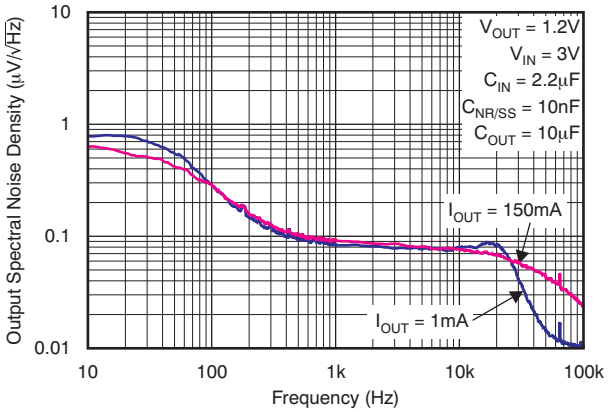


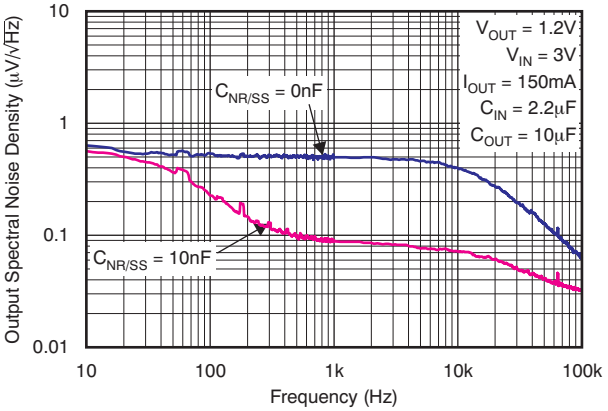
Figure 24. Load Transient Response

7 Parameter Measurement Information



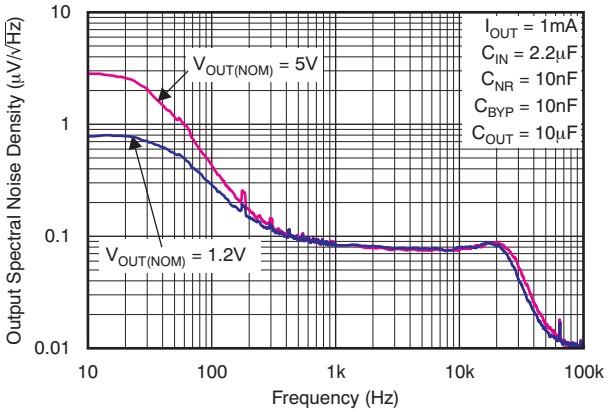
I_{OUT}	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
1mA	15.44	14.14
150mA	17.27	16.46

Figure 25. Output Spectral Noise Density vs Output Current



$C_{NR/SS}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
0nF	69.04	67.87
10nF	16.58	15.86

Figure 26. Output Spectral Noise Density vs $C_{NR/SS}$



$V_{OUT(NOM)}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
5V	21.15	14.74
1.2V	15.44	14.14

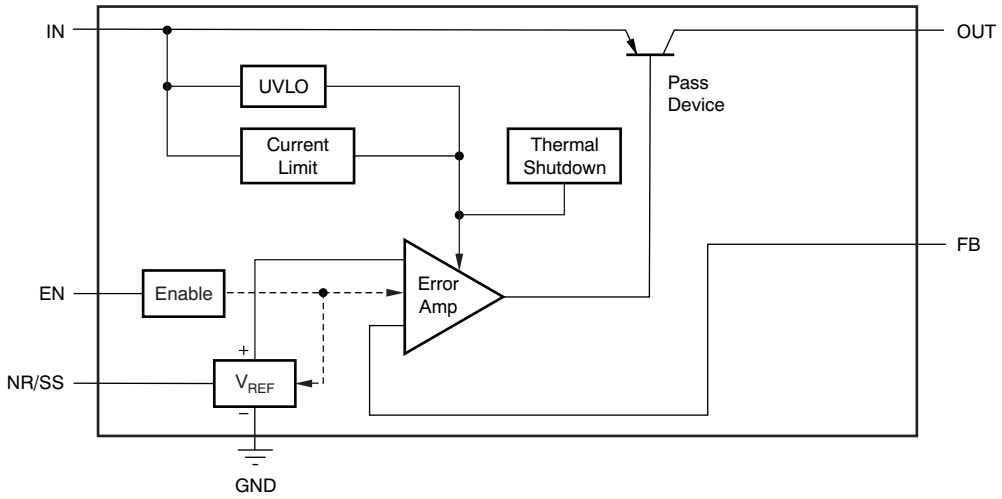
Figure 27. Output Spectral Noise Density vs $V_{OUT(NOM)}$

8 Detailed Description

8.1 Overview

The TPS7A49 family of devices are wide V_{IN}, low-noise, 150-mA linear regulators (LDOs). These devices feature an enable pin, programmable soft-start, current limiting, and thermal protection circuitry that allow the device to be used in a wide variety of applications. As bipolar-based devices, the TPS7A49 family are ideal for high-accuracy, high-precision applications at higher voltages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A49 family helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (309 mA, typical), and is largely independent of output voltage. For reliable operation, the device does not operate in current limit for extended periods of time.

8.3.2 Programmable Soft-Start

The NR capacitor also functions as a soft-start capacitor to slow down the rise time of the output. The rise time of the output when using an NR capacitor is governed by Equation 1. In Equation 1, t_{SS} is the soft-start time in milliseconds, and $C_{NR/SS}$ is the capacitance at the NR pin in nanofarads.

$$t_{SS}\ (ms) = 1.4 \times C_{NR/SS}\ (nF) \quad (1)$$

8.3.3 Enable Pin Operation

The TPS7A49 provides an enable feature (EN) that turns on the regulator when $V_{EN} > V_{EN(high)}$ and disables the device when $V_{EN} < V_{EN(low)}$.

8.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Feature Description (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 45°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A49 is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heatsinking. Continuously running the TPS7A49 into thermal shutdown degrades device reliability.

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 170°C$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7A49 devices belongs to a family of linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage range. These features, combined with a high thermal-performance HVSSOP-8 with a PowerPAD package make this device ideal for high-performance analog applications.

9.1.1 Adjustable Operation

The TPS7A4901 device has an output voltage range of $V_{FB(nom)}$ to 33 V. The nominal output voltage of the device is set by two external resistors; see Figure 29.

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 2. To ensure stability under no-load conditions, this resistive network must provide a current greater than or equal to 5 µA.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{FB(nom)}} - 1 \right), \quad \text{where } \frac{V_{FB(nom)}}{R_2} > 5\ \mu A \tag{2}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions resulting from the feedback pin current and use 0.1% tolerance resistors.

9.1.2 Capacitor Recommendations

Use low-equivalent series resistance (ESR) capacitors for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, whereas ceramic X5R capacitors are more cost-effective and are available in higher values.

High ESR capacitors can degrade PSRR. To ensure stability, maximum ESR must be less than 200 mΩ.

9.1.3 Input and Output Capacitor Requirements

The TPS7A49 family of positive, high-voltage linear regulators achieve stability with a minimum input and output capacitance of 2.2 µF; however, TI highly recommends using a 10-µF capacitor to maximize ac performance. Place the input and output capacitors as close to the pin as possible, on the same side as the device; do not use vias between the capacitor and the pin.

9.1.4 Noise-Reduction and Feed-Forward Capacitor Requirements

Although noise-reduction and feed-forward capacitors ($C_{NR/SS}$ and C_{FF}, respectively) are not needed to achieve stability, TI highly recommends using 10-nF capacitors to minimize noise and maximize ac performance. $C_{NR/SS}$ is a noise-reduction capacitor because it filters out noise from the band gap. For more information on C_{FF}, refer to application report, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* (SBVA042). This application report explains the advantages of using C_{FF} (also known as C_{BYP}), and the problems that can occur when using this capacitor.

9.1.5 Maximum AC Performance

To maximize noise and PSRR performance, TI recommends including 10 µF or higher input and output capacitors, and 10-nF noise-reduction and bypass capacitors; see Figure 29. The solution illustrated in Figure 29 delivers minimum noise levels of 15.4 μV_{RMS} and power-supply rejection levels above 52 dB from 10 Hz to 400 kHz; see Figure 18 and Figure 25.

Application Information (continued)

9.1.6 Output Noise

The TPS7A49 provides low output noise when a noise reduction capacitor ($C_{NR/SS}$) is used.

The noise-reduction capacitor serves as a filter for the internal reference. By using a 10-nF noise reduction capacitor, the output noise is reduced by approximately 75% (from 69 μV_{RMS} to 17 μV_{RMS}); see Figure 26.

The low output voltage noise of the TPS7A49 makes the device an ideal solution for powering noise-sensitive circuitry.

9.1.7 Post DC-DC Converter Filtering

Most of the time, the voltage rails available in a system do not match the voltage requirements for the system. These rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. These converters offer high efficiency with minimum heat generation, but have one primary disadvantage: these converters introduce a high-frequency component (and the associated harmonics) in addition to the dc output signal.

If not filtered properly, this high-frequency component degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A49 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes the device ideal for post dc-dc converter filtering, as shown in Figure 28. TI highly recommends using the maximum performance schematic illustrated in Figure 29. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR; see Figure 18.

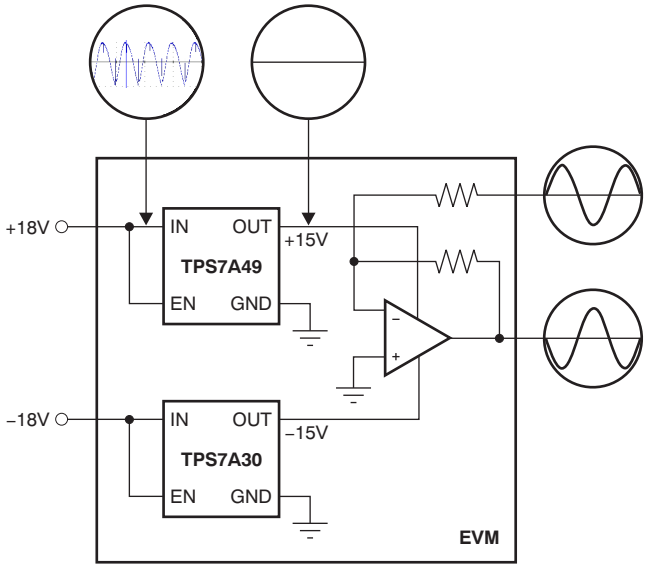


Figure 28. Post DC-DC Converter Regulation to High-Performance Analog Circuitry

9.1.8 Power-Supply Rejection

The 10-nF noise-reduction capacitor greatly improves the TPS7A49 power-supply rejection, achieving up to 15 dB of additional power-supply rejection for frequencies between 110 Hz and 200 kHz.

Additionally, ac performance can be maximized by adding a 10-nF bypass capacitor (C_{FF}) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies for the band from 10 Hz to 200 kHz; see Figure 18.

The very high power-supply rejection of the TPS7A49 makes the device a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACS, and audio amplifiers.

Application Information (continued)

9.1.9 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response.

9.1.10 Audio Applications

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20 Hz to 20 kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very high power-supply rejection ratio (> 55 dB) and low noise at the audio band of the TPS7A49 maximize device performance for audio applications; see Figure 18.

9.1.11 Power for Precision Analog

One of the primary TPS7A49 applications is to provide ultralow-noise voltage rails to high-performance analog circuitry to maximize system accuracy and precision.

The TPS7A49 family of positive high-voltage linear regulators, in conjunction with its negative counterpart (the TPS7A30xx family of negative high-voltage linear regulators), provides ultralow noise, and positive and negative voltage rails for high-performance analog circuitry (such as operational amplifiers, ADCs, DACs, and audio amplifiers).

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range and maximize system accuracy.

9.2 Typical Application

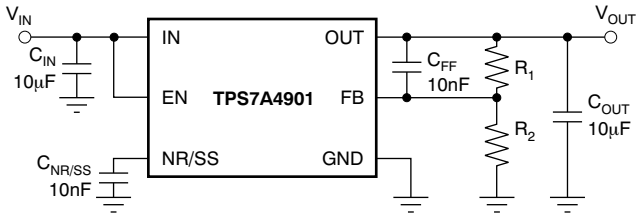


Figure 29. Adjustable Operation for Maximum AC Performance

9.2.1 Design Requirements

The maximum design goals are as follows:

- V_{IN} = 3 V
- V_{OUT} = 1.2 V
- I_{OUT} = 150 mA

The design optimizes transient response and meets a start-up time of 14 ms with a start-up dominated by the soft-start feature. The input supply comes from a supply on the same printed circuit board (PCB). The design circuit is shown in Figure 29.

The design space consists of C_{IN}, C_{OUT}, $C_{NR/SS}$, R_1, and R_2, at $T_{A(max)}$ = 75°C.

9.2.2 Detailed Design Procedure

The first step when designing with a linear regulator is to examine the maximum load current, along with the input and output voltage requirements, to determine if the device thermal and dropout voltage requirements can be met. At 150 mA, the input dropout voltage of the TPS7A49 family is a maximum of 600 mV over temperature; therefore, the dropout headroom of 1.8 V is sufficient for operation over both input and output voltage accuracy. Dropout headroom is calculated as $V_{IN} - V_{OUT} - V_{DO(max)}$, and for optimal performance must be at least 1 V. $V_{DO(max)}$ is the maximum dropout allowed, given worst-case load conditions.

Typical Application (continued)

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output, multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is (3 V – 1.2 V), resulting in $V_{IN} – V_{OUT}$ = 1.8 V. The power dissipated in the pass element is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 0.2724 W, and is calculated as Equation 3:

$$P_D = (V_{IN} – V_{OUT}) (I_{MAX}) + (V_{IN}) (I_Q) \quad (3)$$

When the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. This calculation gives the worst-case junction temperature; good thermal design can significantly reduce this number. For thermal resistance information, refer to the *Power Dissipation* section. For this example, using the DGN package, the maximum junction temperature rise is calculated to be 17.3°C. The maximum junction temperature rise is calculated by adding the junction temperature rise to the maximum ambient temperature, which is 75°C for this example. For this example, calculate the maximum junction temperature to be 103.8°C. Keep in mind that the maximum junction temperate must be below 92.3°C for reliable device operation. Additional ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature.

Use the following guidelines to select the values for the remaining components:

To ensure stability under no-load conditions, the current through the resistor network must be greater than 5 µA, as shown in Equation 4:

$$\frac{V_{REF(max)}}{R_2} > 5\mu A \rightarrow R_2 < 242.4\ k\Omega \quad (4)$$

Next, set the value of R_2 to 100 kΩ for a standard 1% value resistor and use Equation 5 to calculate the value of R_1.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB(nom)}} - 1\right) = 100\ k\Omega\left(\frac{1.2\ V}{1.185\ V} - 1\right) = 1.265\ k\Omega \quad (5)$$

For R_1, select a standard, 1%, 68.1-kΩ resistor.

Use Equation 6 to calculate the start-up time, t_{SS}.

$$t_{SS}\ (ms) = 1.4 \times C_{NR/SS} = 14\ ms$$

$$C_{SS} = 10\ nF \quad (6)$$

For the soft-start to dominate the start-up conditions, place the start-up time as a result of the current limit at two decades below the soft-start time (at 140 µs). C_{OUT} must be at least 2.2 µF for stability, as shown in Equation 7 and Equation 8:

$$t_{SS(CL)} = V_{OUT}\left(\frac{C_{OUT}}{I_{CL(max)}}\right) \quad (7)$$

$$C_{OUT(max)} = t_{SS(CL)}\left(\frac{I_{CL(max)}}{V_{OUT}}\right) = 140\ \mu s \times \frac{500\ mA}{2\ V} = 35\ \mu F \quad (8)$$

For C_{IN}, assume that the 3-V supply has some inductance, and is placed several inches away from the PCB. For this case, select a 2.2-µF ceramic input capacitor to ensure that the input impedance is negligible to the LDO control loop and to keep the physical size and cost of the capacitor low; this component is a common-value capacitor.

For better PSRR for this design, use a 10-µF input and output capacitor. To reduce the peaks from transients but slow down the recovery time, increase the output capacitor size or add additional output capacitors.

Typical Application (continued)

9.2.3 Application Curves

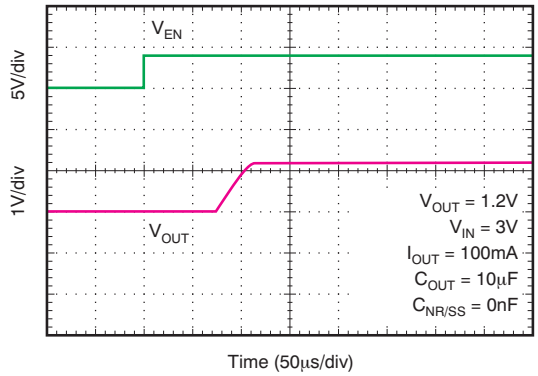


Figure 30. Capacitor-Programmable Soft-Start

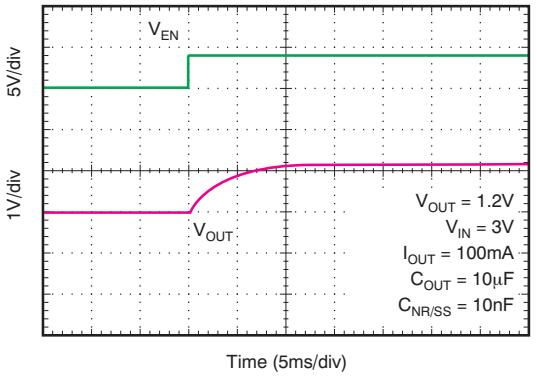


Figure 31. Capacitor-Programmable Soft-Start

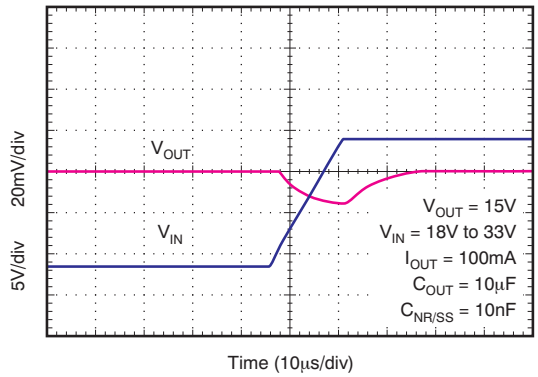


Figure 32. Line Transient Response

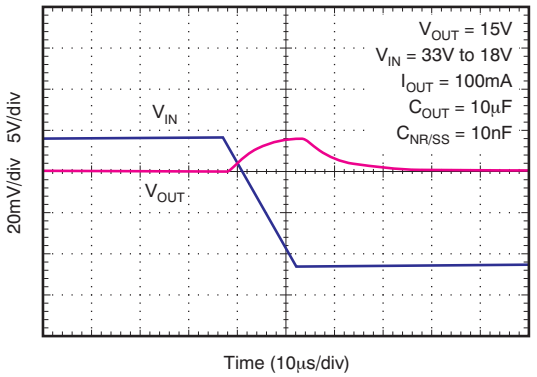


Figure 33. Line Transient Response

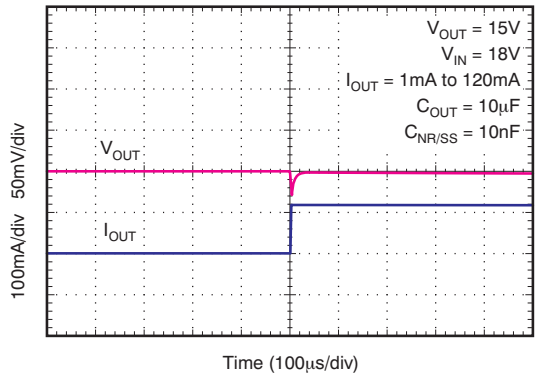


Figure 34. Load Transient Response

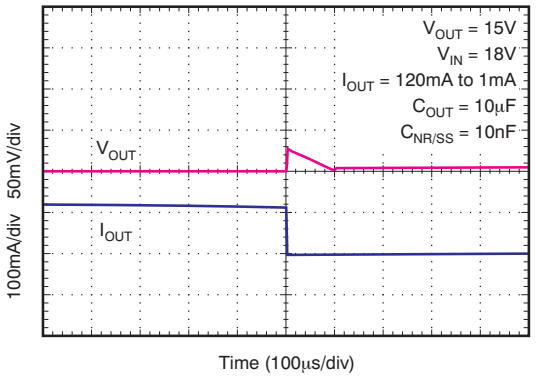


Figure 35. Load Transient Response

9.3 Do's and Don'ts

Place at least one low-ESR, 2.2-µF capacitor as close as possible to both the IN and OUT pins of the regulator to the GND pin.

Provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the enable (EN) pin.

Do not resistively or inductively load the NR/SS pin.

10 Power Supply Recommendations

The input supply for the LDO must be within its recommended operating conditions (that is, between 3 V to 35 V). The input voltage must provide adequate headroom in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

The input and output supplies must also be bypassed with at least a 2.2-µF capacitor located near the input and output pins. No other components must be located between these capacitors and the pins.

11 Layout

11.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low-ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin must be tied directly to the PowerPAD under the device. Connect the PowerPAD to any internal PCB ground planes using multiple vias directly under the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, and C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can negatively affect system performance, and can even cause instability.

11.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane star-connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

11.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 9:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (9)$$

Layout Guidelines (continued)

Figure 36 shows the maximum ambient temperature versus the power dissipation of the TPS7A49. Figure 36 assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS7A49 does not operate above a junction temperature of 125°C.

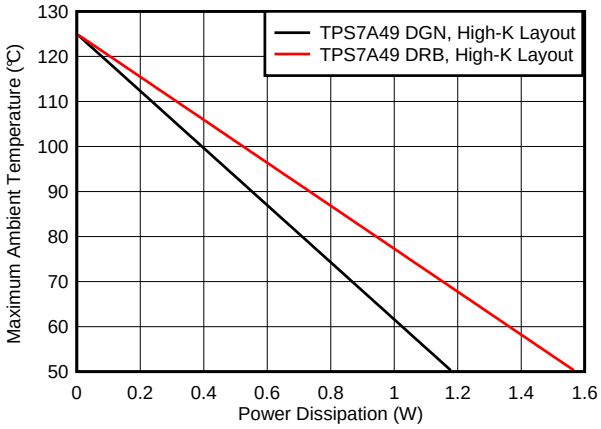


Figure 36. Maximum Ambient Temperature vs Device Power Dissipation

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}; see the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 10.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D \tag{10}$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{10}$$

where

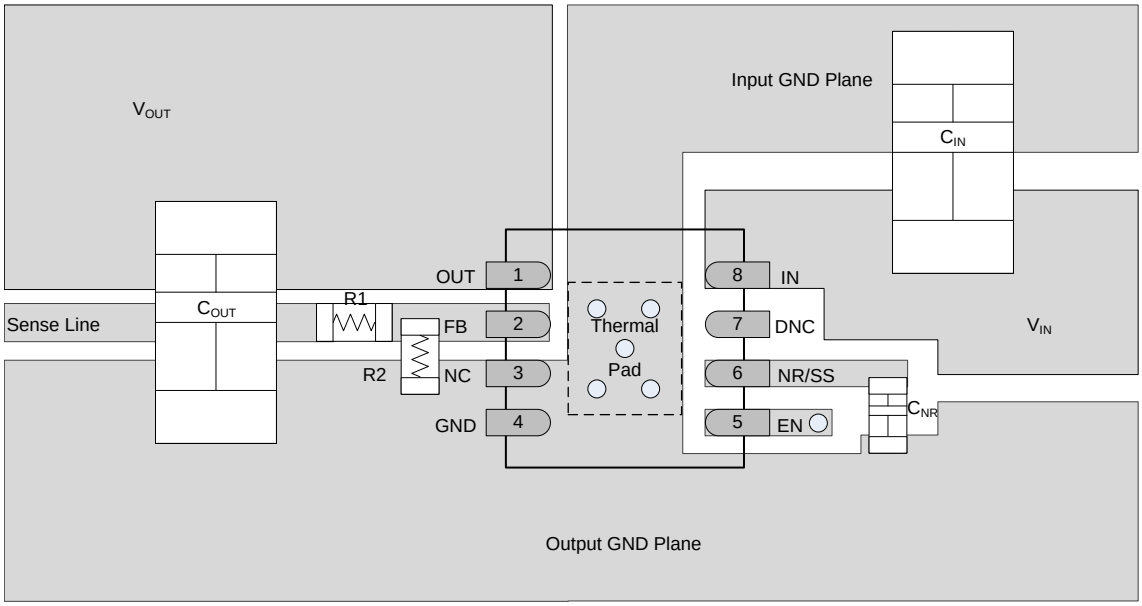
- P_D is the power dissipation given by Equation 9,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11.2 Layout Example



NOTE: C_{IN} and C_{OUT} are size 1206 capacitors and C_{NR}, R1, and R2 are size 0402.

Figure 37. PCB Layout Example

11.3 Package Mounting

Solder pad footprint recommendations for the TPS7A49 are available at the end of this product data sheet and at www.ti.com.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A49. The TPS7A30-49EVM-567 evaluation module (and related user's guide) can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A49 is available through the product folder under *Tools & Software*.

12.1.2 Device Nomenclature

Table 2. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7A49**xxyyyz**	**xx** is the nominal output voltage. An **01** denotes an adjustable voltage version. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

12.2 Documentation Support

12.2.1 Related Documentation

- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042
- *Using New Thermal Metrics*, SBVA025
- *TPS7A30-49EVM-567 User's Guide*, SLVU405

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4901DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DGNT	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

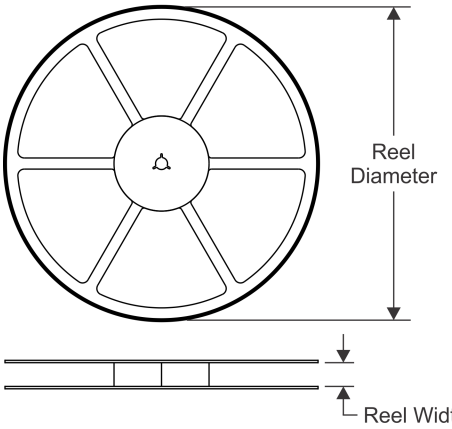
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

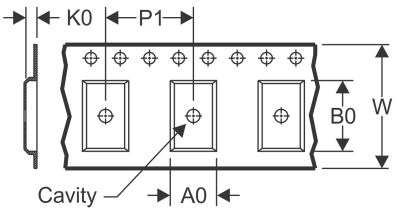
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

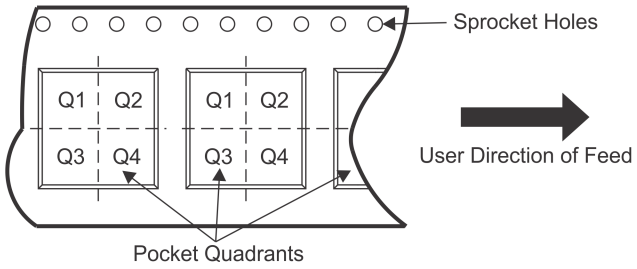


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

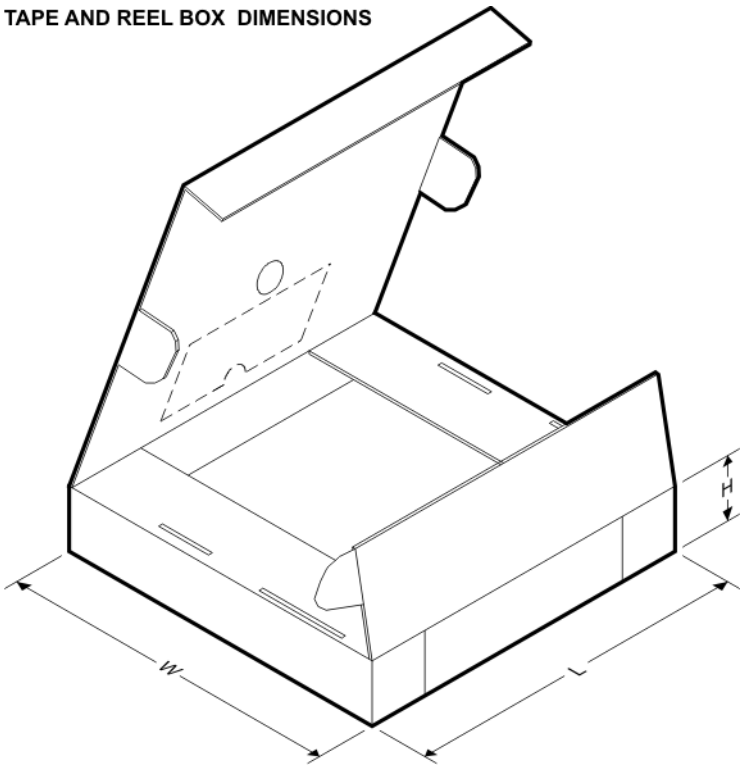
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4901DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A4901DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A4901DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A4901DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4901DGNR	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0
TPS7A4901DGNT	MSOP-PowerPAD	DGN	8	250	210.0	185.0	35.0
TPS7A4901DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS7A4901DRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

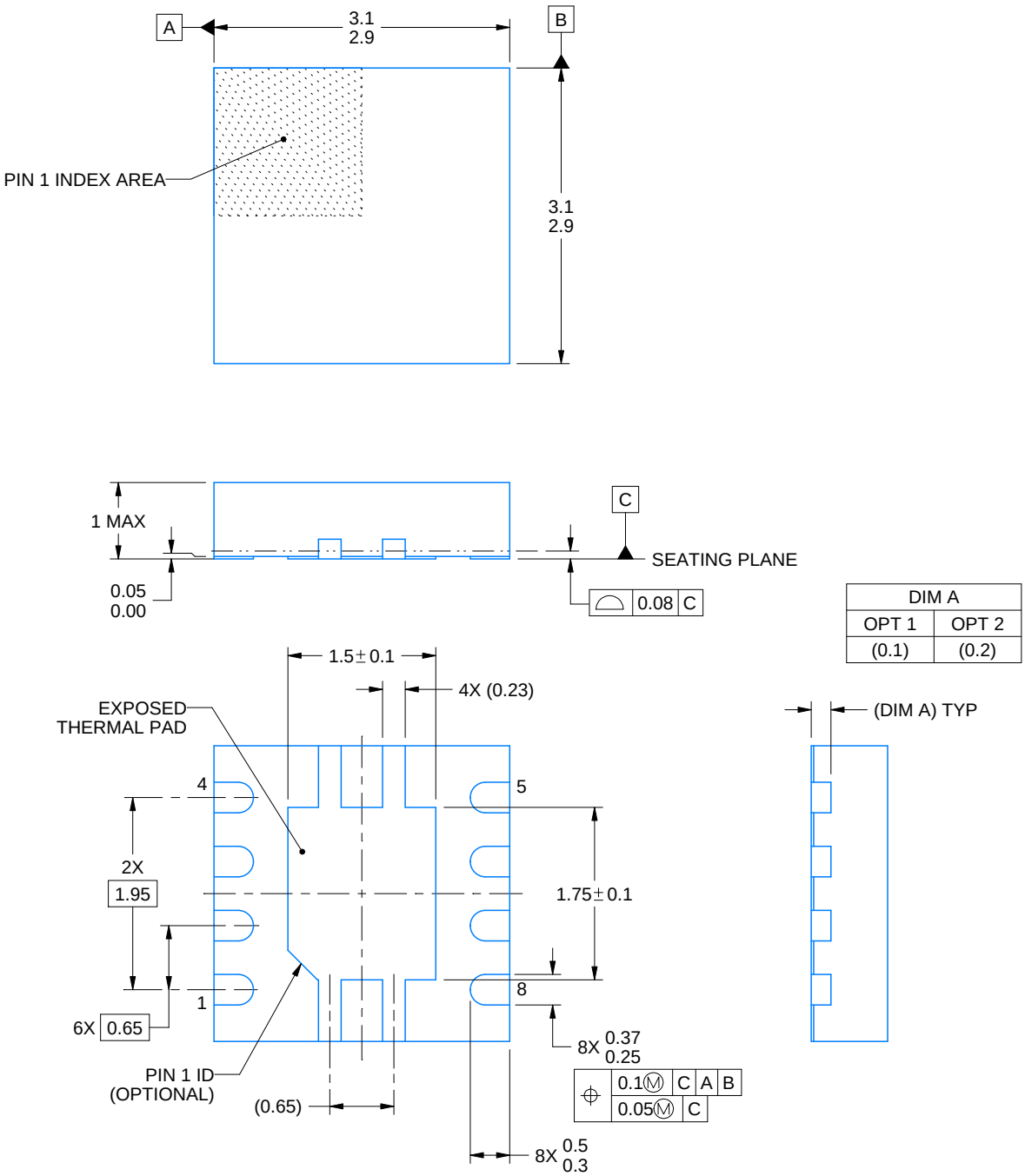
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

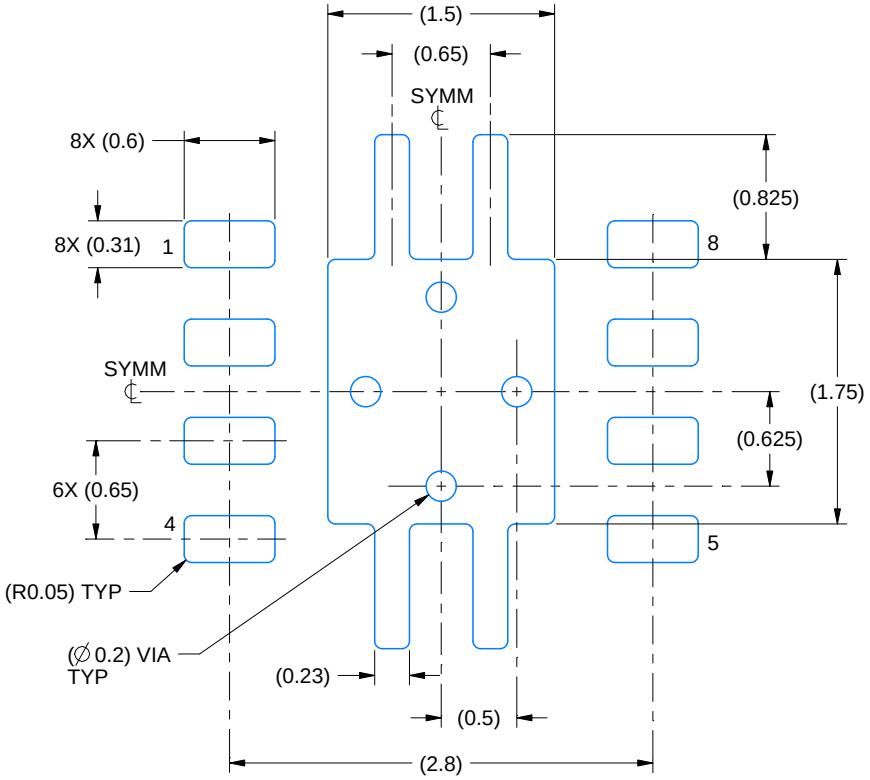
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

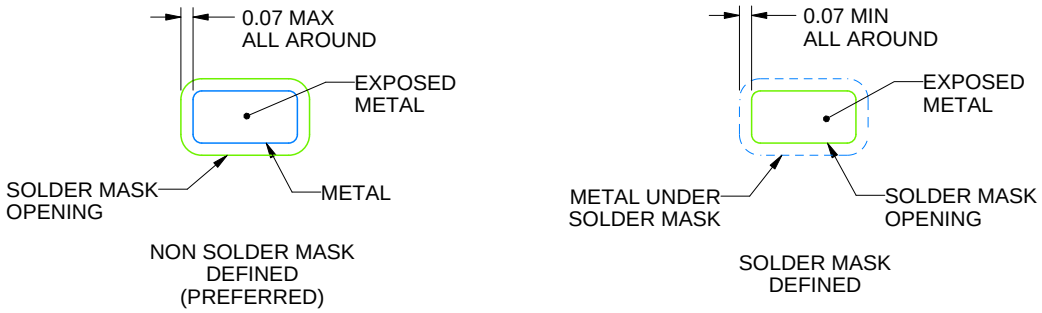
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

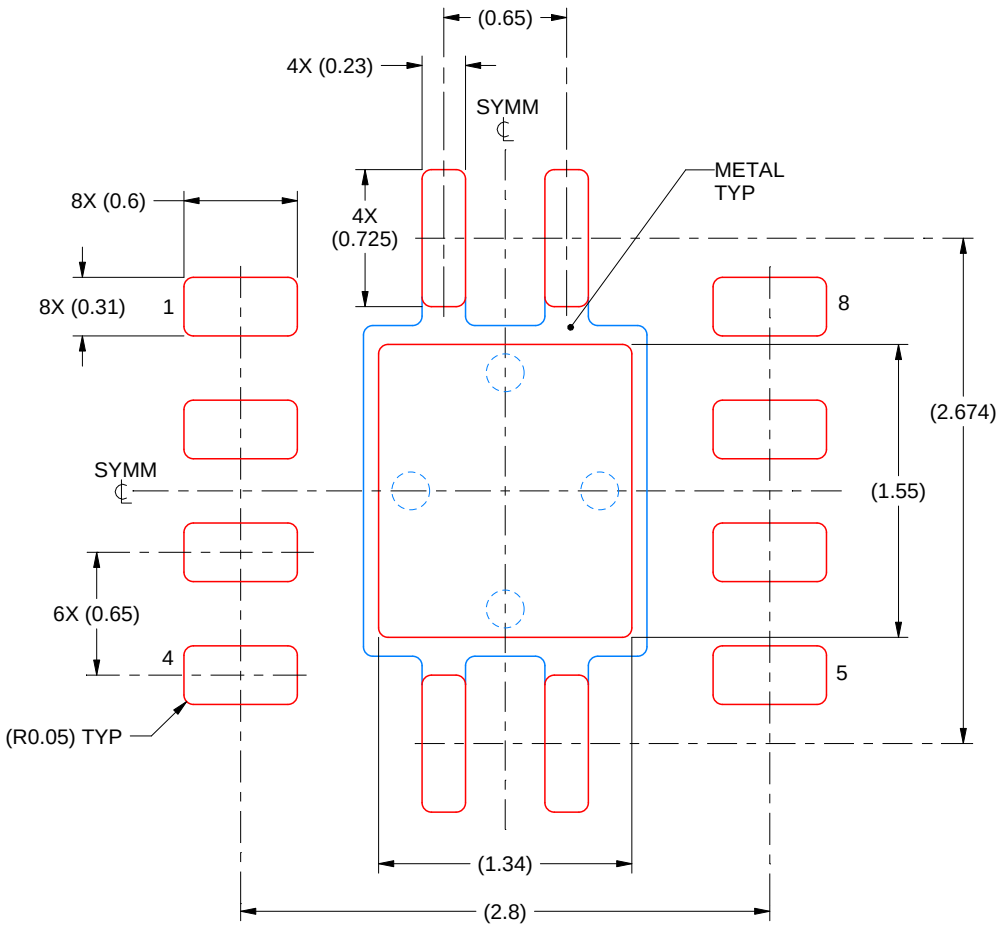


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

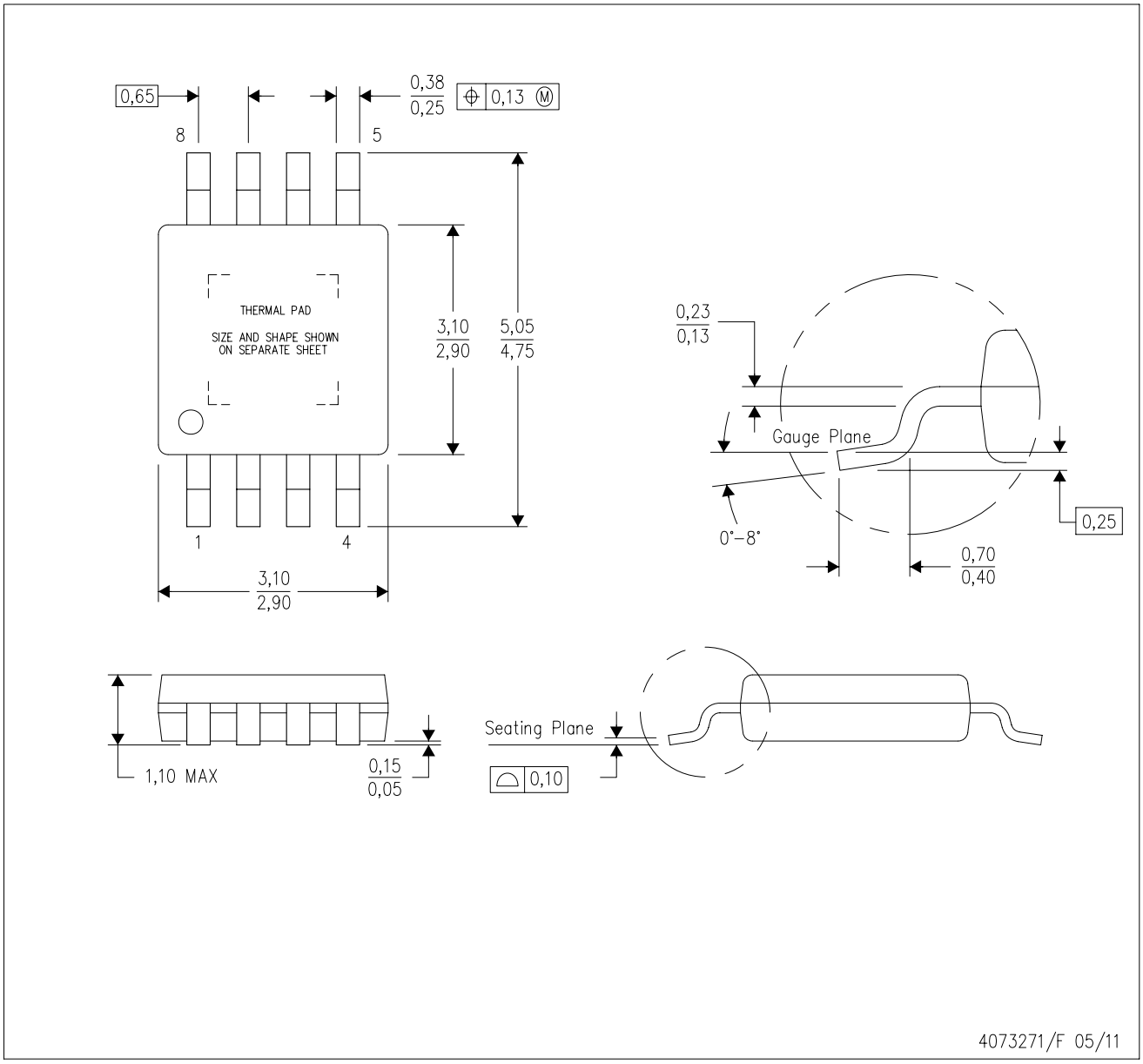
EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

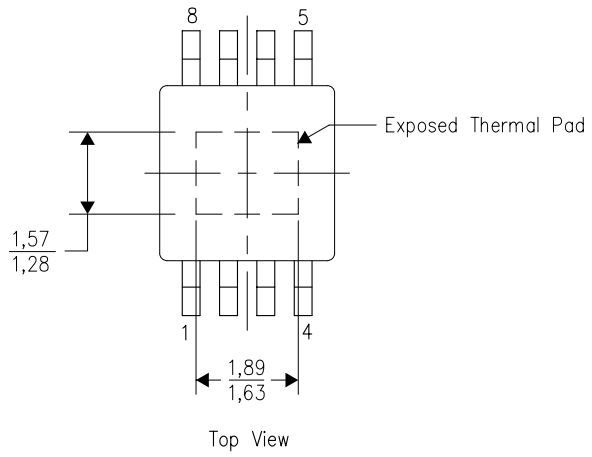
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

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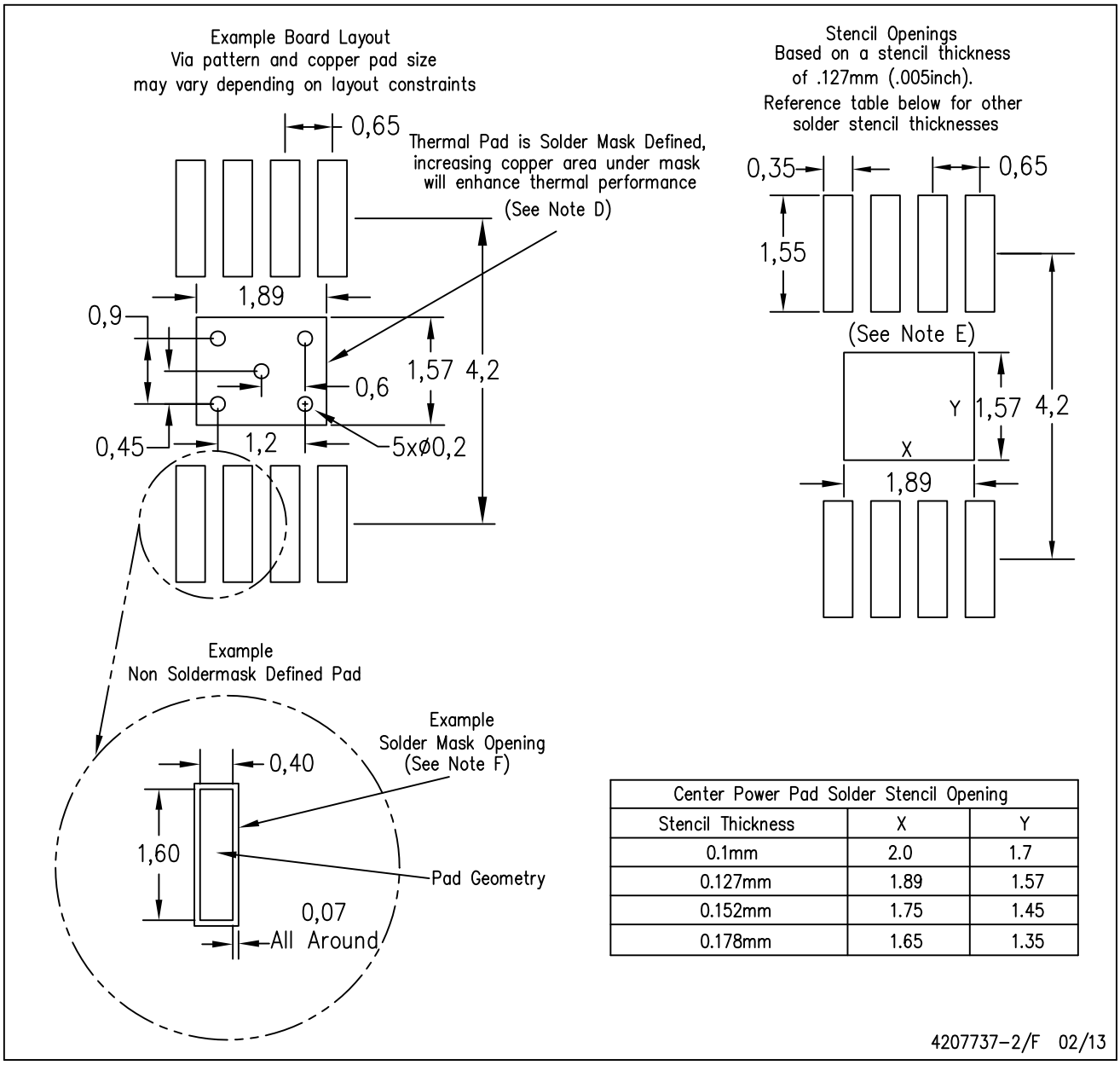
DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TPS7A30 –35-V, –200-mA, Ultralow-Noise, Negative Linear Regulator

1 Features

- Input Voltage Range: –3 V to –35 V
- Noise:
  - 14 μV_{RMS} (20 Hz to 20 kHz)
  - 15.1 μV_{RMS} (10 Hz to 100 kHz)
- Power-Supply Ripple Rejection:
  - 72 dB (120 Hz)
  - ≥ 55 dB (10 Hz to 700 kHz)
- Adjustable Output: –1.18 V to –33 V
- Maximum Output Current: 200 mA
- Dropout Voltage: 216 mV at 100 mA
- Stable with Ceramic Capacitors ≥ 2.2 µF
- CMOS Logic-Level-Compatible Enable Pin
- Built-In, Fixed, Current Limit and Thermal Shutdown Protection
- Packages: 8-Pin HVSSOP PowerPAD™ and 3-mm × 3-mm VSON
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Supply Rails for Operational Amplifiers, DACs, ADCs, and Other High-Precision Analog Circuitry
- Audio
- Post DC-DC Converter Regulation and Ripple Filtering
- Test and Measurement
- RX, TX, and PA Circuitry
- Industrial Instrumentation
- Base Stations and Telecom Infrastructure
- –12-V and –24-V Industrial Buses

3 Description

The TPS7A30 series of devices are negative, high-voltage (–35 V), ultralow-noise (15.1 μV_{RMS}, 72-dB PSRR) linear regulators that can source a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A30 family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A30 family of linear regulators is suitable for post dc-dc converter regulation. By filtering out the output voltage ripple inherent to dc-dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

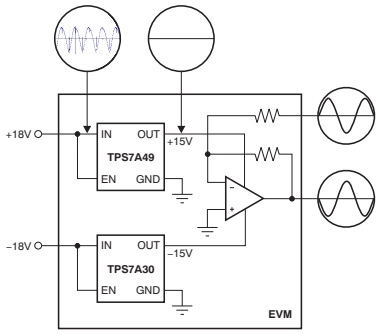
For applications that require positive and negative high-performance rails, consider TI's TPS7A49 family of positive high-voltage, ultralow-noise linear regulators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A30	HVSSOP (8)	3.00 mm × 3.00 mm
	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Post DC-DC Converter Regulation for High-Performance Analog Circuitry



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2015) to Revision D **Page**

- Added DRB package to document ... 1
- Added TI Design ... 1
- Changed *Packages* Features bullet ... 1
- Added VSON row to *Device Information* table ... 1
- Added DRB package to *Pin Configuration and Functions* section ... 4
- Changed EN pin description in *Pin Functions* table: updated voltage symbols ... 4
- Added DRB column to *Thermal Information* table ... 6
- Changed test conditions of last row in $|I_{EN}|$ parameter of *Electrical Characteristics* table ... 7
- Changed title and y-axis of Figure 7 to *Ground Current* ... 9
- Changed y-axis of Figure 11 and Figure 12 to I_Q ... 9
- Changed V_{EN} value of disabled mode in Table 1 ... 16
- Changed first sentence of *Application Information* section ... 17
- Added Table 2 and respective description to *Adjustable Operation* section ... 17
- Deleted third sentence from *Capacitor Recommendations* section ... 17
- Changed third paragraph of *Power for Precision Analog* section ... 19
- Changed description of start-up time in *Design Requirements* section ... 20
- Changed Equation 3 ... 20
- Changed Equation 8 ... 21
- Changed fifth item in *Do's and Don'ts* section ... 23
- Changed Figure 40 footnote ... 25
- Changed 35°C to 45°C in *Thermal Considerations* section ... 26

Changes from Revision B (December 2013) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed document title 1
- Changed *Thermal Information* table; updated values 6
- Deleted *Dissipation Ratings* table 6
- Changed condition statement for *Electrical Characteristics* table 7
- Added footnote about measuring V_{REF} to *Electrical Characteristics* table 7
- Added V_{FB} parameter to *Electrical Characteristics* table 7
- Changed parametric symbol for current limit from I_{LIM} to I_{CL} 7
- Changed C_{BYP} notation to C_{FF} throughout data sheet 7
- Changed condition statement for *Typical Characteristics* 8
- Changed Figure 14; changed notation for C_{BYP} to C_{FF} 9
- Changed Figure 16; changed notation for C_{BYP} to C_{FF} 9
- Changed Figure 18; changed notation for C_{BYP} to C_{FF} 9
- Changed Figure 32; changed C_{BYP} to C_{FF} 20

Changes from Revision A (March 2011) to Revision B **Page**

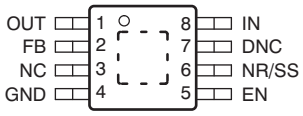
- Changed V_{REF} parameter typical specification in Electrical Characteristics table 7

Changes from Original (August 2010) to Revision A **Page**

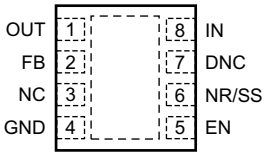
- Switched colors for 10mA and 200mA curves in Figure 10 8

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP PowerPAD
Top View



DRB Package
VSON-8
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DNC	7	—	Do not connect. Do not route this pin to any electrical net, not even GND or IN.
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN(+HI,\ min)}$ or $V_{EN} \leq V_{EN(-HI,\ max)}$, the regulator is enabled. If $V_{EN(+LO,\ max)} \geq V_{EN} \geq V_{EN(-LO,\ min)}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $\lvert V_{EN} \rvert \leq \lvert V_{IN} \rvert$.
FB	2	I	This pin is the feedback pin that sets the output voltage of the device.
GND	4	—	Ground
IN	8	I	Input supply
NC	3	—	Not internally connected. This pin must either be left open or tied to GND.
NR/SS	6	—	Noise reduction pin. Connecting an external capacitor to this pin filters the noise generated by the internal band gap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.
OUT	1	O	Regulator output. A capacitor ≥ 2.2 µF must be tied from this pin to ground to ensure stability.
PowerPAD	—	—	Must either be left open or tied to GND. Solder to printed-circuit-board (PCB) plane to enhance thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–36	0.3	V
	OUT pin to GND pin	–33	0.3	V
	OUT pin to IN pin	–0.3	36	V
	FB pin to GND pin	–2	0.3	V
	FB pin to IN pin	–0.3	36	V
	EN pin to IN pin	–0.3	36	V
	EN pin to GND pin	–36	36	V
	NR/SS pin to IN pin	–0.3	36	V
	NR/SS pin to GND pin	–2	0.3	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	–35		–3	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Output voltage	V_{REF}		33	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	2.2	10		µF
C_{OUT}	Output capacitor	2.2	10		µF
C_{NR}	Noise reduction capacitor	0	10		nF
C_{FF}	Feed-forward capacitor	0	10		nF
R_2	Lower feedback resistor			237	kΩ

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A30		UNIT
		DGN (HVSSOP PowerPAD)	DRB (VSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	47.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53	55.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	13.5	7.0	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics(1)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		–35		–3	V
V_{REF}	Internal reference(2)	T_J = 25°C, $V_{NR/SS} = V_{REF}$	–1.202	–1.179	–1.166	V
V_{FB}	Feedback voltage			–1.176		V
V_{OUT}	Output voltage range(3)	$\|V_{IN}\| \geq \|V_{OUT(nom)}\| + 1$ V	–33		V_{REF}	V
	Nominal accuracy	T_J = 25°C, $\|V_{IN}\| = \|V_{OUT(nom)}\| + 0.5$ V	–1.5		1.5	$\%V_{OUT}$
	Overall accuracy	$\|V_{OUT(nom)}\| + 1$ V ≤ $\|V_{IN}\|$ ≤ 35 V 1 mA ≤ I_{OUT} ≤ 200 mA	–2.5		2.5	$\%V_{OUT}$
$\left\|\frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}}\right\|$	Line regulation	T_J = 25°C, $\|V_{OUT(nom)}\| + 1$ V ≤ $\|V_{IN}\|$ ≤ 35 V		0.14		$\%V_{OUT}$
$\left\|\frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}}\right\|$	Load regulation	T_J = 25°C, 1 mA ≤ I_{OUT} ≤ 200 mA		0.04		$\%V_{OUT}$
$\|V_{DO}\|$	Dropout voltage	V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 100 mA		216		mV
		V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 200 mA		325	600	mV
I_{CL}	Current limit	V_{OUT} = 90% $V_{OUT(nom)}$	220	330	500	mA
I_{GND}	Ground current	I_{OUT} = 0 mA		55	100	µA
		I_{OUT} = 100 mA		950		µA
$\|I_{SHDN}\|$	Shutdown supply current	V_{EN} = 0.4 V		1	3	µA
		V_{EN} = –0.4 V		1	3	µA
I_{FB}	Feedback current(4)			14	100	nA
$\|I_{EN}\|$	Enable current	$V_{EN} = \|V_{IN}\| = \|V_{OUT(nom)}\| + 1$ V		0.48	1	µA
		$V_{IN} = V_{EN}$ = –35 V		0.51	1	µA
		V_{IN} = –21 V, V_{EN} = 15 V		0.5	1	µA
$V_{EN(+HI)}$	Positive enable high-level voltage	T_J = –40°C to 125°C	2		15	V
		T_J = –40°C to 85°C	1.8		15	V
$V_{EN(+LO)}$	Positive enable low-level voltage		0		0.4	V
$V_{EN(–HI)}$	Negative enable high-level voltage		V_{IN}		–2	V
$V_{EN(–LO)}$	Negative enable low-level voltage		–0.4		0	V
V_n	Output noise voltage	V_{IN} = –3 V, $V_{OUT(nom)} = V_{REF}$, C_{OUT} = 10 µF, $C_{NR/SS}$ = 10 nF, BW = 10 Hz to 100 kHz		15.1		μV_{RMS}
		V_{IN} = –6.2 V, $V_{OUT(nom)}$ = –5 V, C_{OUT} = 10 µF, $C_{NR/SS} = C_{FF}$(5) = 10 nF, BW = 10 Hz to 100 kHz		17.5		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = –6.2 V, $V_{OUT(nom)}$ = –5 V, C_{OUT} = 10 µF, $C_{NR/SS} = C_{FF}$(5) = 10 nF, f = 120 Hz		72		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_J	Operating junction temperature range		–40		125	°C

(1) At operating conditions, $V_{IN} \leq 0$ V, $V_{OUT(nom)} \leq V_{REF} \leq 0$ V. At regulation, $V_{IN} \leq V_{OUT(nom)} - |V_{DO}|$. $I_{OUT} > 0$ V flows from OUT to IN.
(2) V_{REF} is measured at the NR/SS pin.
(3) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 µA is required.
(4) $I_{FB} > 0$ V flows into the device.
(5) C_{FF} refers to a feed-forward capacitor connected to the FB and OUT pins.

6.6 Typical Characteristics

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at T_A = 25°C.

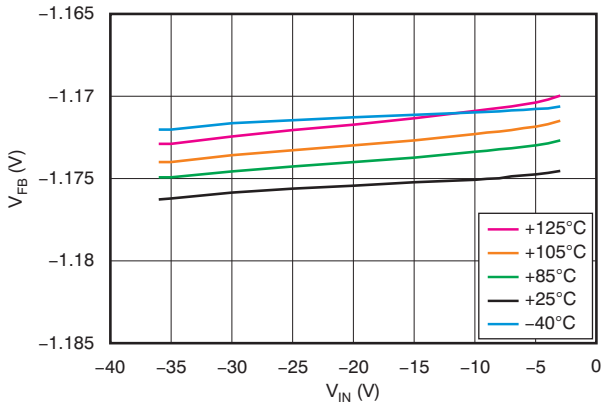


Figure 1. Feedback Voltage vs Input Voltage

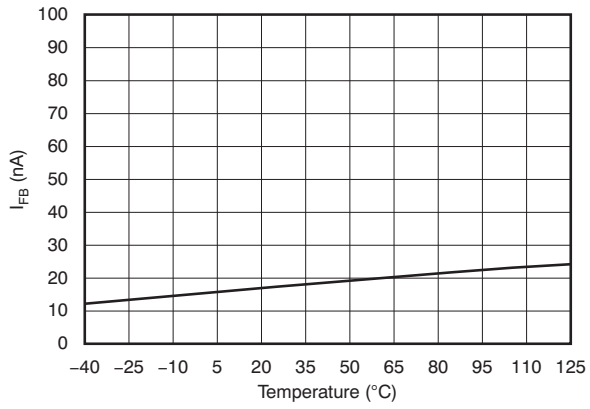


Figure 2. Feedback Current vs Temperature

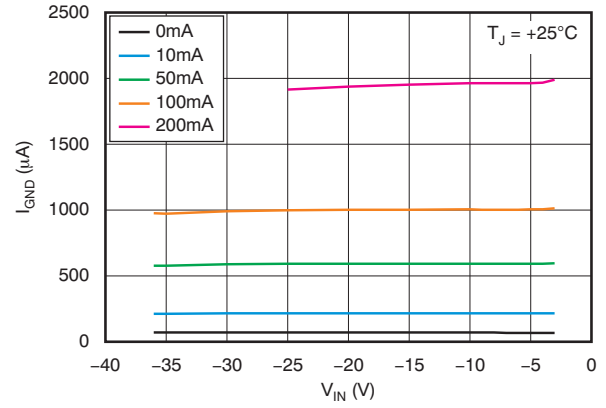


Figure 3. Ground Current vs Input Voltage

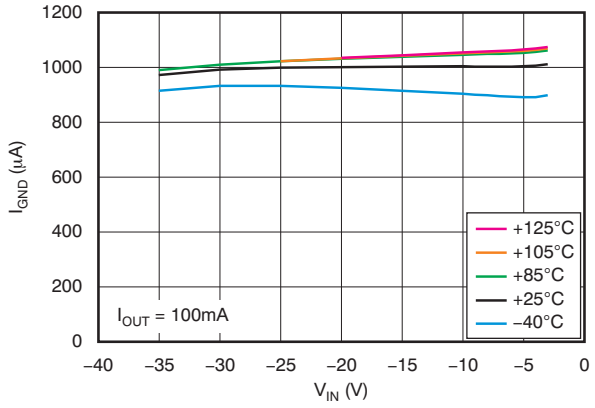


Figure 4. Ground Current vs Input Voltage

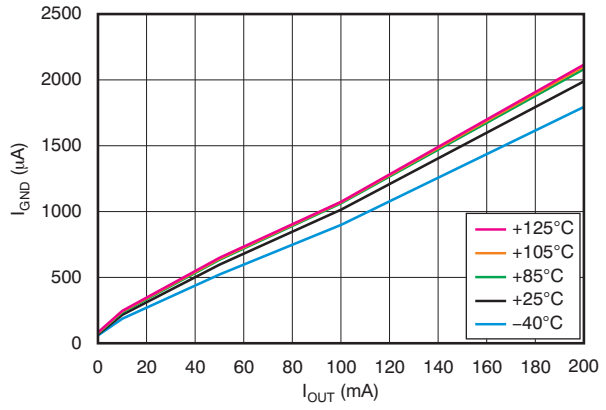


Figure 5. Ground Current vs Output Current

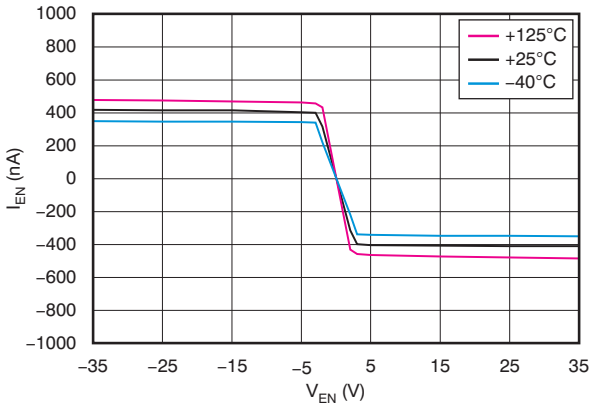


Figure 6. Enable Current vs Enable Voltage

Typical Characteristics (continued)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at T_A = 25°C.

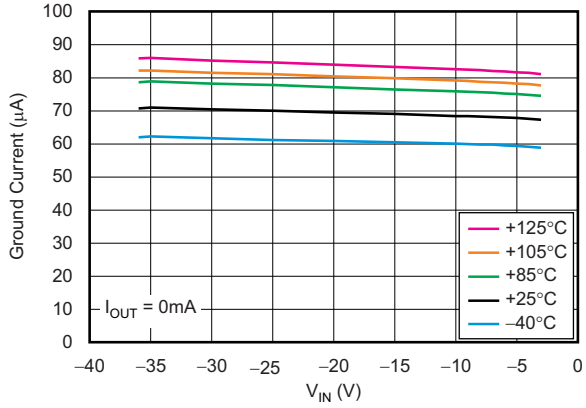


Figure 7. Ground Current vs Input Voltage

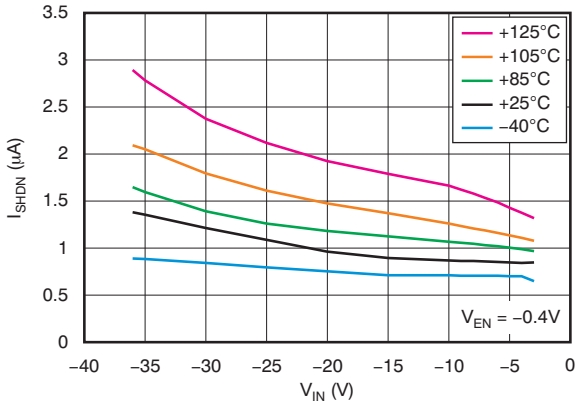


Figure 8. Shutdown Current vs Input Voltage

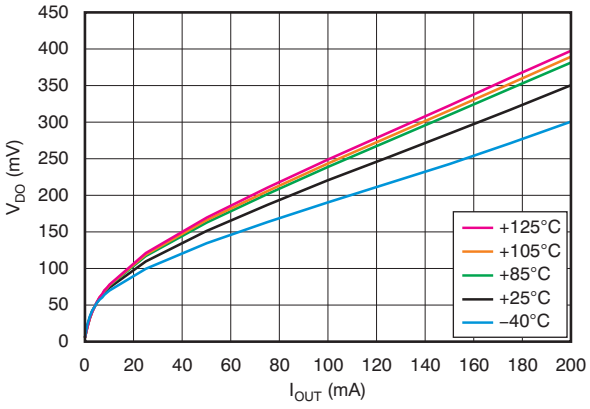


Figure 9. Dropout Voltage vs Output Current

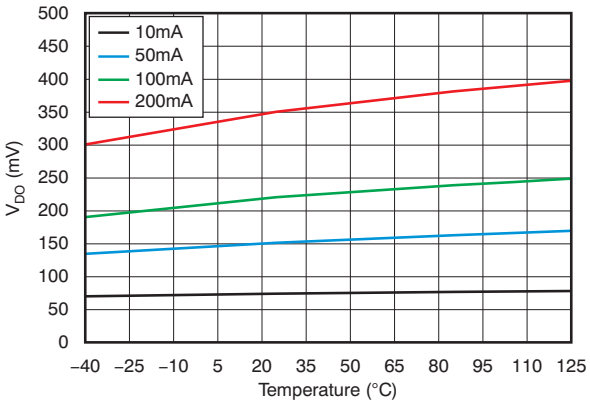


Figure 10. Dropout Voltage vs Temperature

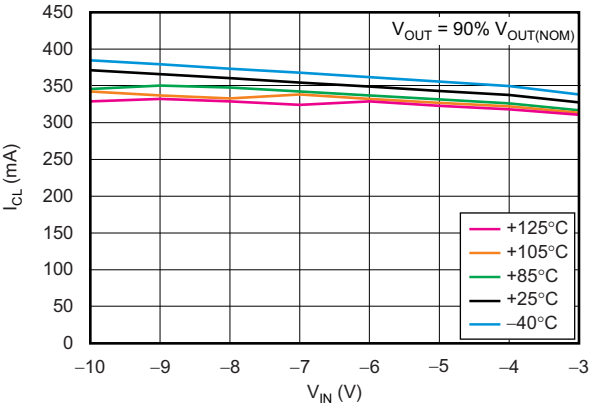


Figure 11. Current Limit vs Input Voltage

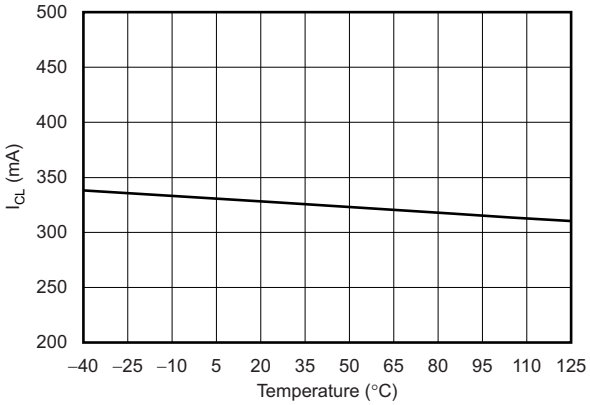


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at T_A = 25°C.

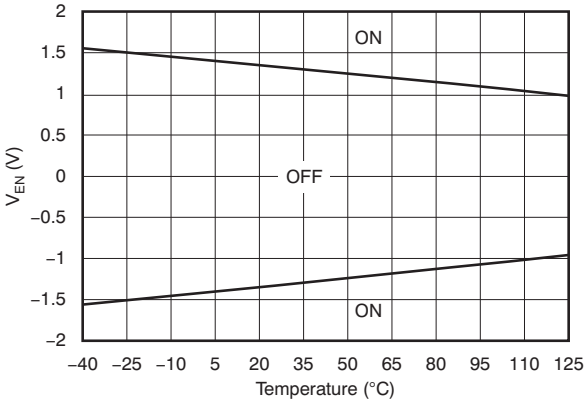


Figure 13. Enable Threshold Voltage vs Temperature

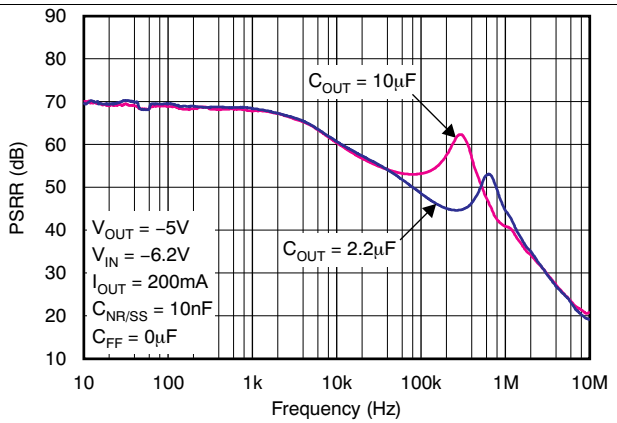


Figure 14. Power-Supply Rejection Ratio vs C_{OUT}

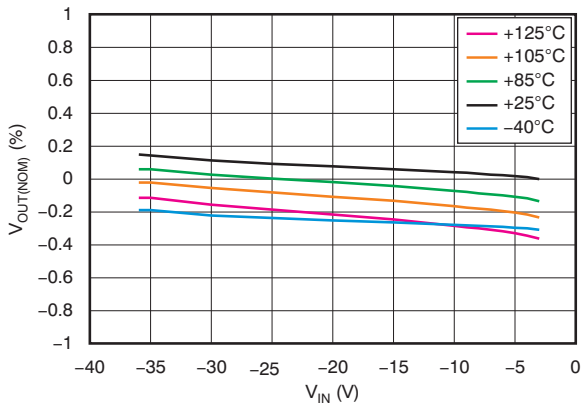


Figure 15. Line Regulation

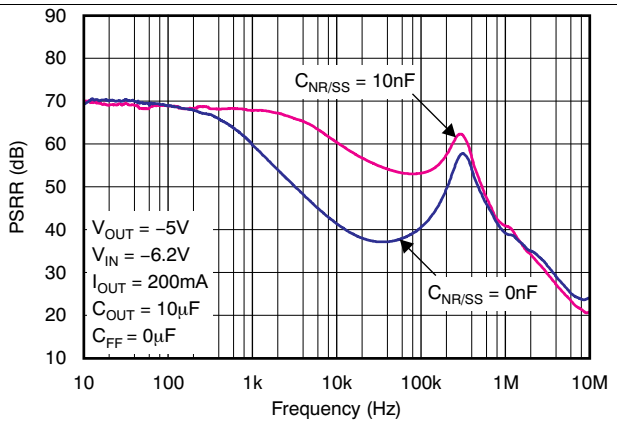


Figure 16. Power-Supply Rejection Ratio vs $C_{NR/SS}$

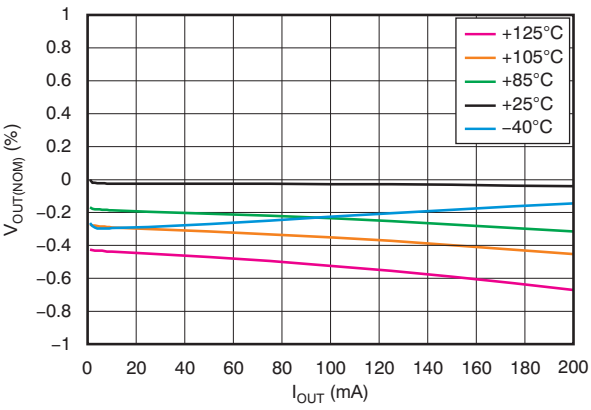


Figure 17. Load Regulation

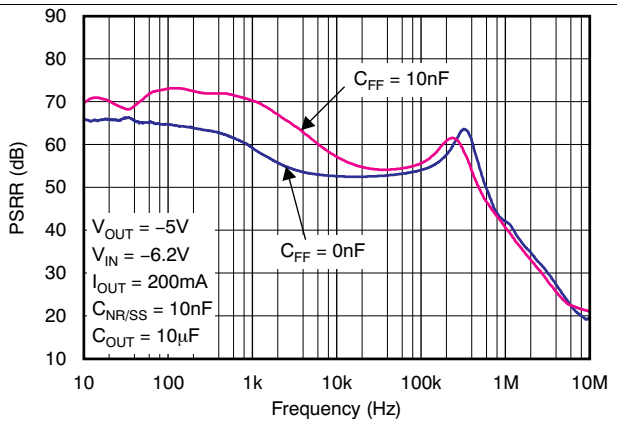


Figure 18. Power-Supply Rejection Ratio vs C_{FF}

Typical Characteristics (continued)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at T_A = 25°C.

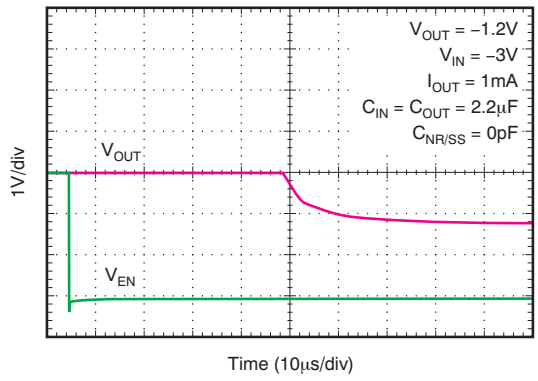


Figure 19. Capacitor-Programmable Soft-Start

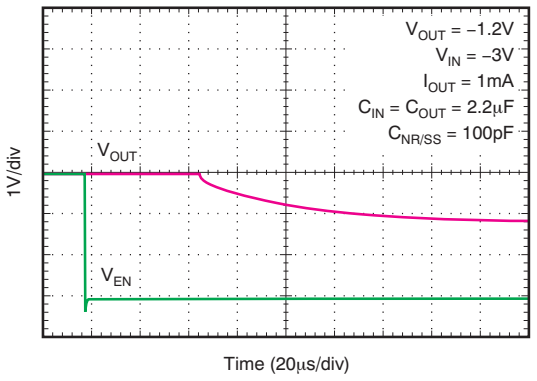


Figure 20. Capacitor-Programmable Soft-Start

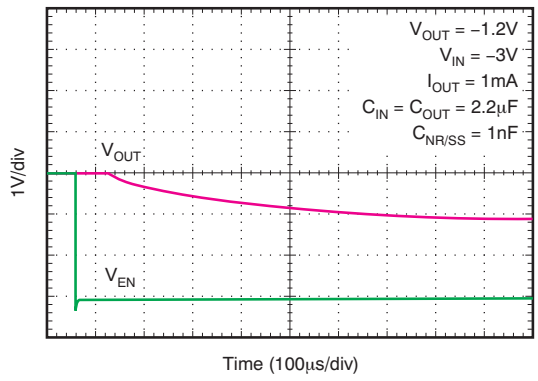


Figure 21. Capacitor-Programmable Soft-Start

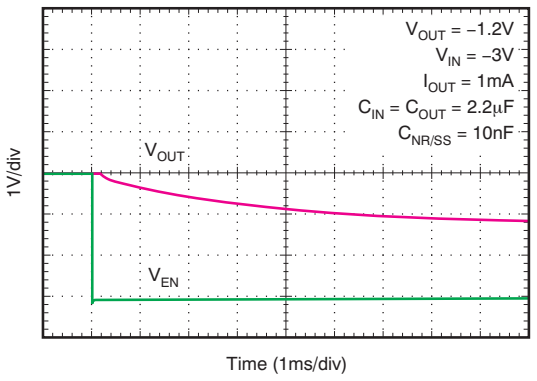


Figure 22. Capacitor-Programmable Soft-Start

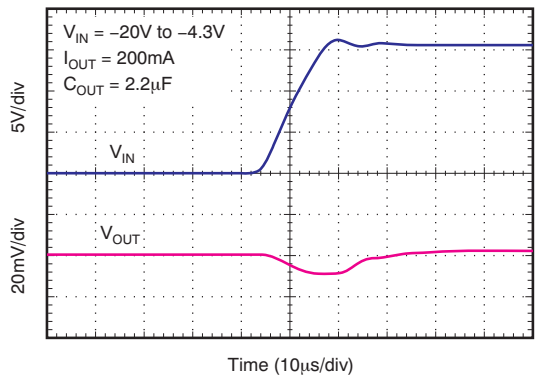


Figure 23. Line Transient Response

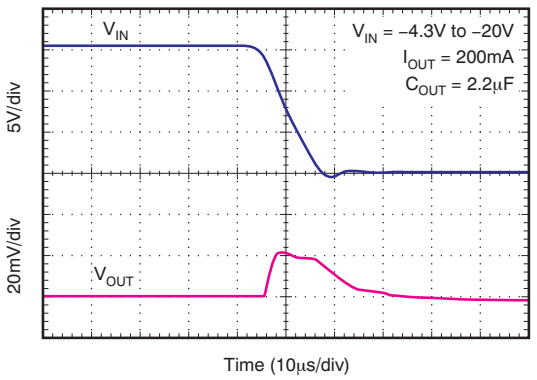


Figure 24. Line Transient Response

Typical Characteristics (continued)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at T_A = 25°C.

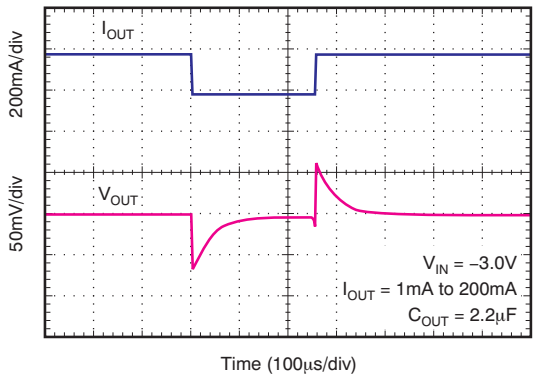
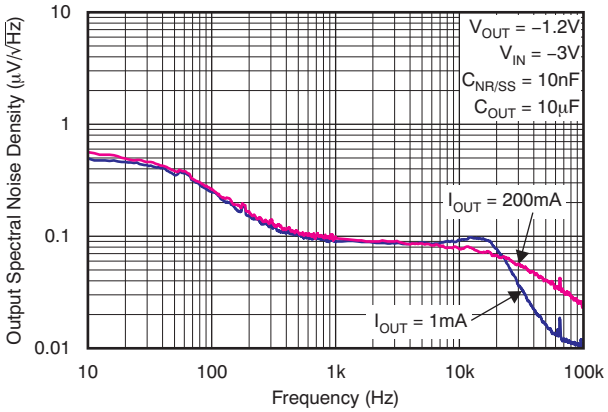


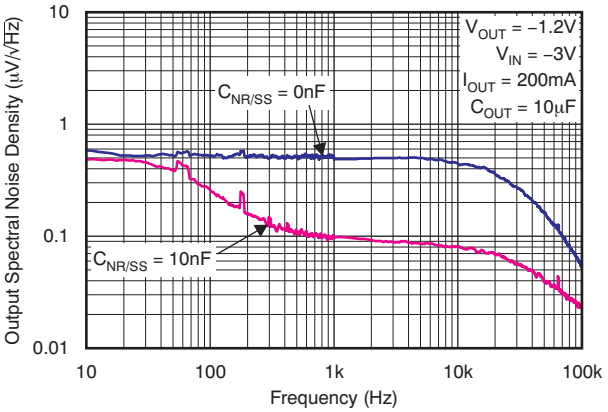
Figure 25. Load Transient Response

7 Parameter Measurement Information



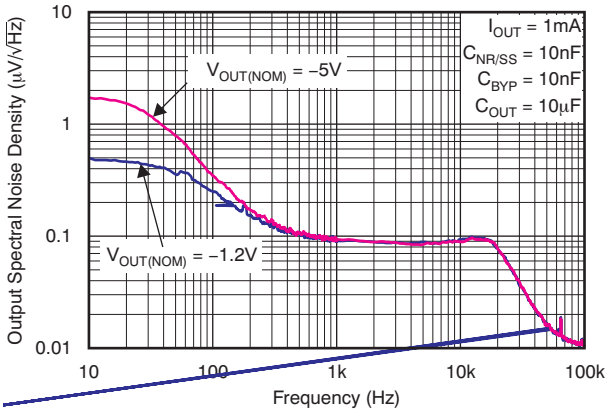
I_{OUT}	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
1mA	15.13	14.73
200mA	17.13	16.71

Figure 26. Output Spectral Noise Density vs Output Current



$C_{NR/SS}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
0nF	80.00	79.83
10nF	17.29	16.81

Figure 27. Output Spectral Noise Density vs $C_{NR/SS}$



$V_{OUT(NOM)}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
–5V	17.50	15.04
–1.2V	15.13	14.73

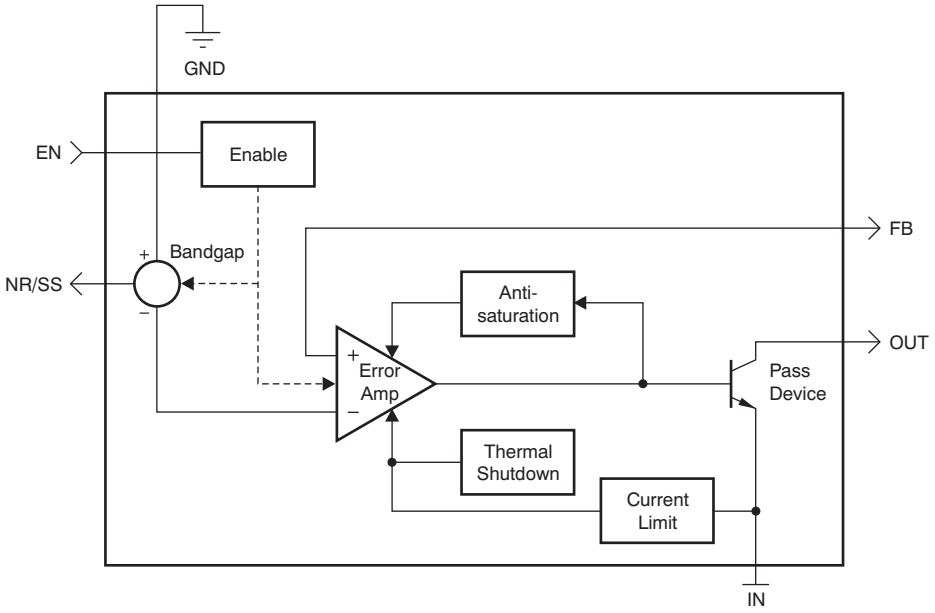
Figure 28. Output Spectral Noise Density vs $V_{OUT(nom)}$

8 Detailed Description

8.1 Overview

The TPS7A30 family of devices are wide V_{IN}, low-noise, 150-mA linear regulators (LDOs). These devices feature an enable pin, programmable soft-start, current limiting, and thermal protection circuitry that allow the device to be used in a wide variety of applications. As bipolar-based devices, the TPS7A30 devices are ideal for high-accuracy, high-precision applications at higher voltages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A30 family helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (330 mA, typical), and is largely independent of the output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

8.3.2 Programmable Soft-Start

The NR/SS capacitor also functions as a soft-start capacitor to slow down the rise time of the output. The rise time of the output when using an NR/SS capacitor is governed by Equation 1. In Equation 1, t_{SS} is the soft-start time in milliseconds and $C_{NR/SS}$ is the capacitance at the NR pin in nanofarads. Figure 29 shows the relationship between the $C_{NR/SS}$ size and the start-up time without a C_{FF}.

$$t_{SS}\ (ms) = 0.9 \times C_{NR/SS}\ (nF) \quad (1)$$

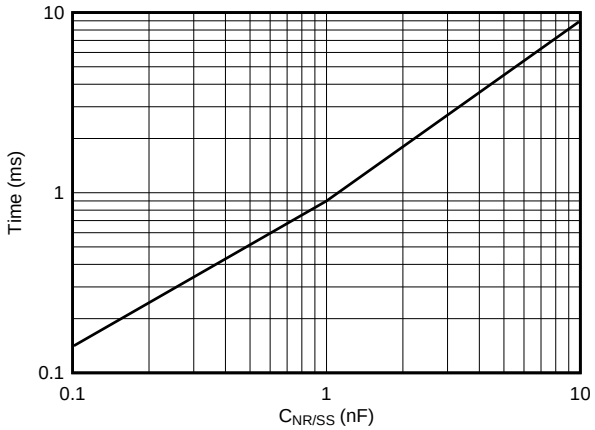


Figure 29. Soft-Start Time vs $C_{NR/SS}$

8.3.3 Enable Pin Operation

The TPS7A30 provides a dual-polarity enable pin (EN) that turns on the regulator when $|V_{EN}| > 2$ V, whether the voltage is positive or negative, as shown in Figure 30.

This functionality allows for different system power management topologies:

- Connecting the EN pin directly to a negative voltage (such as V_{IN}).
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

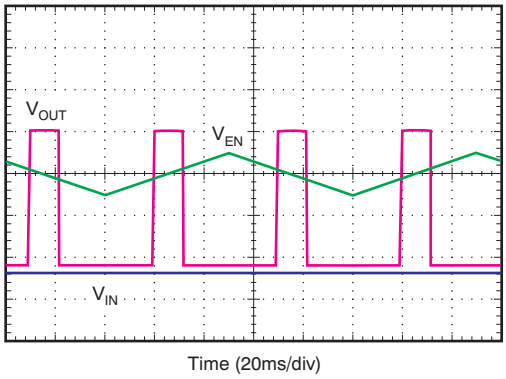


Figure 30. Enable Pin Positive and Negative Threshold

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as the $|V_{IN(min)}|$.
- The input voltage magnitude is greater than the nominal output voltage magnitude added to the dropout voltage.
- $|V_{EN}| > |V_{(HI)}|$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

8.4.2 Dropout Operation

If the input voltage magnitude is lower than the nominal output voltage magnitude plus the specified dropout voltage magnitude, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage magnitude is the same as the input voltage magnitude minus the dropout voltage magnitude. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- $|V_{EN}| < |V_{(HI)}|$.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$\|V_{IN}\| > \{ \|V_{OUT(nom)}\| + \|V_{DO}\|, \|V_{IN(min)}\| \}$	$\|V_{EN}\| > \|V_{(HI)}\|$	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$\|V_{IN(min)}\| < \|V_{IN}\| < \|V_{OUT(nom)}\| + \|V_{DO}\|$	$\|V_{EN}\| > \|V_{(HI)}\|$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$\|V_{EN}\| < \|V_{(LO)}\|$	—	$T_J > 170°C$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7A30 belongs to a family of linear regulators that use an innovative bipolar process to achieve ultralow-noise. The TPS7A30 are bipolar-based devices and are therefore ideal for high-accuracy, high-performance analog applications at higher voltages.

9.1.1 Adjustable Operation

The TPS7A3001 has an output voltage range of –1.174 V to –33 V. The nominal output voltage of the device is set by two external resistors; see Figure 32.

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 2. To ensure stability under no load conditions, this resistive network must provide a current equal to or greater than 5 µA.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB(nom)}} - 1\right), \text{ where } \frac{|V_{FB(nom)}|}{R_2} > 5\mu A \quad (2)$$

If greater voltage accuracy is required, take into account the output voltage offset contributions resulting from the feedback pin current and use 0.1% tolerance resistors. Table 2 shows the 1% resistor values for several different standard output voltages.

Table 2. Standard 1% Resistor Values for Various Output Voltages

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)
–2.5	11.3	10
–5	32.4	10
–12	93.1	10
–15	118	10
–18	143	10

9.1.2 Capacitor Recommendations

Use low-equivalent series resistance (ESR) capacitors for the input, output, noise reduction, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. Ceramic X7R capacitors offer improved overtemperature performance, whereas ceramic X5R capacitors are the most cost-effective and are available in higher values.

NOTE

High-ESR capacitors can degrade PSRR.

9.1.2.1 Input and Output Capacitor Requirements

The TPS7A30 family of negative, high-voltage linear regulators achieve stability with a minimum input and output capacitance of 2.2 µF; however, TI highly recommends using a 10-µF capacitor to maximize ac performance.

9.1.2.2 Noise-Reduction and Feed-Forward Capacitor Requirements

Although noise-reduction and feed-forward capacitors ($C_{NR/SS}$ and C_{FF}, respectively) are not needed to achieve stability, TI highly recommends using 10-nF capacitors to minimize noise and maximize ac performance.

For more information on C_{FF}, refer to application report, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* (SBVA042). This application report explains the advantages of using C_{FF} (also known as C_{BYP}), and the problems that can occur when using this capacitor.

9.1.3 Maximum AC Performance

To maximize noise and PSRR performance, TI recommends including a 10-µF or higher input and output capacitors, and 10-nF noise-reduction and bypass capacitors; see Figure 32. The solution illustrated in Figure 32 delivers minimum noise levels of 15.1 μV_{RMS} and power-supply rejection levels above 55 dB from 10 Hz to 700 kHz; see Figure 18 and Figure 26.

9.1.4 Output Noise

The TPS7A30 provides low output noise when a noise-reduction capacitor ($C_{NR/SS}$) is used.

The noise-reduction capacitor serves as a filter for the internal reference. By using a 10-nF noise reduction capacitor, the output noise is reduced by approximately 80% (from 80 μV_{RMS} to 17 μV_{RMS}); see Figure 27.

The TPS7A30 low output voltage noise makes the device an ideal solution for powering noise-sensitive circuitry.

9.1.5 Power-Supply Rejection

The 10-nF noise-reduction capacitor greatly improves TPS7A30 power-supply rejection, achieving up to 20 dB of additional power-supply rejection for frequencies between 110 Hz and 400 kHz.

Additionally, ac performance can be maximized by adding a 10-nF bypass capacitor (C_{FF}) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies, for the band from 10 Hz to 200 kHz; see Figure 18.

The very high power-supply rejection of the TPS7A30 makes the device a good choice for powering high-performance analog circuitry (such as operational amplifiers, ADCs, DACS, and audio amplifiers).

9.1.6 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response.

9.1.7 Post DC-DC Converter Filtering

Most of the time, the voltage rails available in a system do not match the voltage requirements for the system. These rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. These converters offer high efficiency with minimum heat generation, but have one primary disadvantage: these converters introduce a high-frequency component (and the associated harmonics) in addition to the dc output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A30 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes the device ideal for post dc-dc converter filtering; see Figure 31. TI highly recommends using the maximum performance schematic illustrated in Figure 32. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR; see Figure 18.

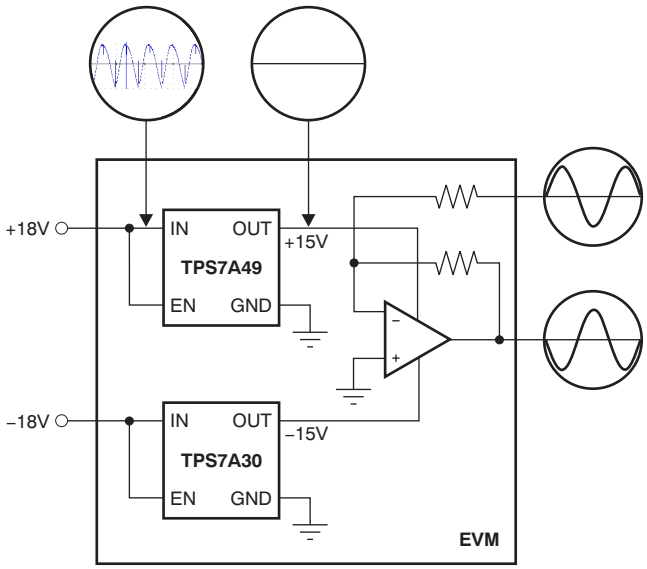


Figure 31. Post DC-DC Converter Regulation to High-Performance Analog Circuitry

9.1.8 Audio Applications

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20 Hz to 20 kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very-high power-supply rejection ratio (> 55 dB) and low noise at the audio band of the TPS7A30 maximize performance for audio applications; see Figure 18.

9.1.9 Power for Precision Analog

One of the primary TPS7A30 applications is to provide ultralow noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

In conjunction with its positive counterpart, the TPS7A49xx family of positive high-voltage linear regulators, the TPS7A30 family of negative high voltage linear regulators provides ultralow noise positive and negative voltage rails to high-performance analog circuitry (such as operational amplifiers, ADCs, DACs, and audio amplifiers).

The low noise levels at high voltages, such as ±15 V, enables clean power rails for precision analog circuitry. This characteristic allows for high-performance analog solutions to optimize the voltage range, thus maximizing system accuracy.

9.2 Typical Application

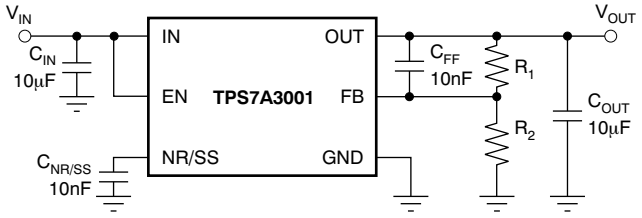


Figure 32. Adjustable Operation for Maximum AC Performance

9.2.1 Design Requirements

The design goals are V_{IN} = –3 V, V_{OUT} = –1.2 V, and I_{OUT} = 150 mA, maximum. The design must optimize transient response and meet a start-up time of 14 ms. The input supply comes from a supply on the same printed circuit board (PCB). The design circuit is shown in Figure 32.

The design space consists of C_{IN}, C_{OUT}, $C_{NR/SS}$, R_1, and R_2, at $T_{A(max)}$ = 75°C.

9.2.2 Detailed Design Procedure

The first step when designing with a linear regulator is to examine the maximum load current, along with the input and output voltage requirements, to determine if the device thermal and dropout voltage requirements can be met. At 150 mA, the input dropout voltage of the TPS7A30 family is a maximum of 600 mV overtemperature; therefore, the dropout headroom of 1.8 V is sufficient for operation over both input and output voltage accuracy. Dropout headroom is calculated as $V_{IN} – V_{OUT} – V_{DO(max)}$, and must be greater than 0 V for reliable operation. $V_{DO(max)}$ is the maximum dropout allowed, given worst-case load conditions.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output, multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is |3 V – 1.2 V|, resulting in $V_{IN} – V_{OUT}$ = 1.8 V. The power dissipated in the pass element is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 0.273 W, and is calculated as Equation 3:

$$P_D = (V_{IN} – V_{OUT}) (I_{MAX}) + (V_{IN}) (I_Q) \quad (3)$$

When the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. This calculation gives the worst-case junction temperature; good thermal design can significantly reduce this number. For thermal resistance information, refer to the *Thermal Information* table. For this example, using the DGN package, the maximum junction temperature rise is calculated to be 17.3°C. The maximum junction temperature rise is calculated by adding the junction temperature rise to the maximum ambient temperature, which is 75°C for this example. For this example, calculate the maximum junction temperature as 92.3°C. Keep in mind that the maximum junction temperate must be below 125°C for reliable device operation. Additional ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature.

Use the following equations to select the rest of the components:

To ensure stability under no-load conditions, the current through the resistor network must be greater than 5 µA, as shown in Equation 4.

$$\frac{V_{FB}}{R_2} > 5\mu A \rightarrow R_2 < 242.4\ k\Omega \quad (4)$$

To set R_2 = 100 kΩ for a standard 1% value resistor, calculate R_1 as shown in Equation 5.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF(nom)}} - 1 \right) = 100\ k\Omega \left(\frac{1.2\ V}{1.176\ V} - 1 \right) = 2.04\ k\Omega \quad (5)$$

Use a standard, 1%, 2.05-kΩ resistor for R_1.

Typical Application (continued)

Equation 6 calculates the start-up time, t_{SS}.

$$t_{SS}\ (ms) = 0.9 \times C_{NR/SS} = 14\ ms$$

$$C_{SS} = 15\ nF \tag{6}$$

For the soft-start to dominate the start-up conditions, ideally place the start-up time as a result of the current limit at two decades below the soft-start time (at 140 µs). C_{OUT} must be at least 2.2 µF for stability, as shown in Equation 7 and Equation 8.

$$t_{SS(CL)} = V_{OUT}\left(\frac{C_{OUT}}{I_{CL(max)}}\right) \tag{7}$$

$$C_{OUT(max)} = t_{SS(CL)}\left(\frac{I_{CL(min)}}{V_{OUT}}\right) = 140\ \mu s \times \frac{220\ mA}{2\ V} = 15.4\ \mu F \tag{8}$$

For C_{IN}, assume that the –3-V supply has some inductance and is placed several inches away from the PCB. For this case, select a 2.2-µF ceramic input capacitor to ensure that the input impedance is negligible to the LDO control loop and to keep the physical size and cost of the capacitor low; this component is a common-value capacitor.

For better PSRR for this design, use a 10-µF input and output capacitor. To reduce the peaks from transients but slow down the recovery time, increase the output capacitor size or add additional output capacitors.

Typical Application (continued)

9.2.3 Application Curves

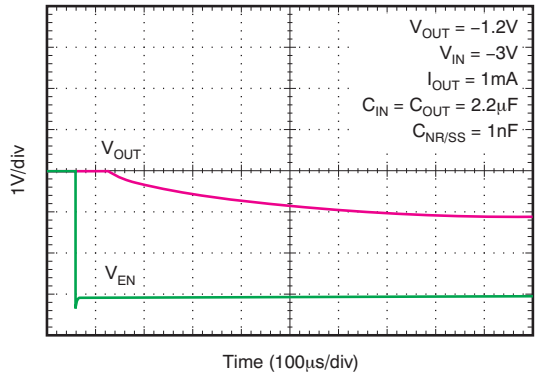


Figure 33. Capacitor-Programmable Soft-Start

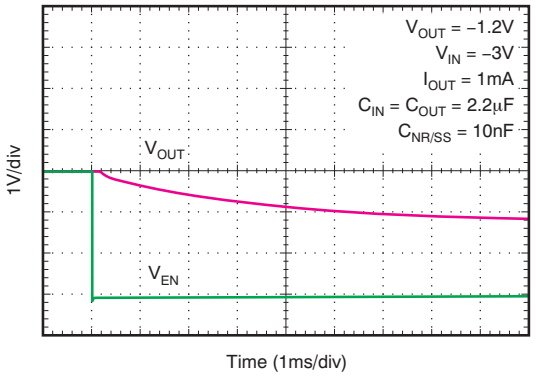


Figure 34. Capacitor-Programmable Soft-Start

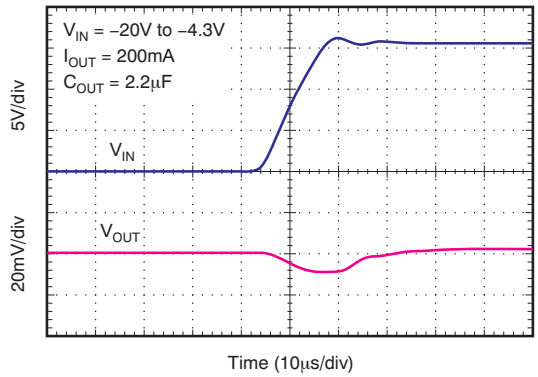


Figure 35. Line Transient Response

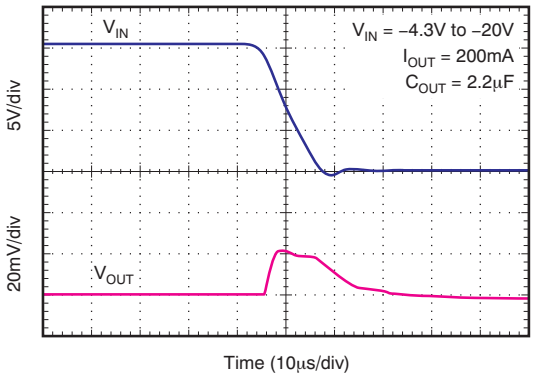


Figure 36. Line Transient Response

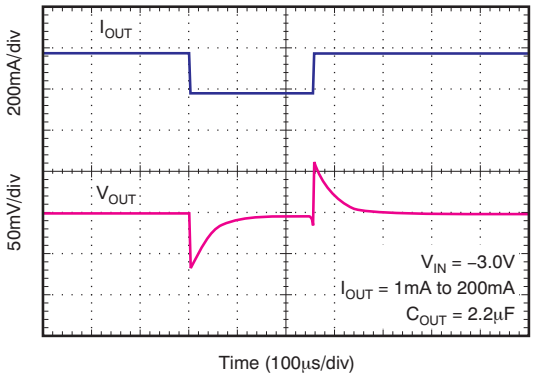


Figure 37. Load Transient Response

9.3 Do's and Don’ts

Place at least one low-ESR, 2.2-µF capacitor as close as possible to both the IN and OUT pins of the regulator to the GND pin.

Provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the enable (EN) pin.

Do not resistively or inductively load the NR/SS pin.

10 Power Supply Recommendations

The input supply for the LDO must be within the recommended operating conditions (that is, between –3 V and –35 V). The input voltage must provide adequate headroom in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

The input and output supplies must also be bypassed with at least a 2.2-µF capacitor located near the input and output pins. There must be no other components located between these capacitors and the pins.

11 Layout

11.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin must be tied directly to the PowerPAD under the device. The PowerPAD must be connected to any internal PCB ground planes using multiple vias directly under the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, and C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can negatively affect system performance, and can even cause instability.

11.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane star-connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

11.2 Layout Examples

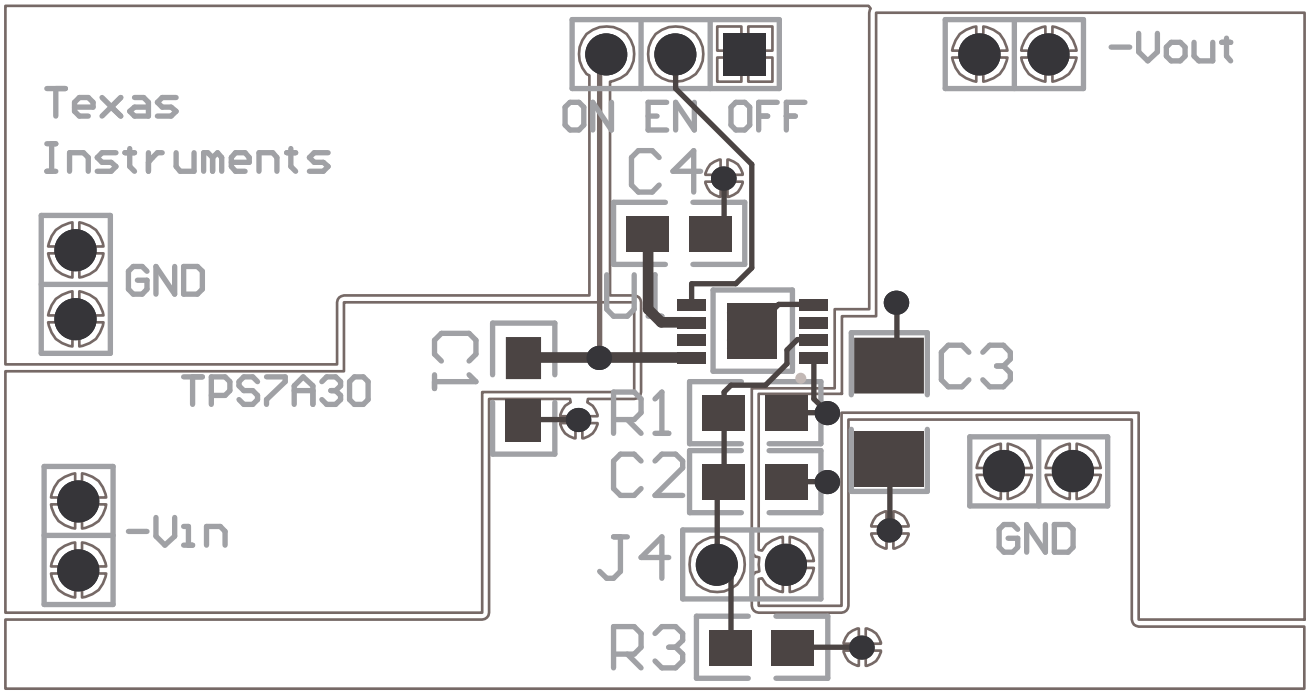


Figure 38. PCB Layout Example

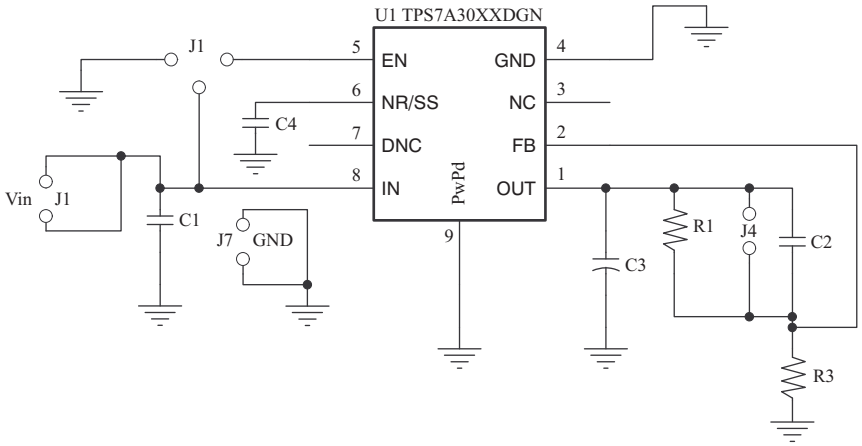
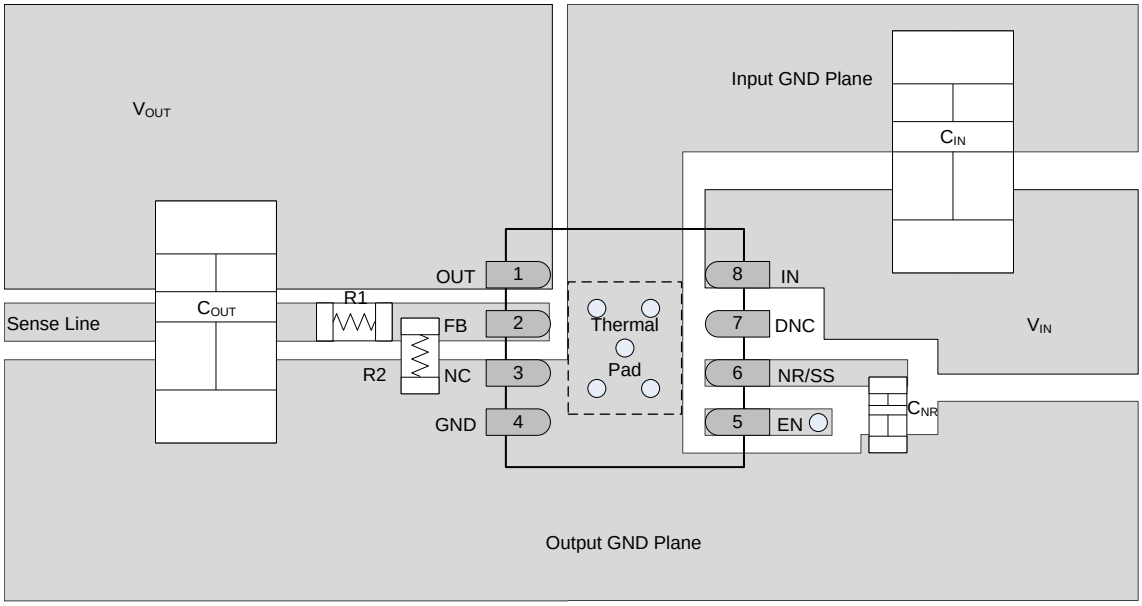


Figure 39. PCB Layout Example Schematic



NOTE: C_{IN} and C_{OUT} are size 1206 capacitors, and C_{NR}, R1, and R2 are size 0402.

Figure 40. PCB Layout Example

11.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 45°C above the maximum expected ambient condition of any particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A30 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS7A30 into thermal shutdown degrades device reliability.

11.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data or JEDEC low- and high-K boards are provided in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element, as shown in Equation 9.

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \tag{9}$$

Power Dissipation (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, as discussed in the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 10.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D \tag{10}$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{10}$$

where

- P_D is the power dissipation given by Equation 9,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A30. The TPS7A30-49EVM-567 evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A30 is available through the product folders under the *Tools & Software* tab.

12.1.2 Device Nomenclature

Table 3. Ordering Information(1)

PRODUCT	V_{OUT}
TPS7A30**xx** ***yyy*** **z**	**XX** is nominal output voltage (01 = Adjustable).(2) **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) For fixed –1.2-V operation, tie FB to OUT.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042.
- *Using New Thermal Metrics*, SBVA025
- *TPS7A30-49EVM-567 Evaluation Module User's Guide*, SLVU405

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3001DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSZQ	Samples
TPS7A3001DGNT	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSZQ	Samples
TPS7A3001DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSZQ	Samples
TPS7A3001DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSZQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

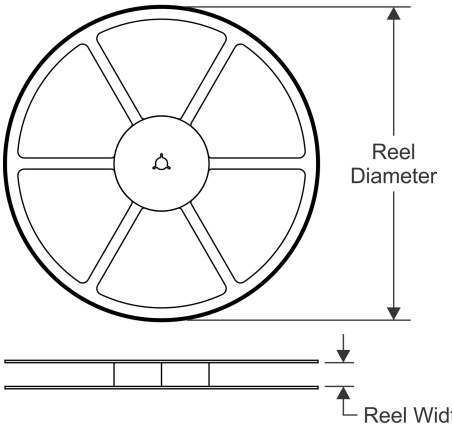
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

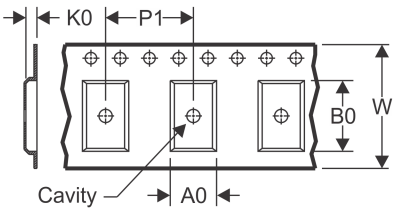
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

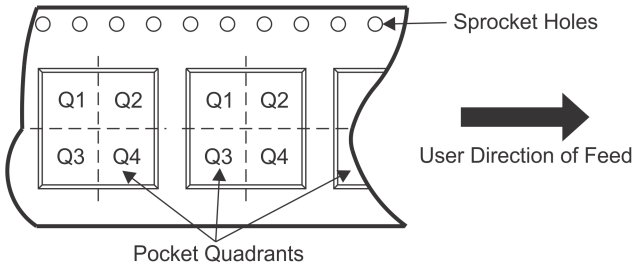


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

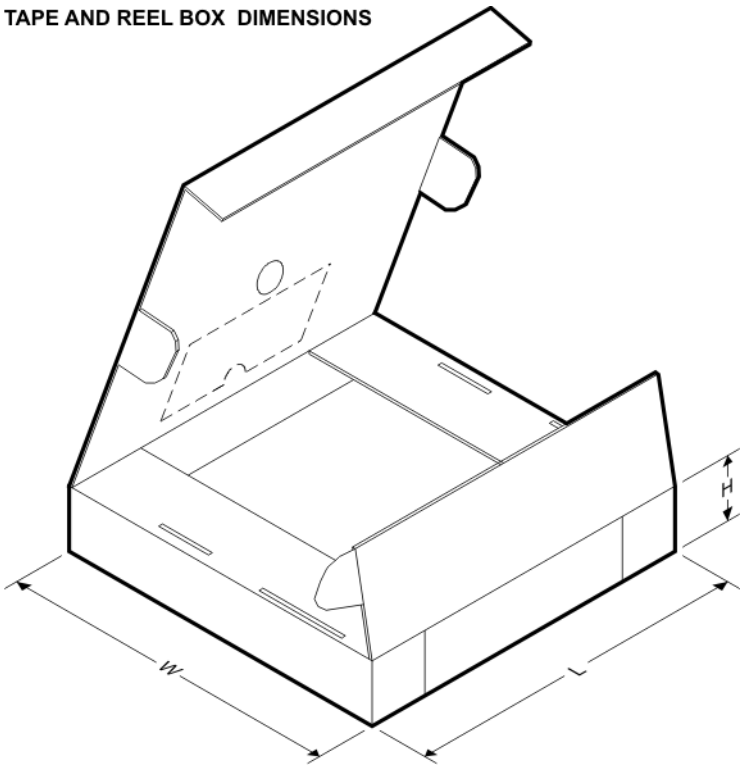
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3001DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A3001DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A3001DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A3001DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3001DGNR	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0
TPS7A3001DGNT	MSOP-PowerPAD	DGN	8	250	210.0	185.0	35.0
TPS7A3001DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS7A3001DRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

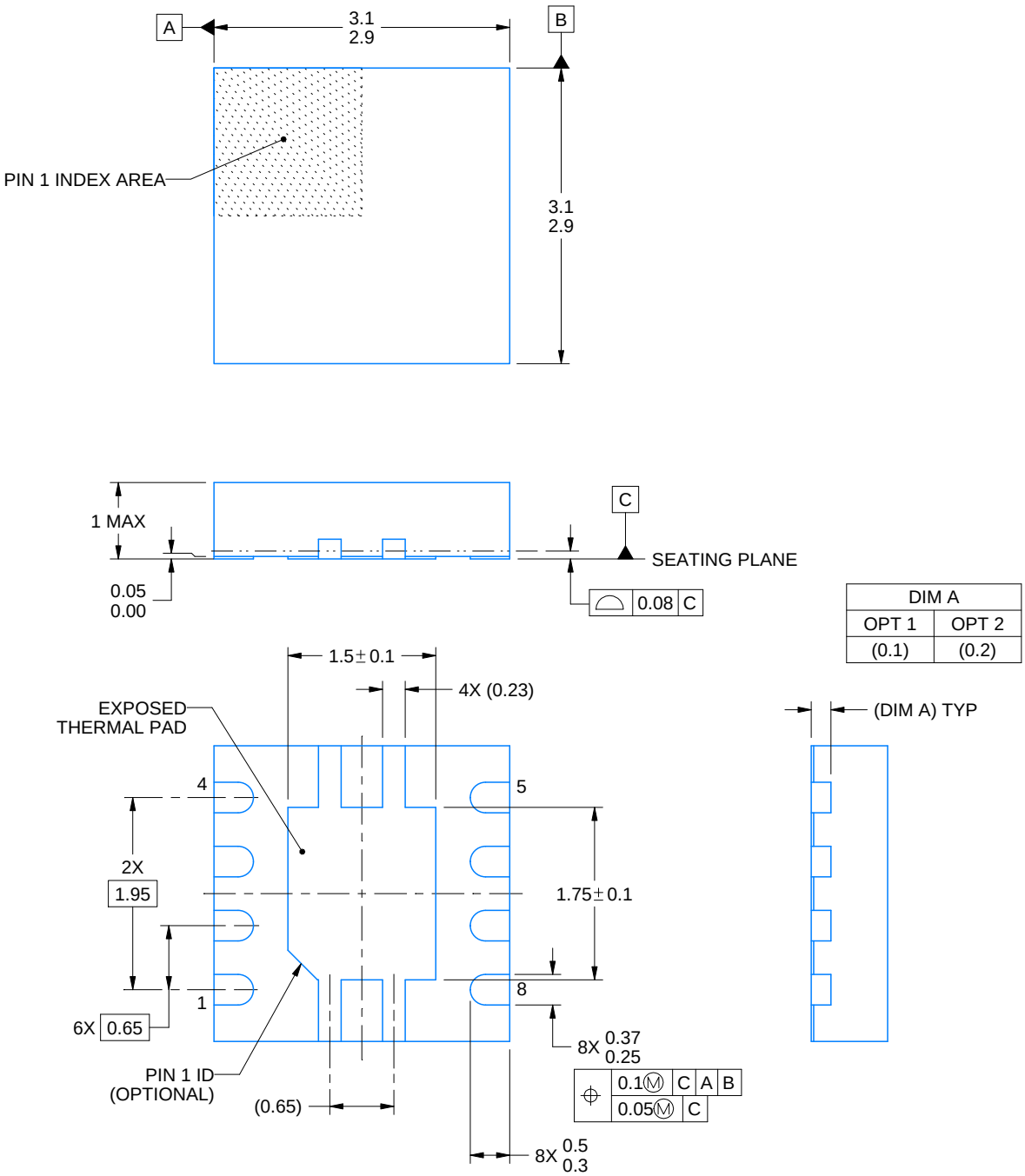
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

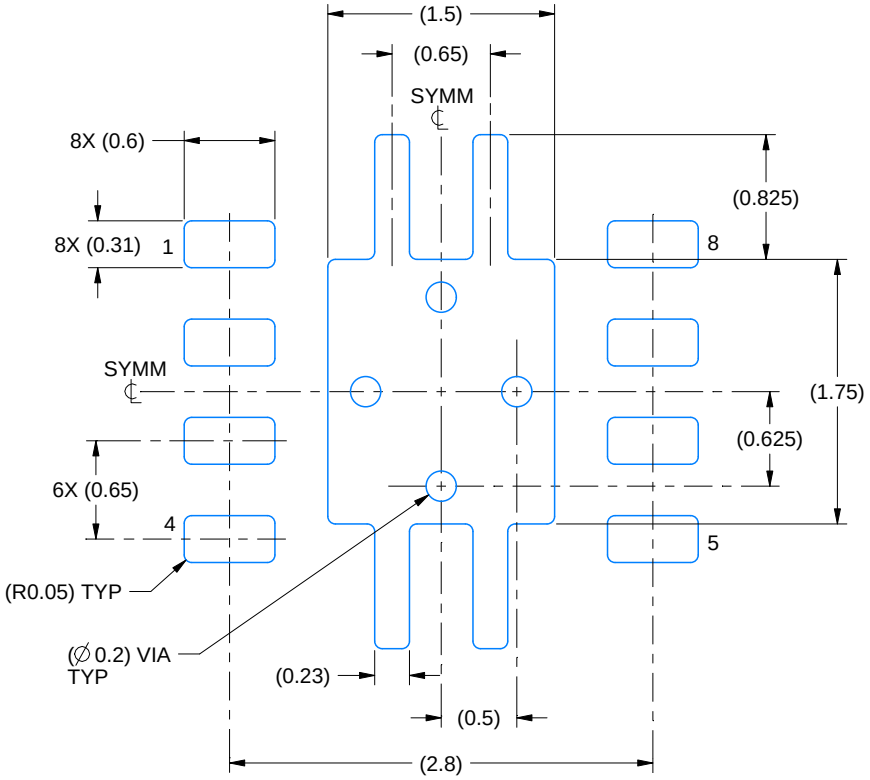
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

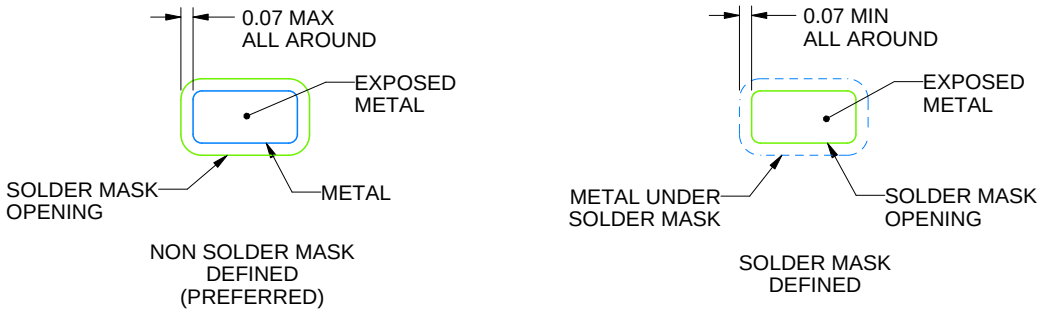
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

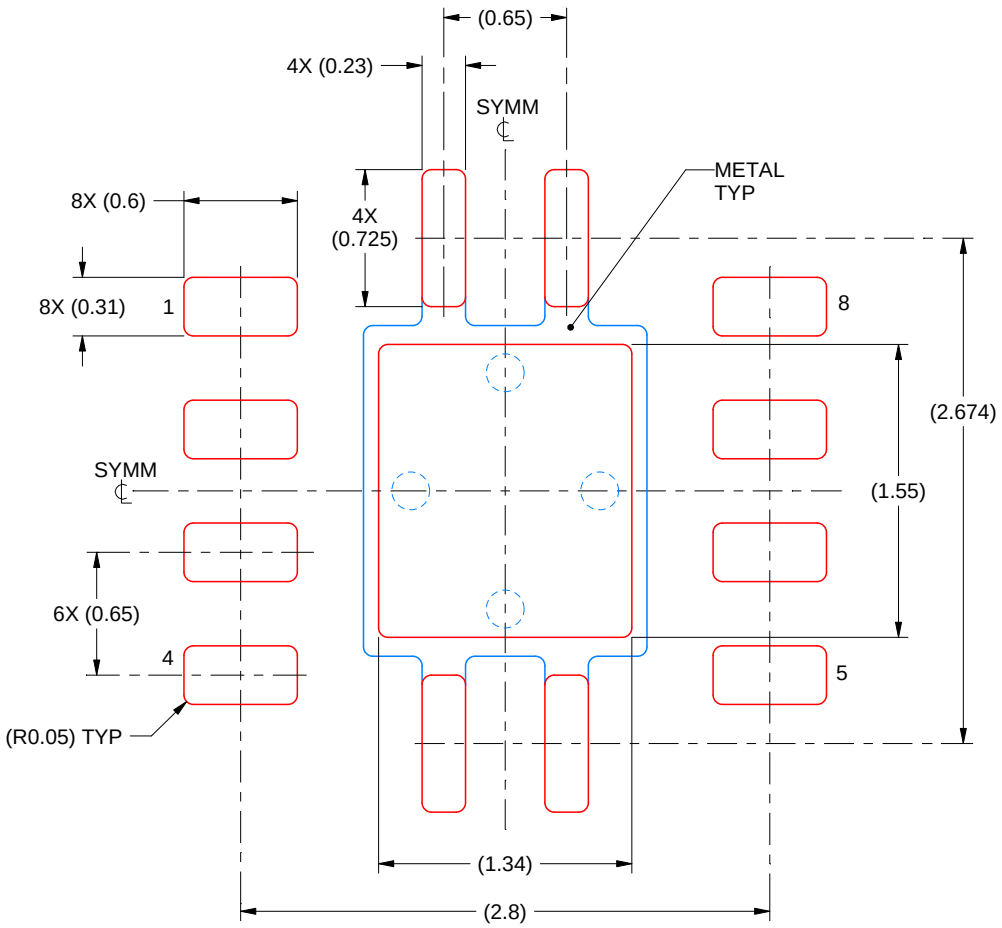


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

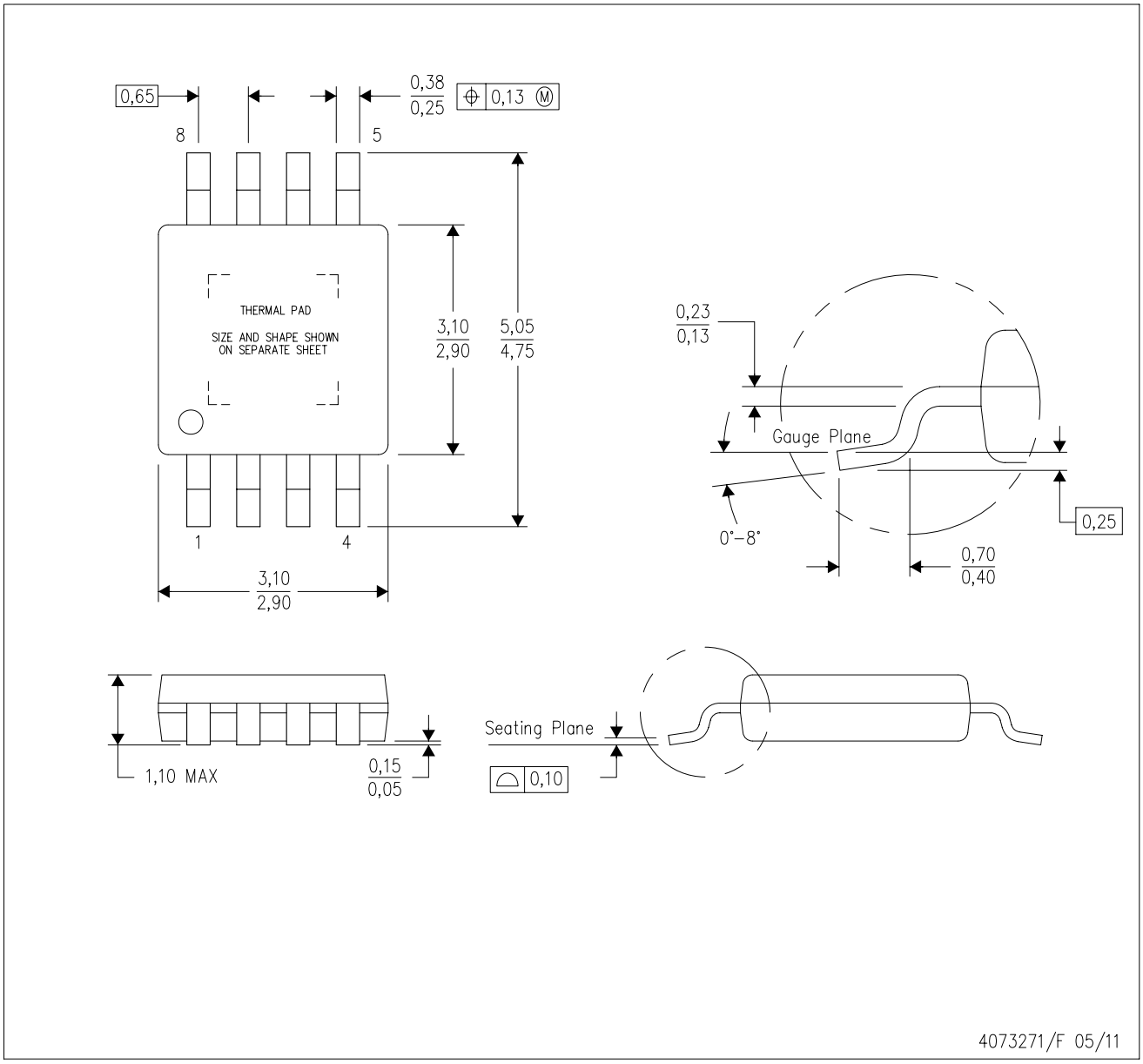
EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

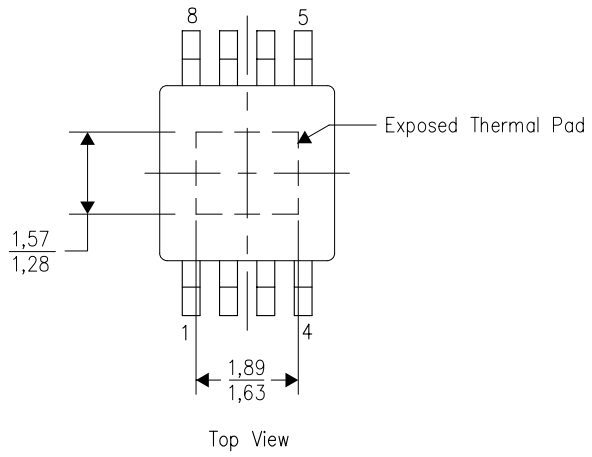
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

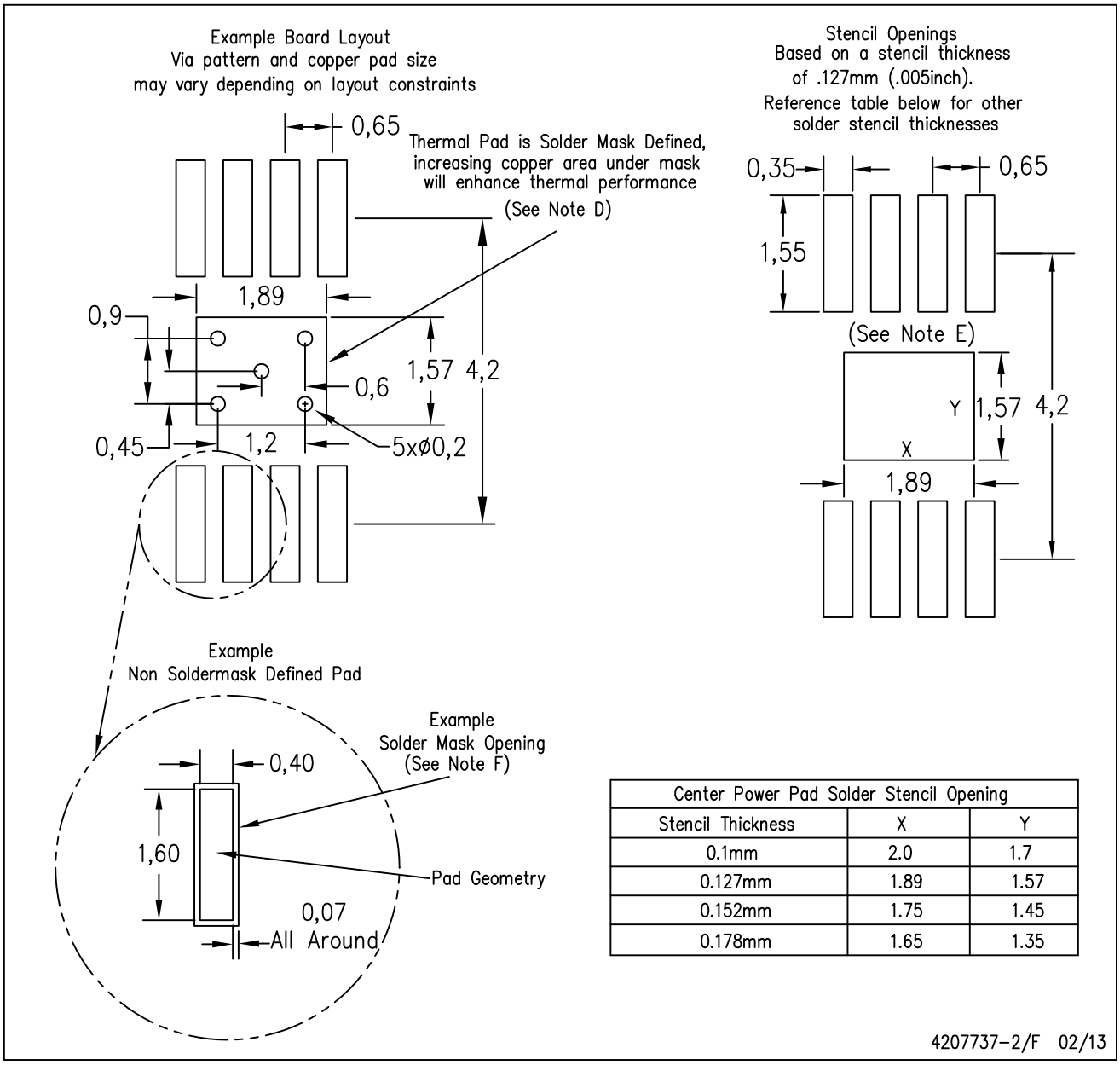
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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- **Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, $I_O = \pm 8$ mA**
- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.7 μs Typ With 5-mV Overdrive**
- **Single Supply Operation . . . 3 V to 16 V**
  TLC3704M . . . 4 V to 16 V
- **On-Chip ESD Protection**

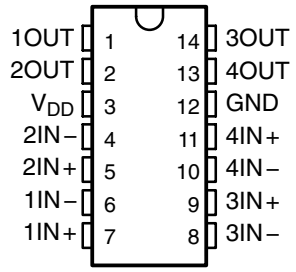
description

The TLC3704 consists of four independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use 1/20th the power for similar response times. The push-pull CMOS output stage drives capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

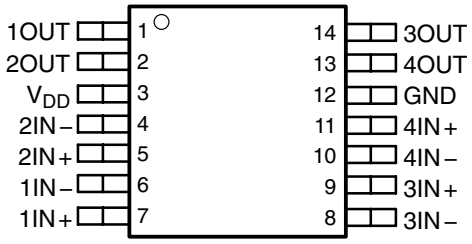
Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3704C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3704I is characterized for operation over the extended industrial temperature range of – 40°C to 85°C. The TLC3704M is characterized for operation over the full military temperature range of – 55°C to 125°C. The TLC3704Q is characterized for operation from – 40°C to 125°C.

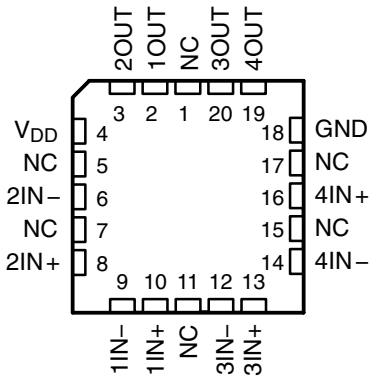
D, J, OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

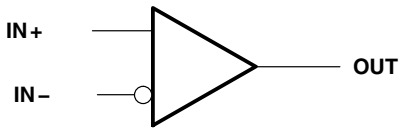


FK PACKAGE
(TOP VIEW)



NC – No internal connection

symbol (each comparator)

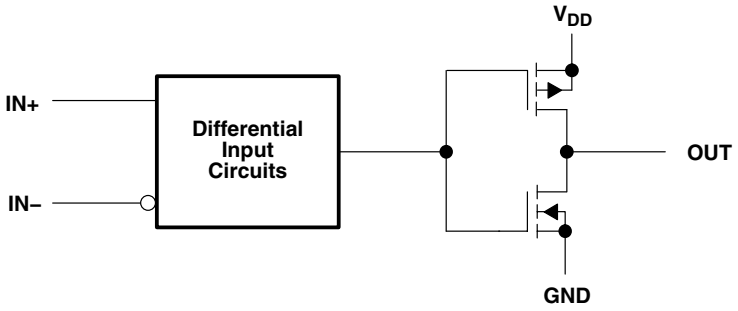


AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE				
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	5 mV	TLC3704CD	—	—	TLC3704CN	TLC3704CPW
–40°C to 85°C	5 mV	TLC3704ID	—	—	TLC3704IN	TLC3704IPW
–55°C to 125°C	5 mV	TLC3704MD	TLC3704MFK	TLC3704MJ	—	—
–40°C to 125°C	5 mV	—	—	TLC3704QJ	—	—

The D and PW packages are available taped and reeled. Add R suffix to the device type (e.g., TLC3704CDR).

functional block diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ± 18 V
Input voltage range, V_I . . . . . –0.3 to V_{DD}
Output voltage range, V_O . . . . . –0.3 to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±20 mA
Total supply current into V_{DD} . . . . . 40 mA
Total current out of GND . . . . . 60 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC3704C . . . . . 0 to 70°C
TLC3704I . . . . . –40°C to 85°C
TLC3704M . . . . . –55°C to 125°C
TLC3704Q . . . . . –40°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	N/A
PW	675 mW	5.4 mW/°C	432 mW	351 mW	N/A

recommended operating conditions

	TLC3704C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC3704C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, $V_{IC} = V_{ICR}$min,	See Note 3	25°C		1.2	5	mV
				0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				70°C			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				0°C to 70°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				70°C		84		
				0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				70°C		85		
				0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				70°C			375	
I_{DD}	Supply current (all four comparators)	Outputs low,	No load	25°C		35	80	µA
				0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3704I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC3704I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, $V_{IC} = V_{ICR}$min,	See Note 3	25°C		1.2	5	mV
				–40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				85°C			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				–40°C to 85°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				85°C		84		
				–40°C		83		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				85°C		85		
				–40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				85°C			400	
I_{DD}	Supply current (all four comparators)	Outputs low,	No load	25°C		35	80	µA
				–40°C to 85°C			125	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3704M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC3704M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, $V_{IC} = V_{ICR}$min,	See Note 3	25°C		1.2	5	mV
				–55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				–55°C to 125°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				125°C		83		
				–55°C		82		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		85		
				–55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				125°C			500	
I_{DD}	Supply current (all four comparators)	Outputs low,	No load	25°C		35	80	μA
				–55°C to 125°C			175	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3704Q			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	–0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC3704Q			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, $V_{IC} = V_{ICR}$min, See Note 3	25°C		1.2	5	mV
			–40°C to 125°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			–40°C to 125°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		83		
			–40°C		83		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			–40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = –4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OH} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (all four comparators)	Outputs low, No load	25°C		35	80	µA
			–40°C to 125°C			175	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC3704C, TLC3704I TLC3704M, TLC3704Q			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4-V step at IN+			1.1		
t_{PHL}	Propagation delay time, high-to-low-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4-V step at IN+			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

† Simultaneous switching of inputs causes degradation in output response.

PRINCIPLES OF OPERATION

LinCMOS process

The LinCMOS process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS products. Direct further questions to the nearest TI field sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented on the next page.

All input and output pins on LinCMOS and Advanced LinCMOS products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

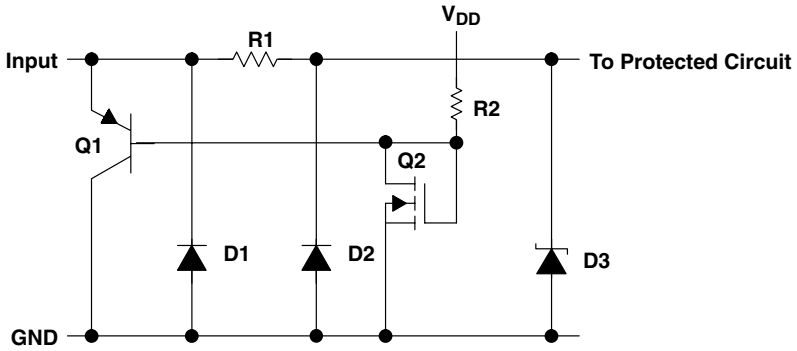


Figure 1. LinCMOS ESD-Protection Schematic

PRINCIPLES OF OPERATION

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded, and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 2 and 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

PRINCIPLES OF OPERATION

circuit-design considerations (continued)

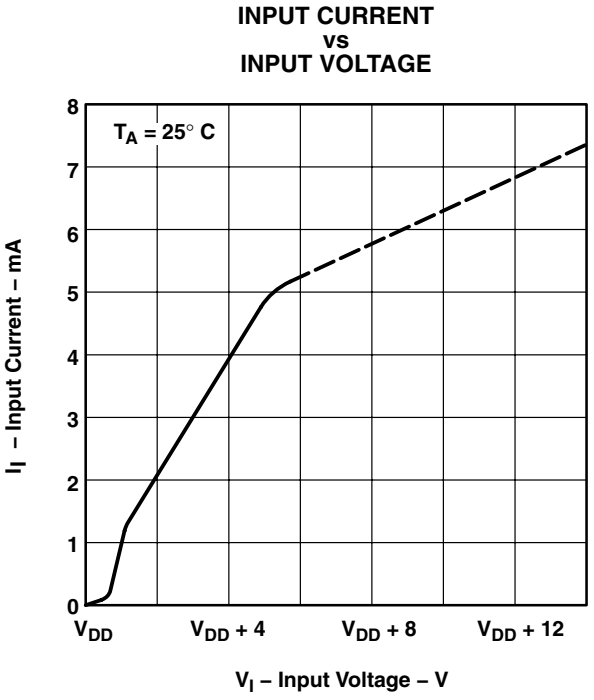


Figure 2

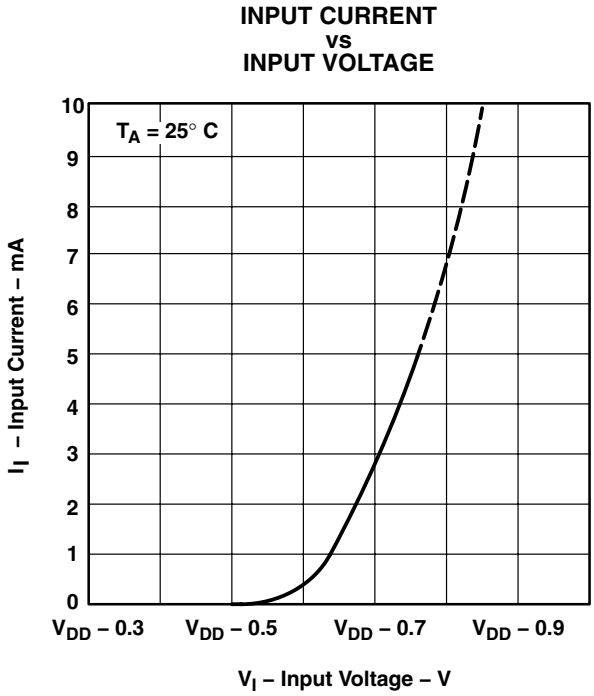
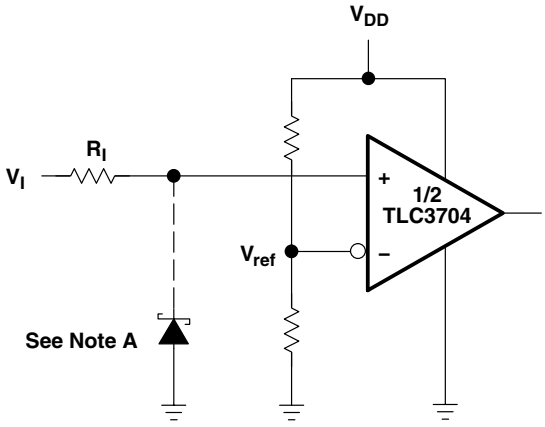


Figure 3



Positive Voltage Input Current Limit :

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit :

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

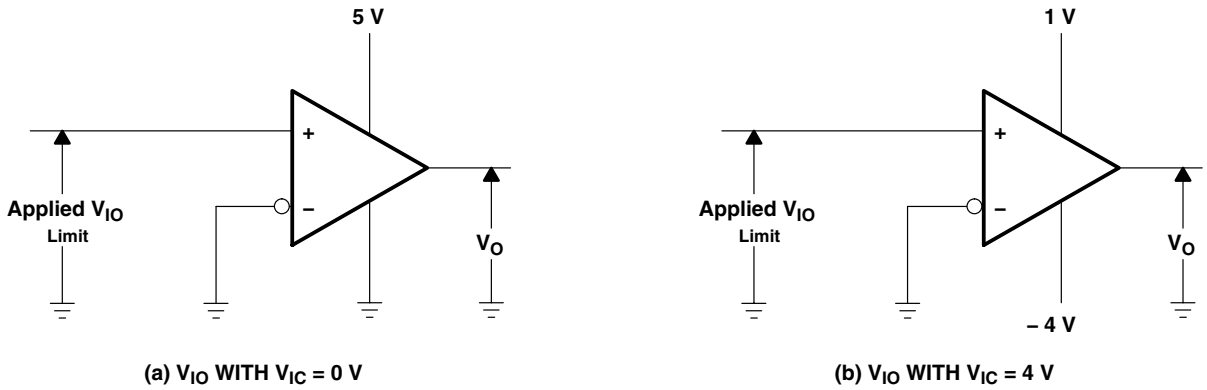
Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS Comparator

PARAMETER MEASUREMENT INFORMATION

The TLC3704 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 5(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides an increase in the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

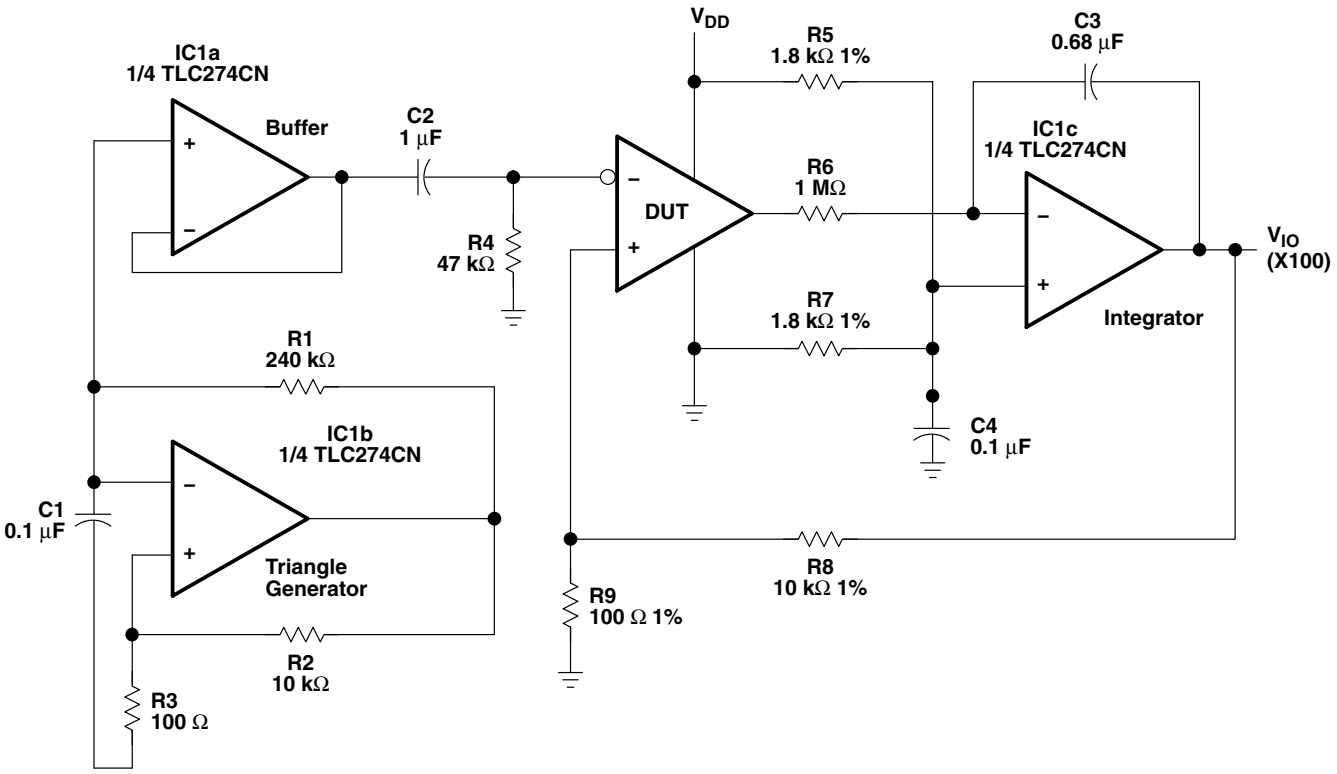
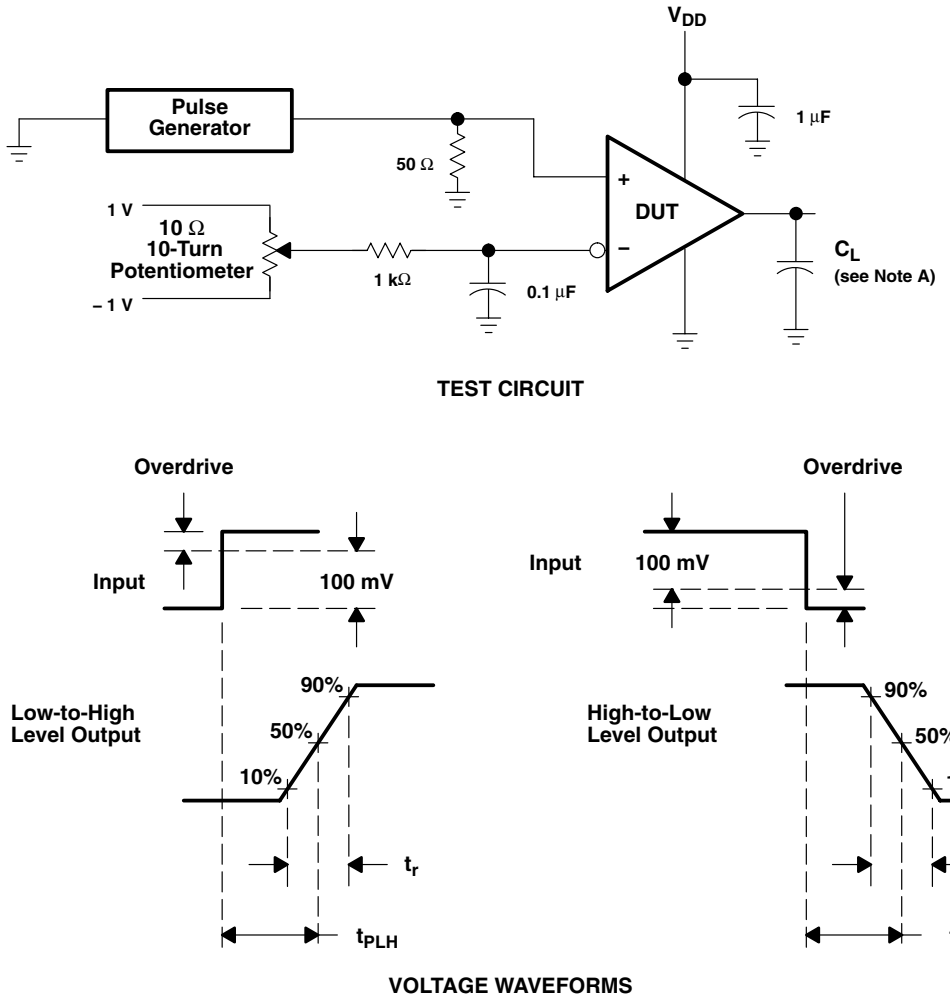


Figure 6. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 7, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	8
I_{IB}	Input bias current	vs Free-air temperature	9
CMRR	Common-mode rejection ratio	vs Free-air temperature	10
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	11
V_{OH}	High-level output current	vs Free-air temperature vs High-level output current	12 13
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	Supply current response to an output voltage transition		17
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t_{PHL}	High-to-low-level output response time	vs Supply voltage	21
I_{DD}	Supply current	vs Frequency vs Supply voltage vs Free-air temperature	22 23 24

DISTRIBUTION OF INPUT OFFSET VOLTAGE†

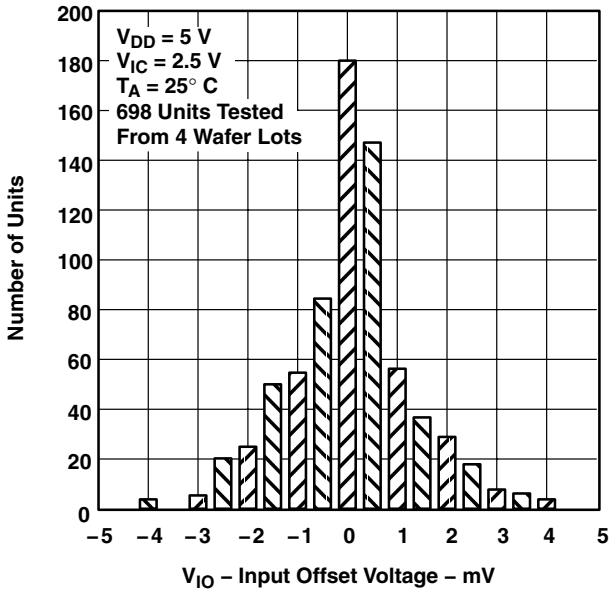

Figure 8

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE†

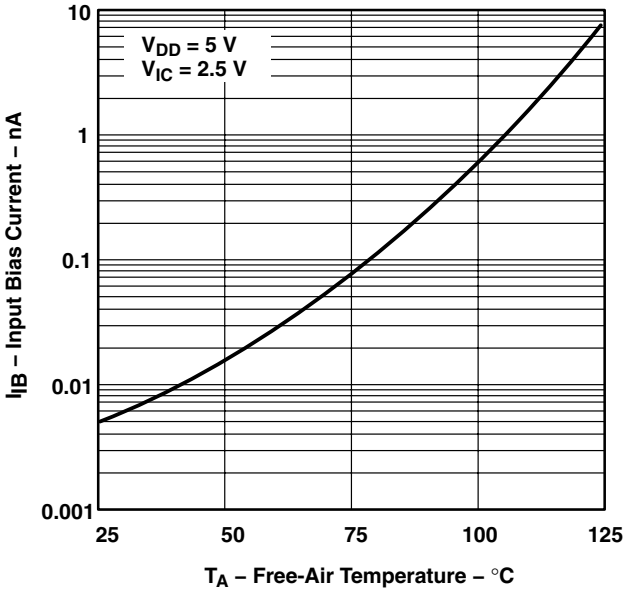

Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

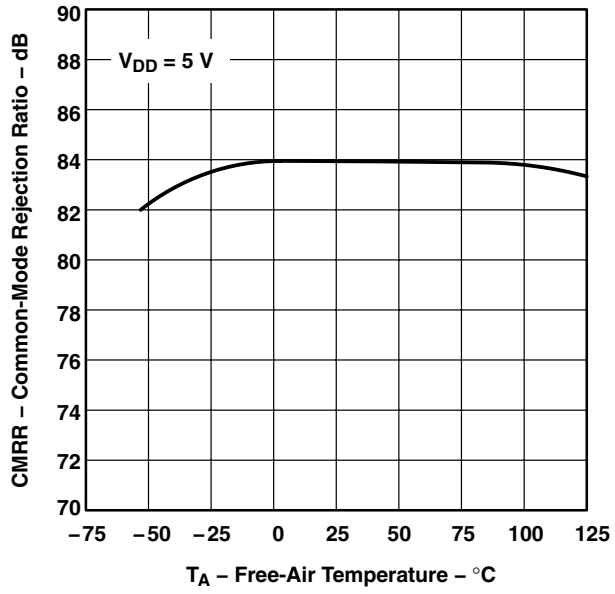

Figure 10

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

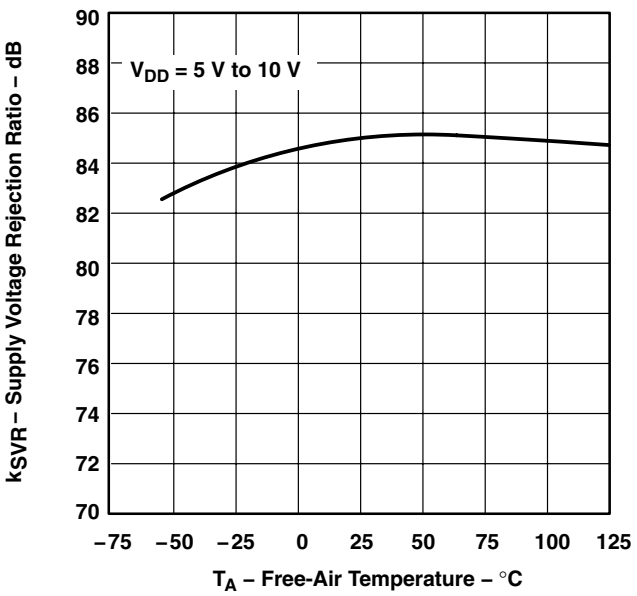

Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

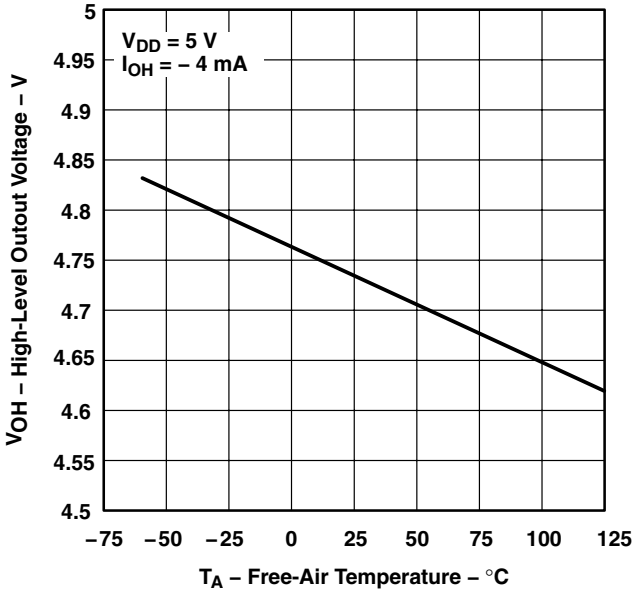

Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

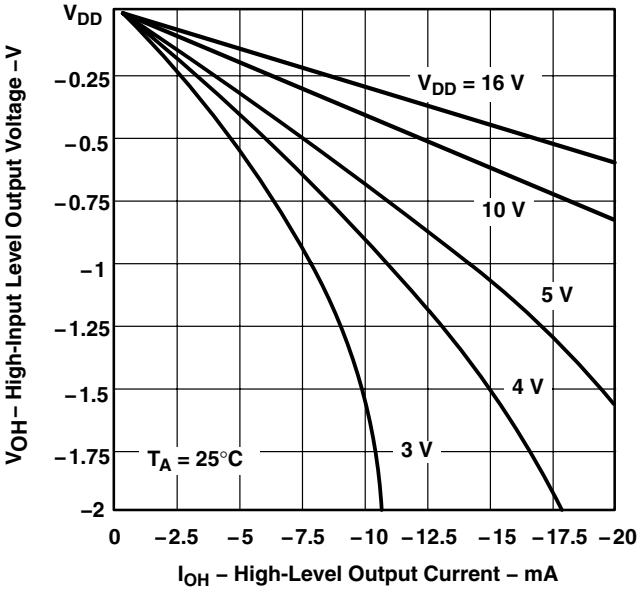

Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

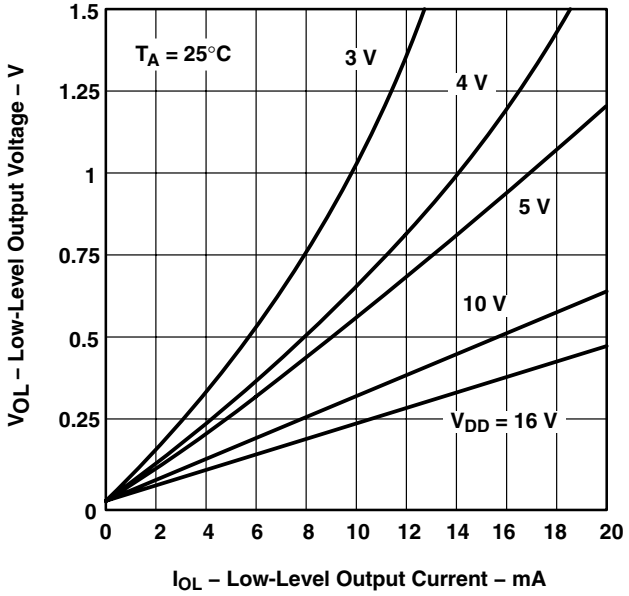

Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

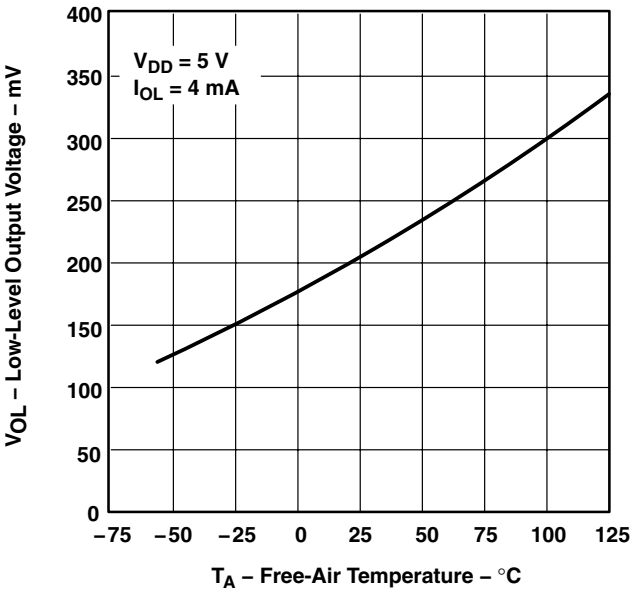

Figure 15

OUTPUT TRANSITION TIME vs LOAD CAPACITANCE

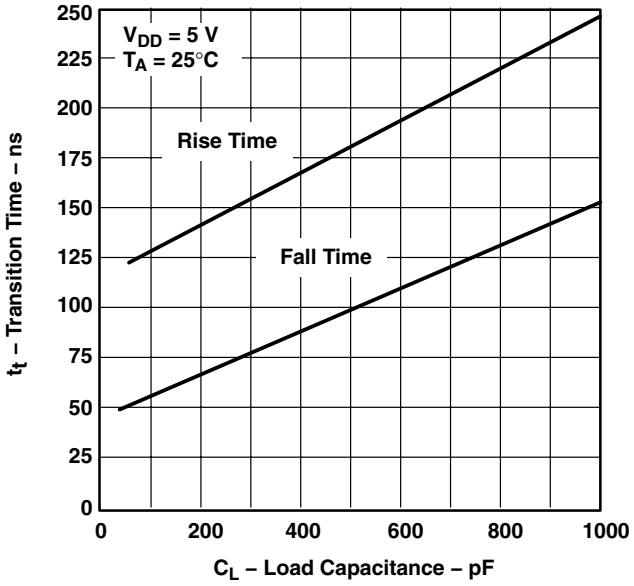

Figure 16

SUPPLY CURRENT RESPONSE TO AN OUTPUT VOLTAGE TRANSITION

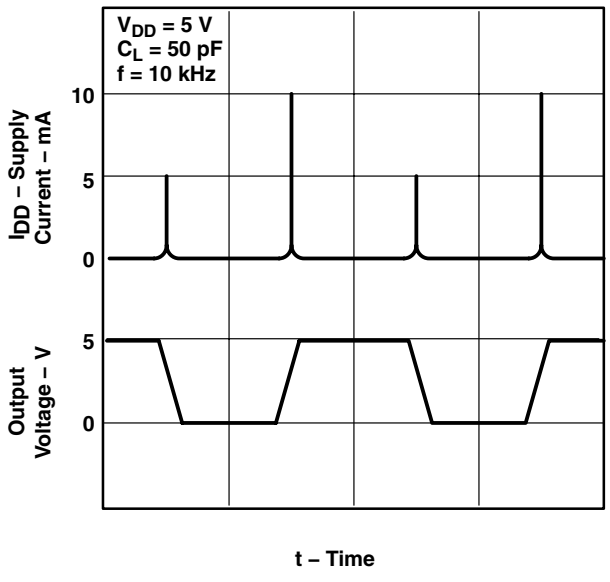

Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

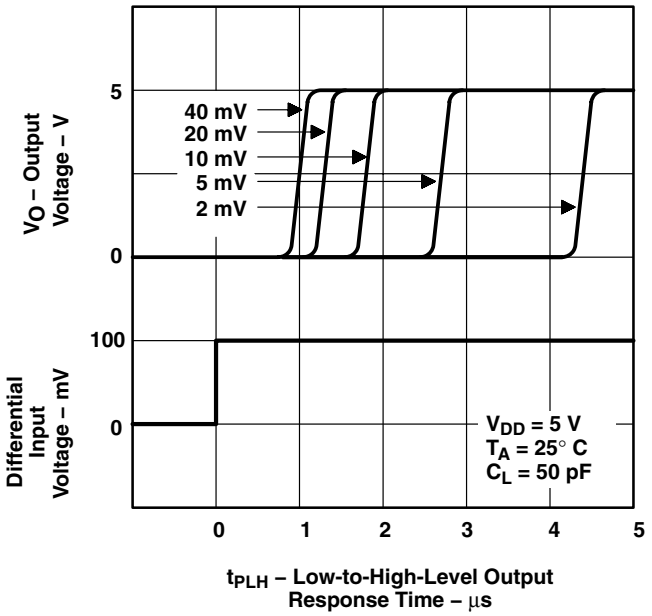

Figure 18

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

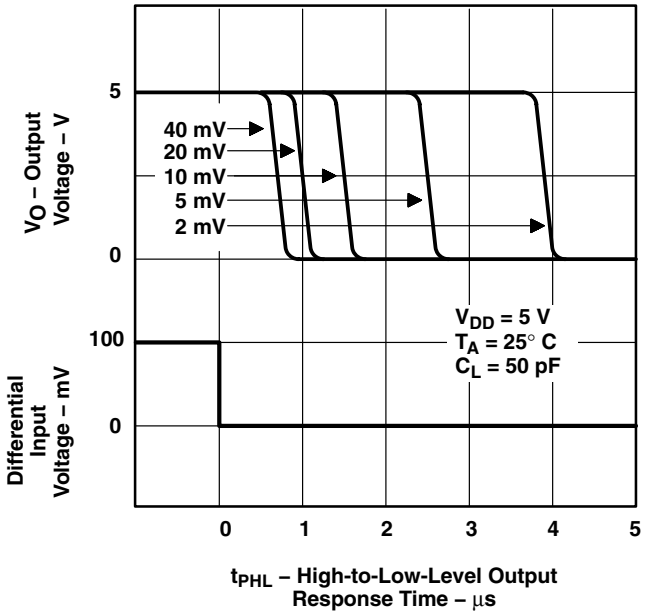

Figure 19

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

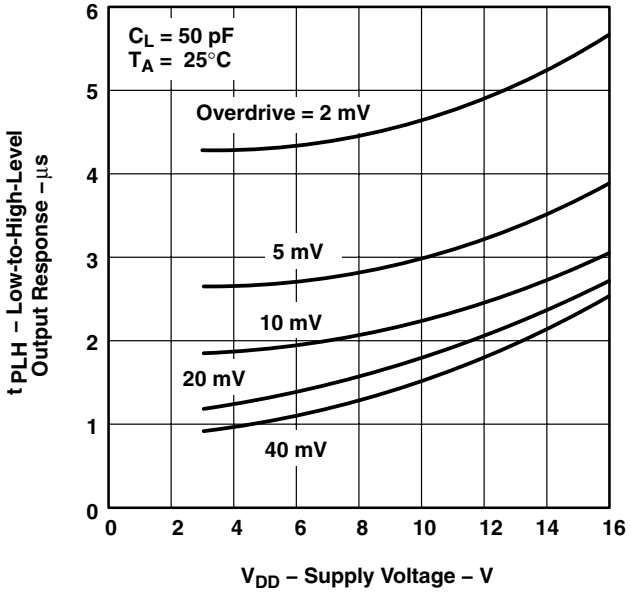

Figure 20

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

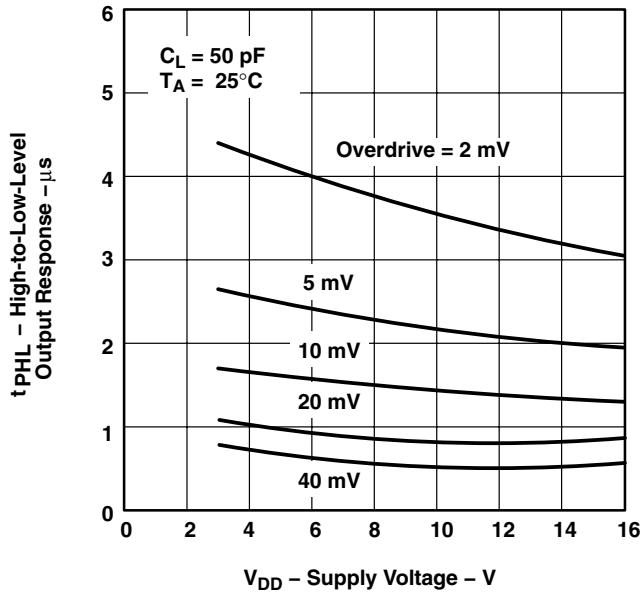

Figure 21

TYPICAL CHARACTERISTICS†

AVERAGE SUPPLY CURRENT (PER COMPARATOR) vs FREQUENCY

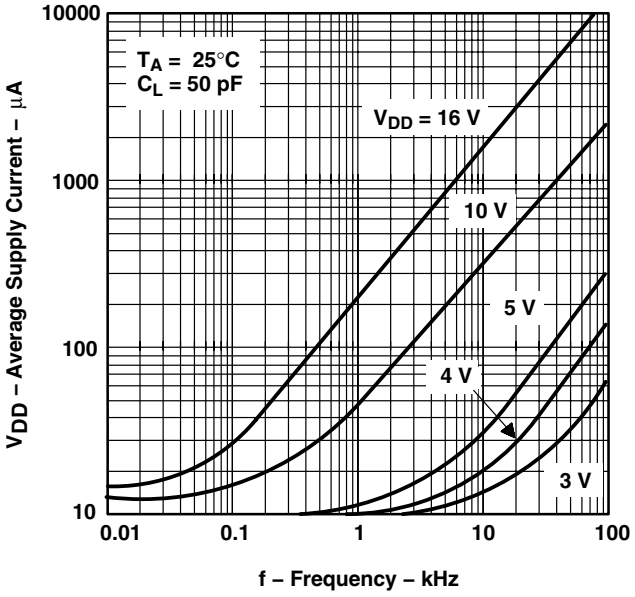

Figure 22

SUPPLY CURRENT vs SUPPLY VOLTAGE

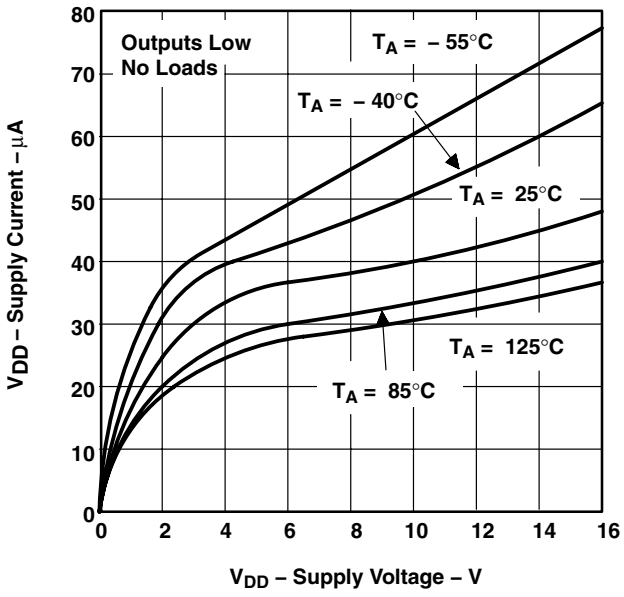

Figure 23

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

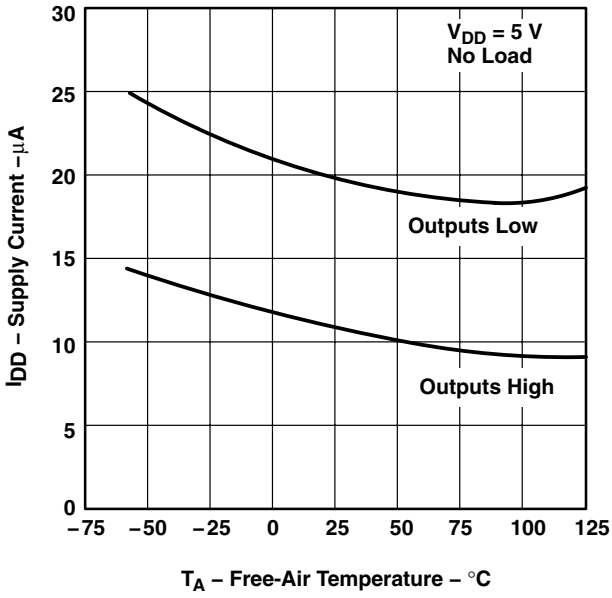

Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between – 0.2 V and 4 V to ensure proper device operation. To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) that is positioned as close to the device as possible.

Output and supply current limitations should be watched carefully since the TLC3704 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground can only be an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC3704 has internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

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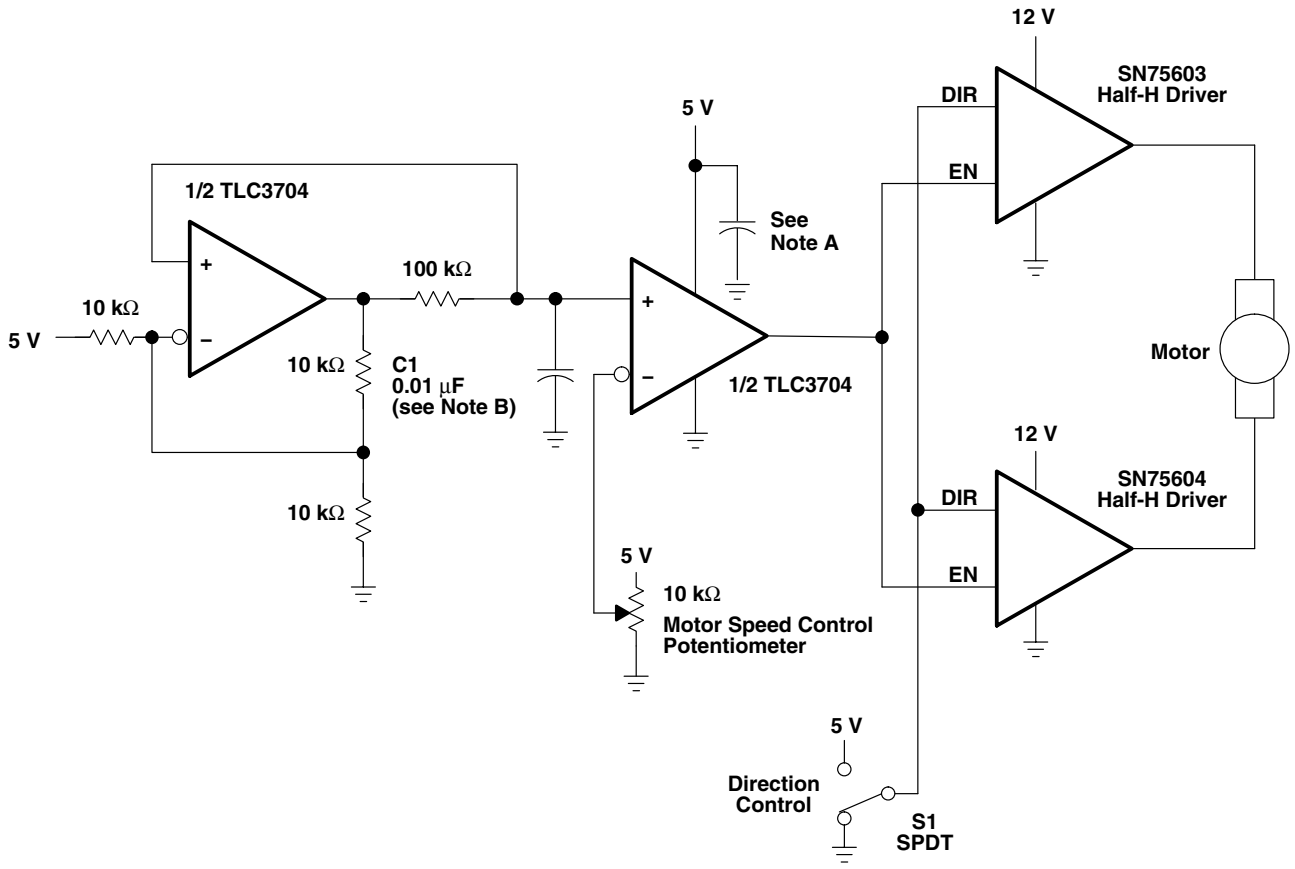
Micropower switching regulator	28

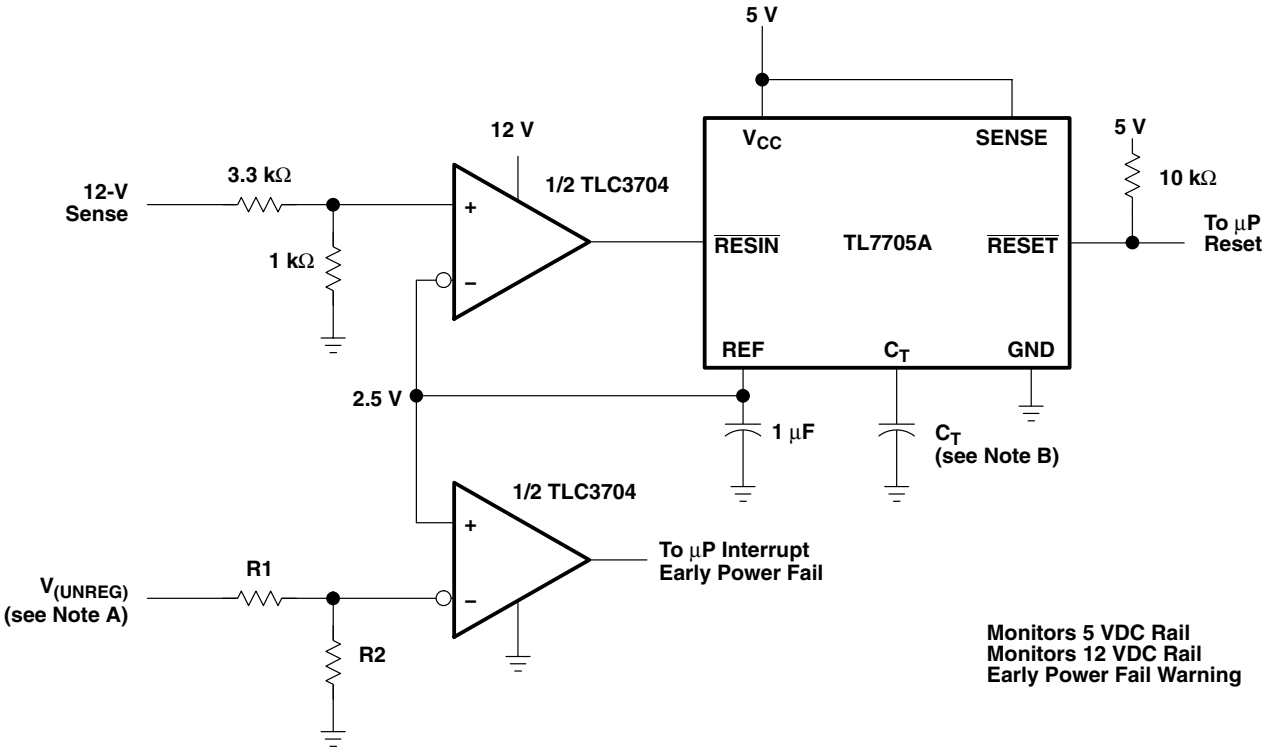
APPLICATION INFORMATION



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency

Figure 25. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

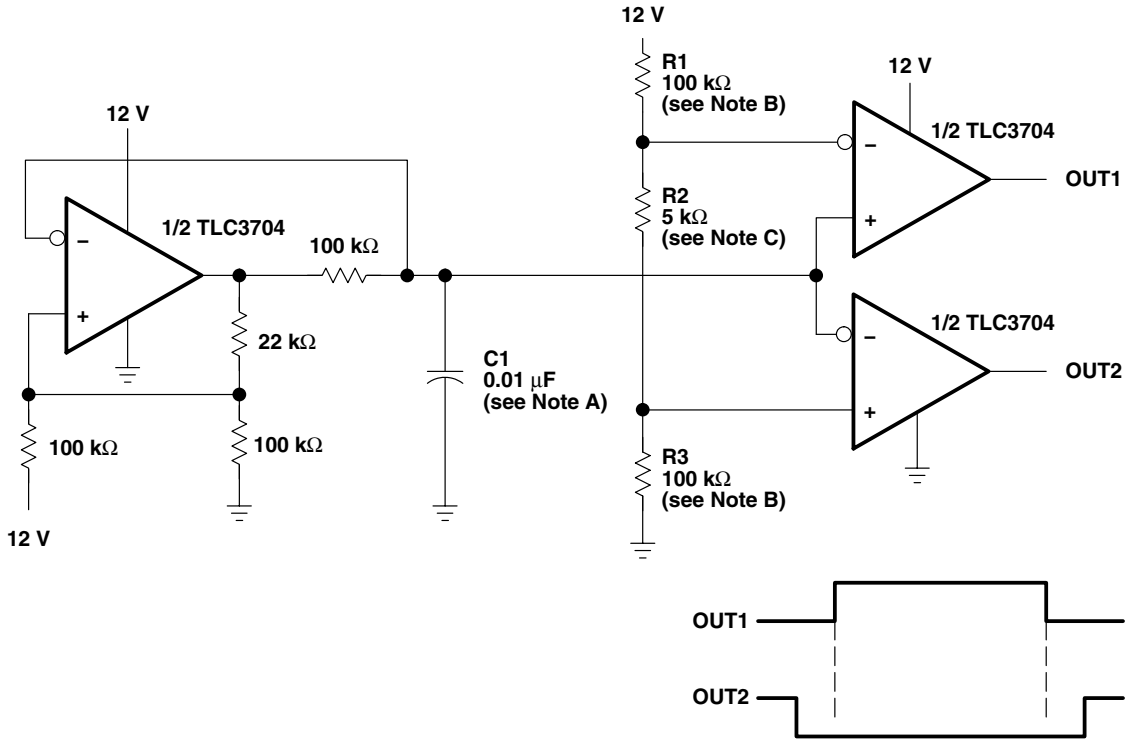


NOTES: A. $V_{(UNREG)} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 26. Enhanced Supply Supervisor

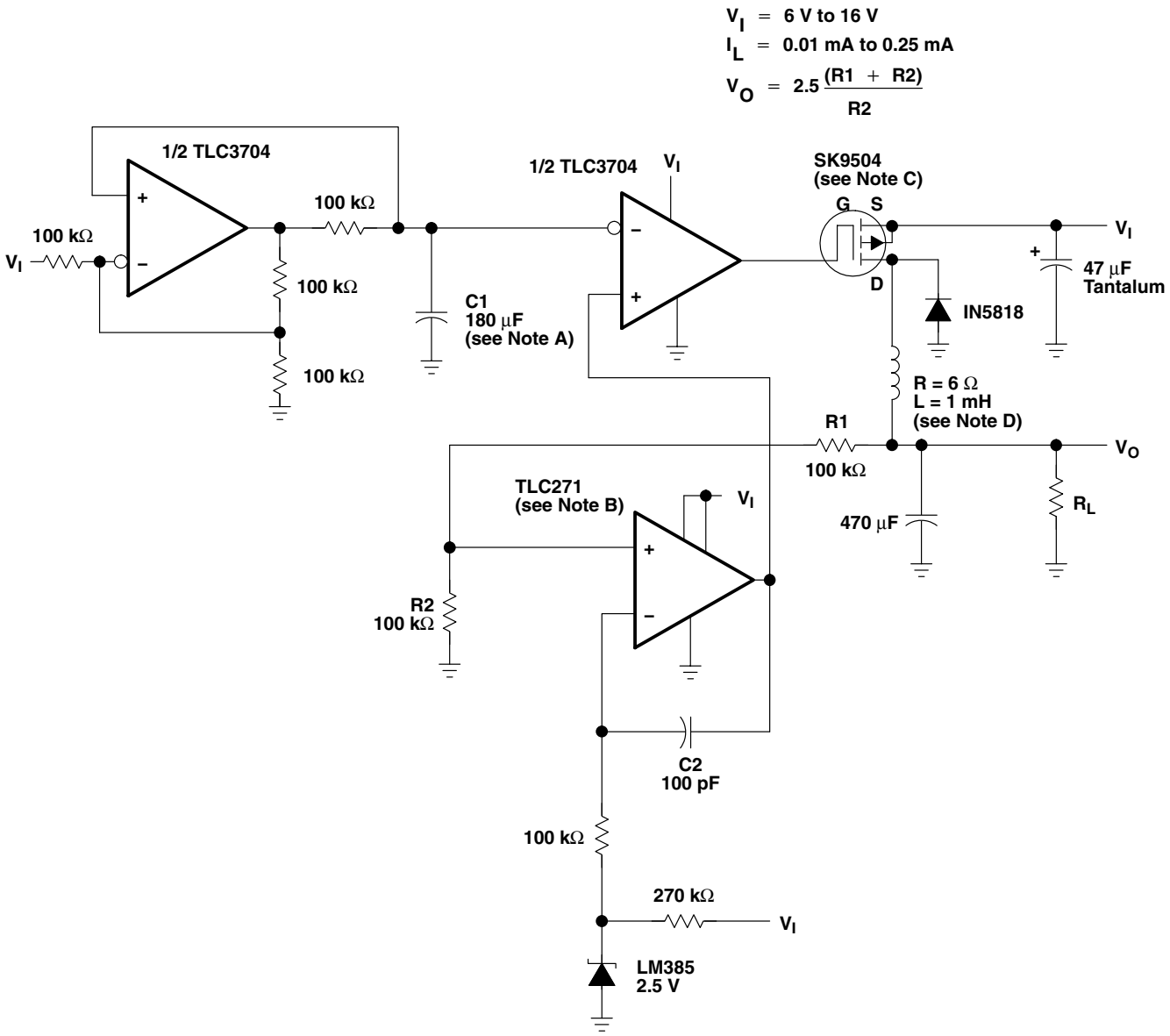
APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency where:
1/f = 1.85(100 kΩ)C1
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

Figure 27. Two-Phase Nonoverlapping Clock Generator

APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 – Tie pin 8 to pin 7 for low bias operation
C. SK9504 – VDS = 40 V
IDS = 1 Awill
D. To achieve microampere current drive, the inductance of the circuit must be increased.

Figure 28. Micropower Switching Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9096901M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9096901M2A TLC3704 MFKB	Samples
5962-9096901MCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9096901MCA TLC3704MJB	Samples
TLC3704CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3704C	Samples
TLC3704CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3704C	Samples
TLC3704CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC3704CN	Samples
TLC3704CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3704	Samples
TLC3704CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P3704	Samples
TLC3704CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P3704	Samples
TLC3704CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P3704	Samples
TLC3704ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC3704I	Samples
TLC3704IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC3704I	Samples
TLC3704IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC3704I	Samples
TLC3704IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC3704IN	Samples
TLC3704IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	P3704I	Samples
TLC3704IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	P3704I	Samples
TLC3704MD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC3704MD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC3704MDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PJ3704M	Samples
TLC3704MDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC3704MD	Samples
TLC3704MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9096901M2A TLC3704 MFKB	Samples
TLC3704MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9096901MCA TLC3704MJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC3704, TLC3704M :

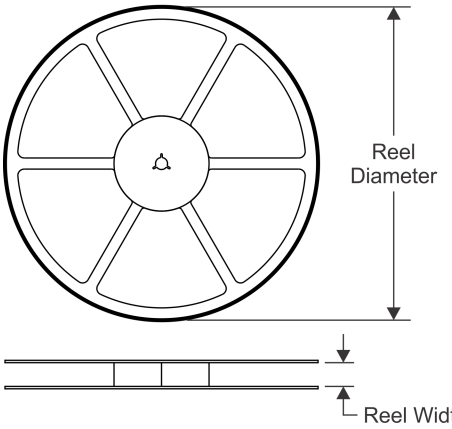
- Catalog: TLC3704
- Automotive: TLC3704-Q1, TLC3704-Q1
- Military: TLC3704M

NOTE: Qualified Version Definitions:

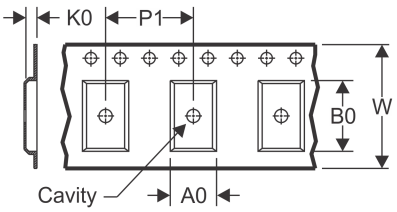
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

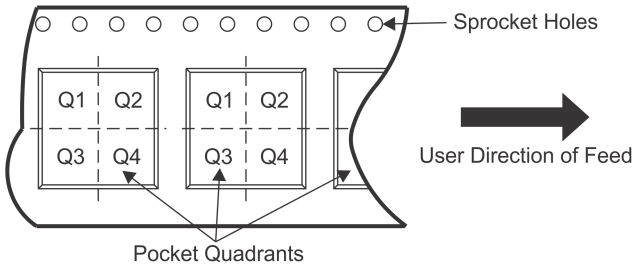


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

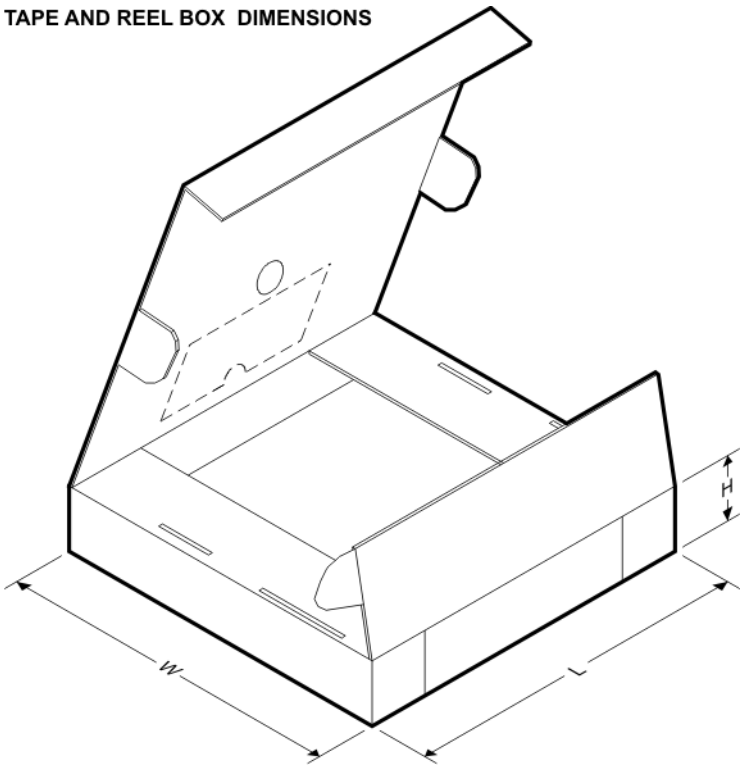
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3704CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC3704CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC3704CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC3704IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC3704IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC3704MDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



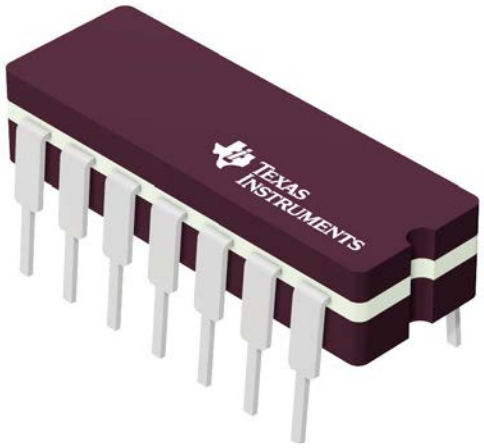
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3704CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC3704CNSR	SO	NS	14	2000	367.0	367.0	38.0
TLC3704CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC3704IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC3704IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC3704MDR	SOIC	D	14	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

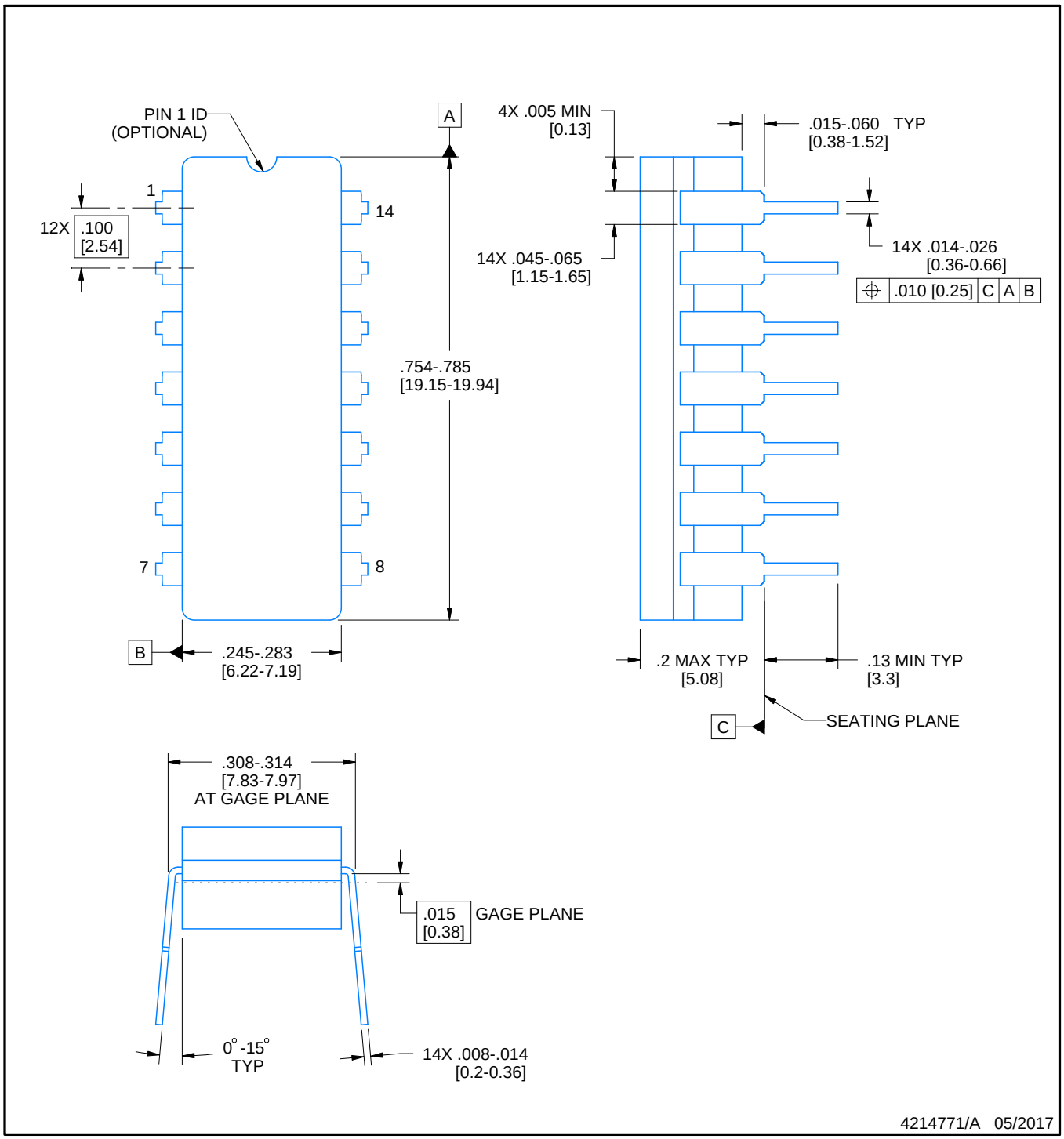
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

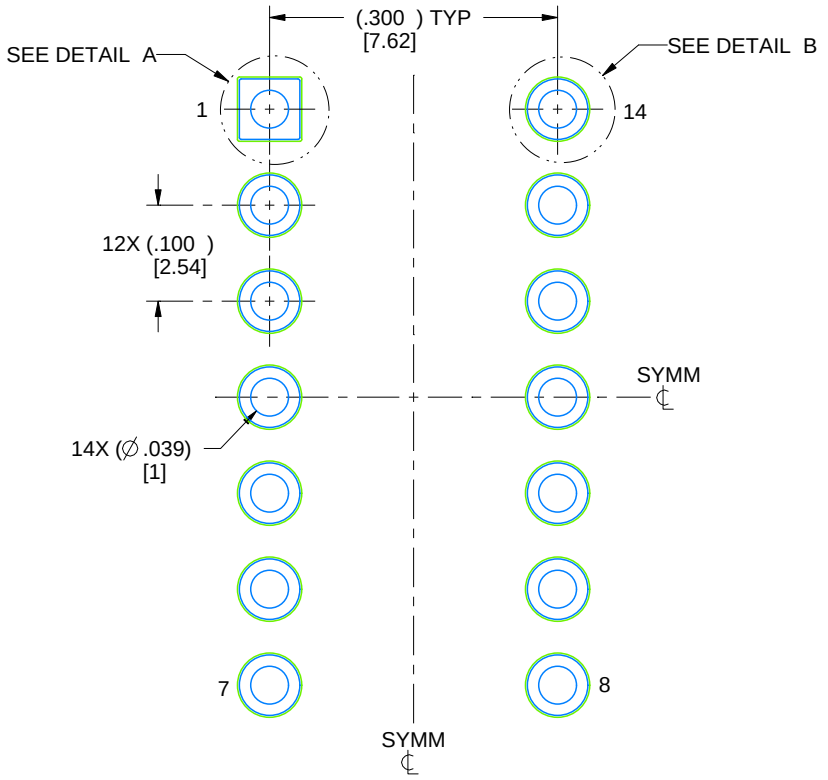
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

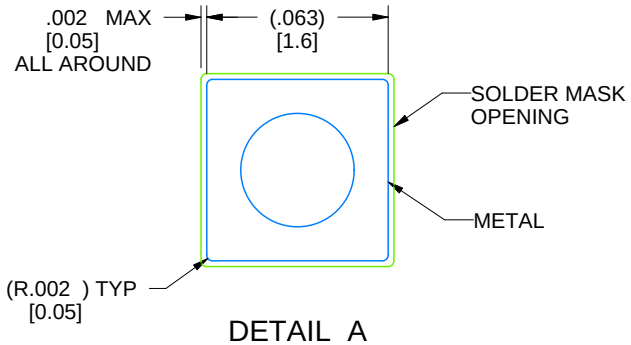
J0014A

CDIP - 5.08 mm max height

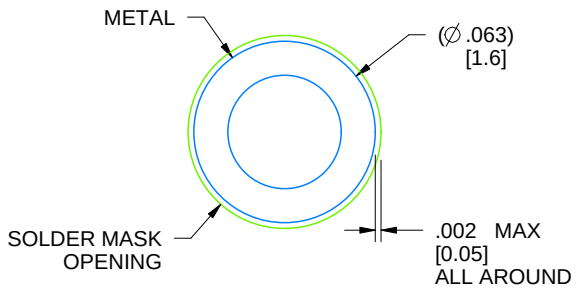
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



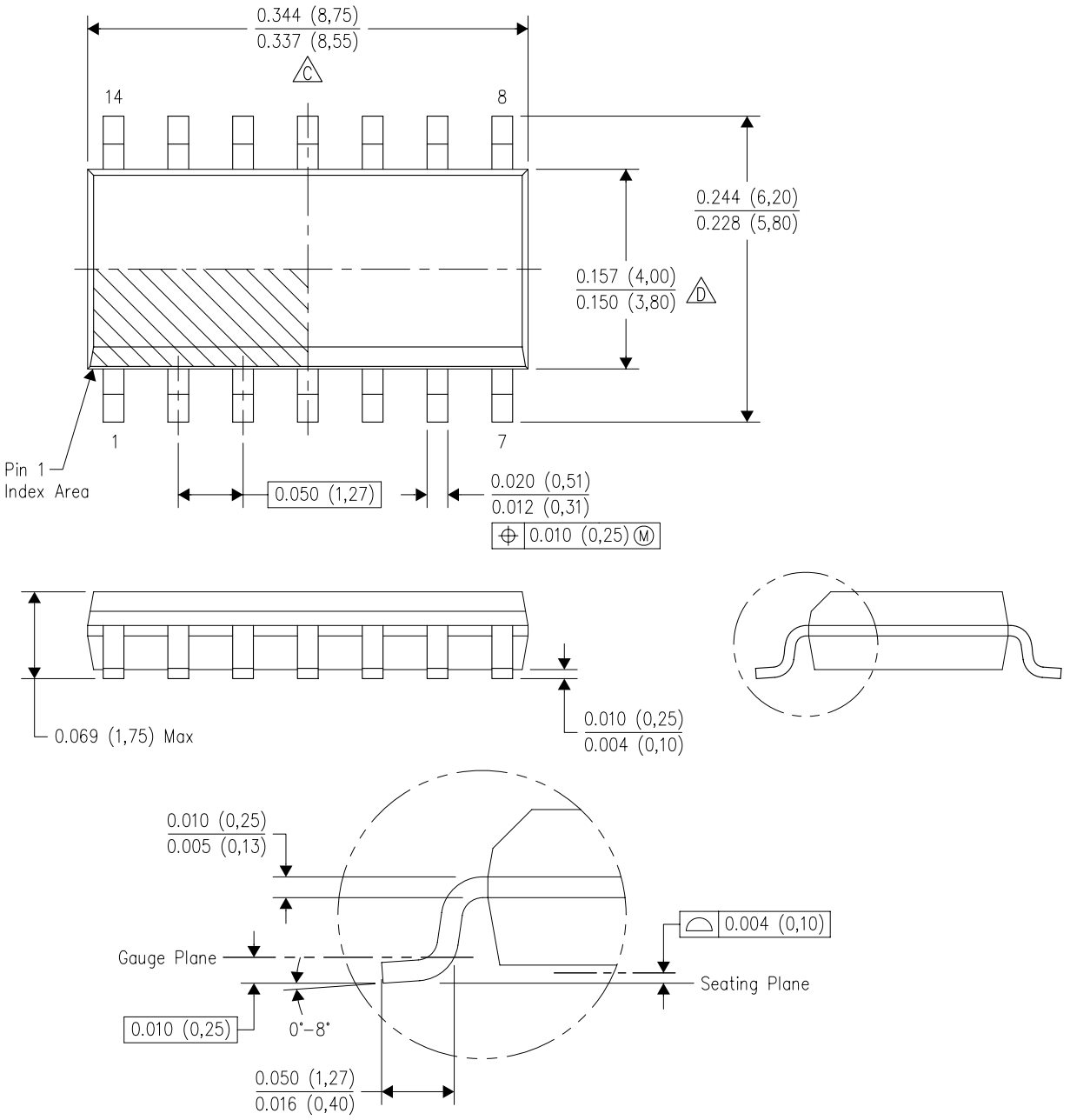
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

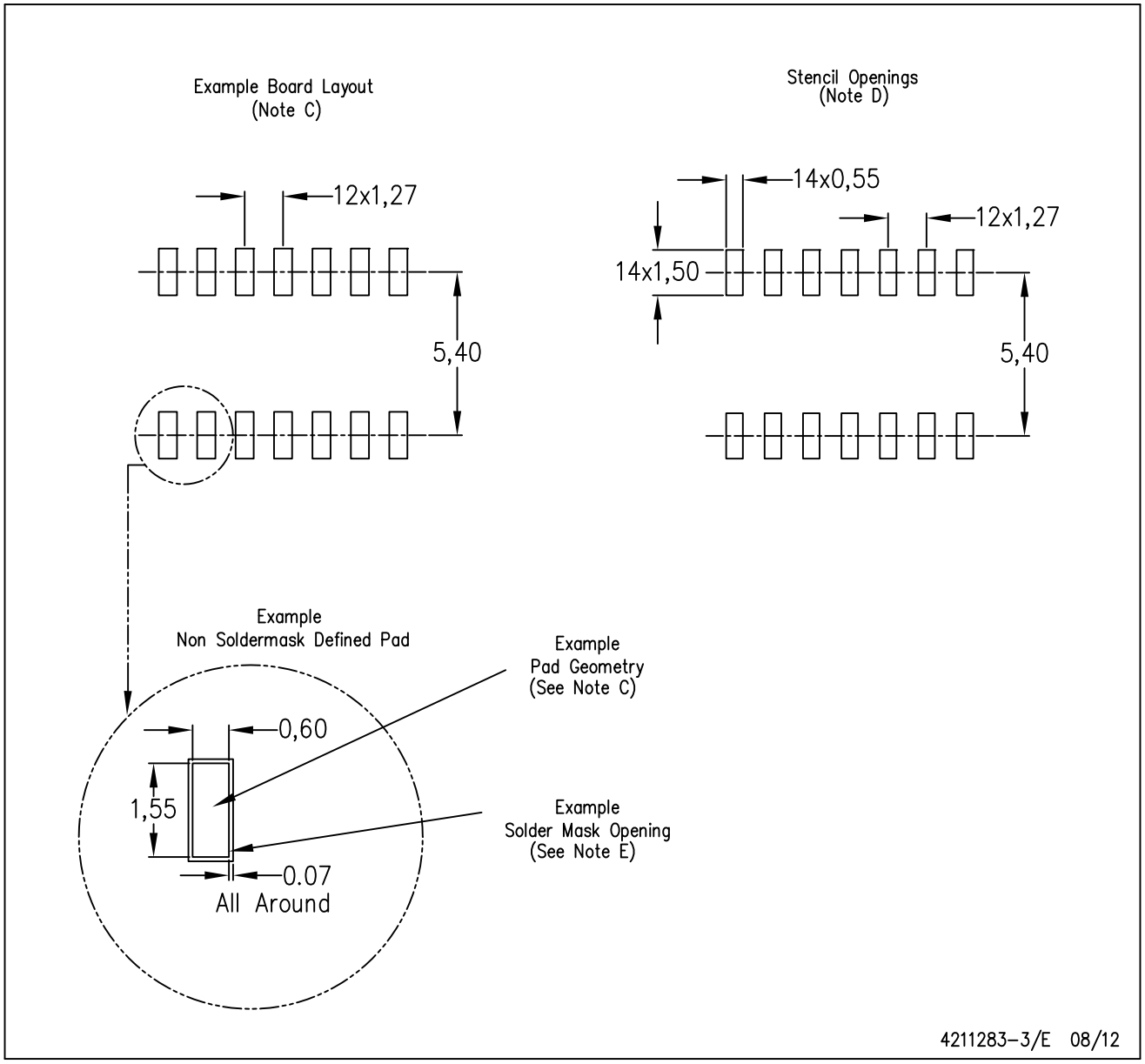
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

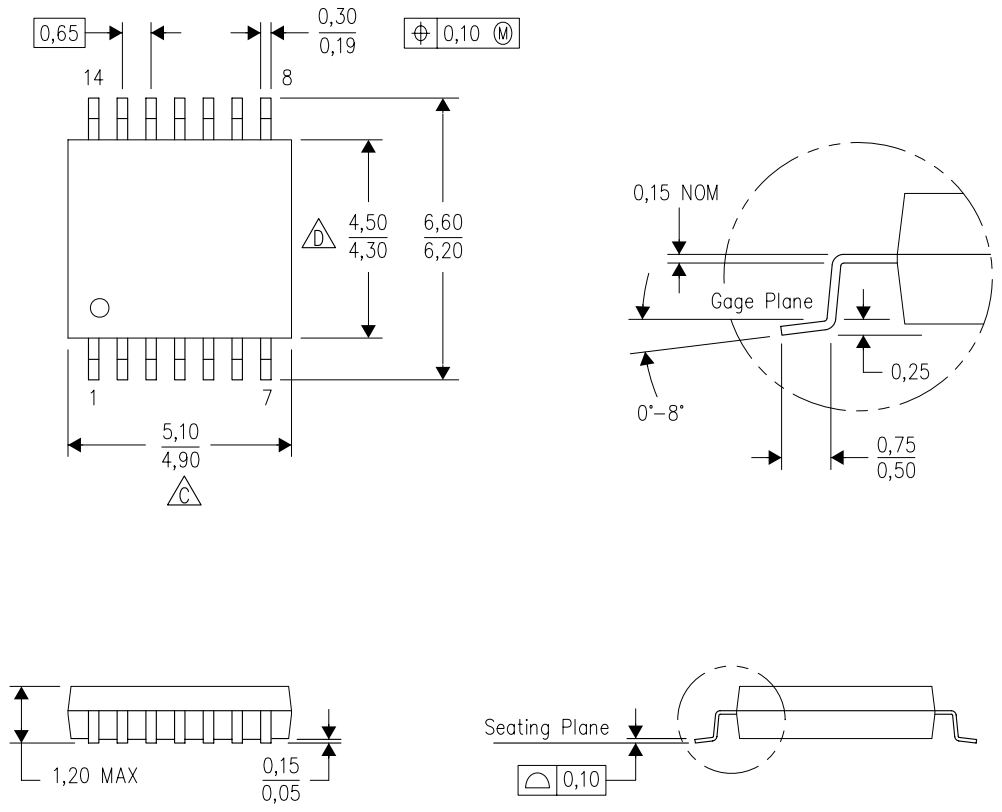
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



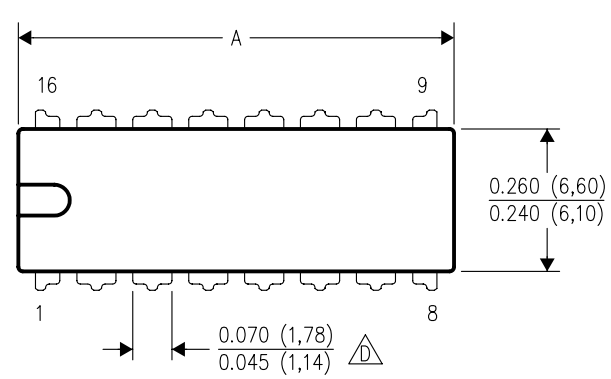
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

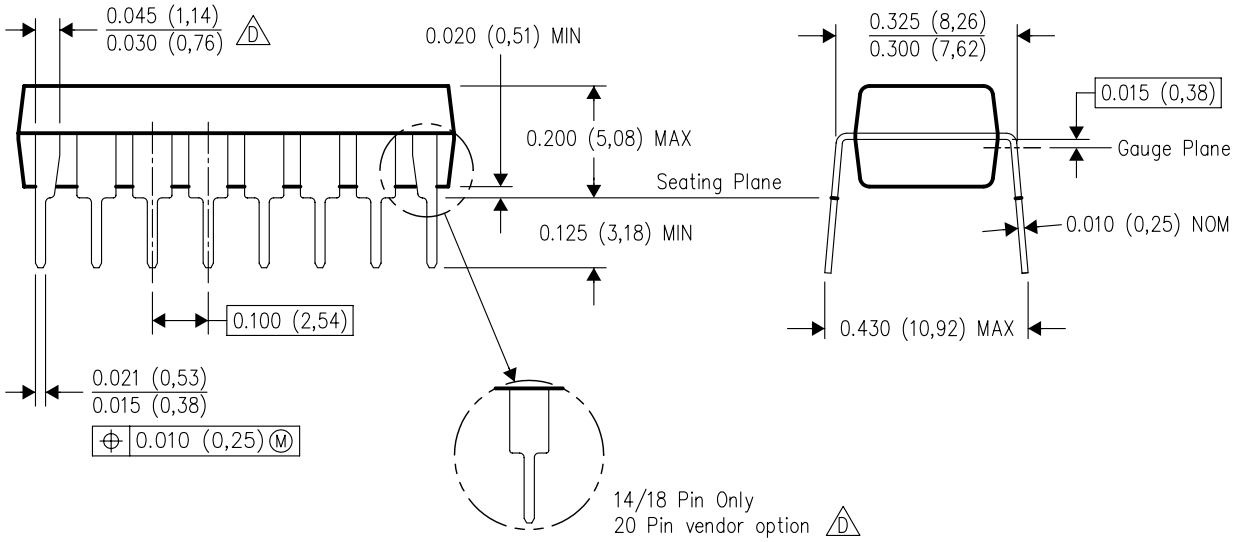
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

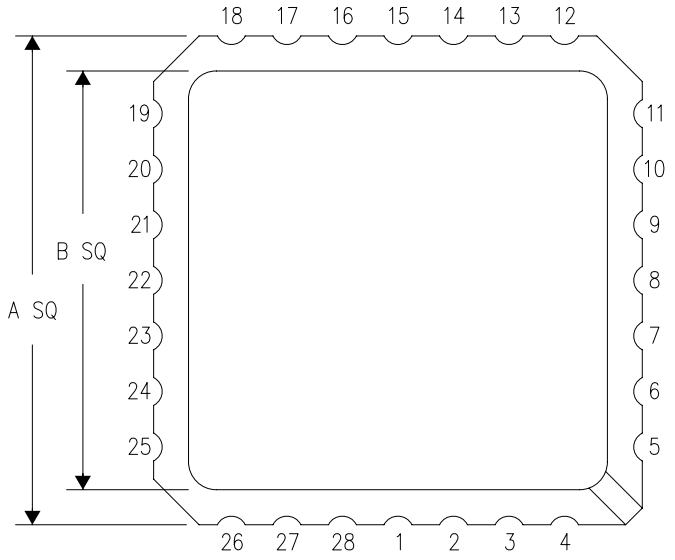


4040049/E 12/2002

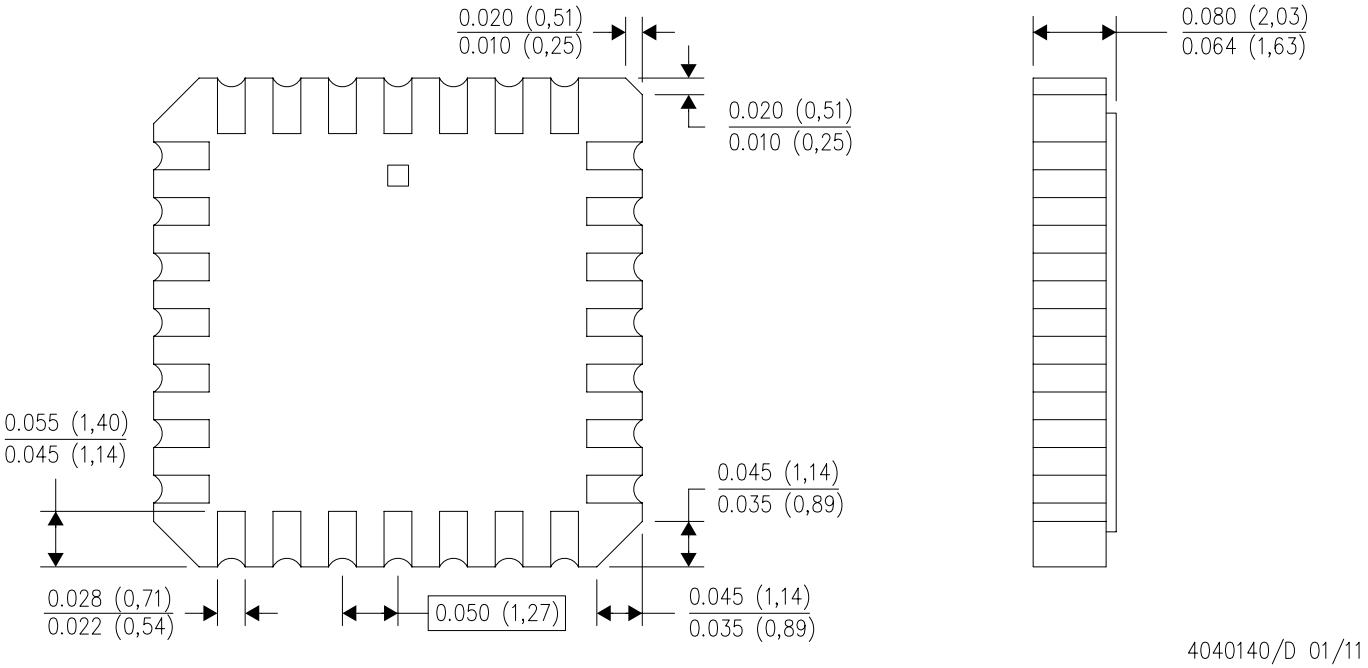
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



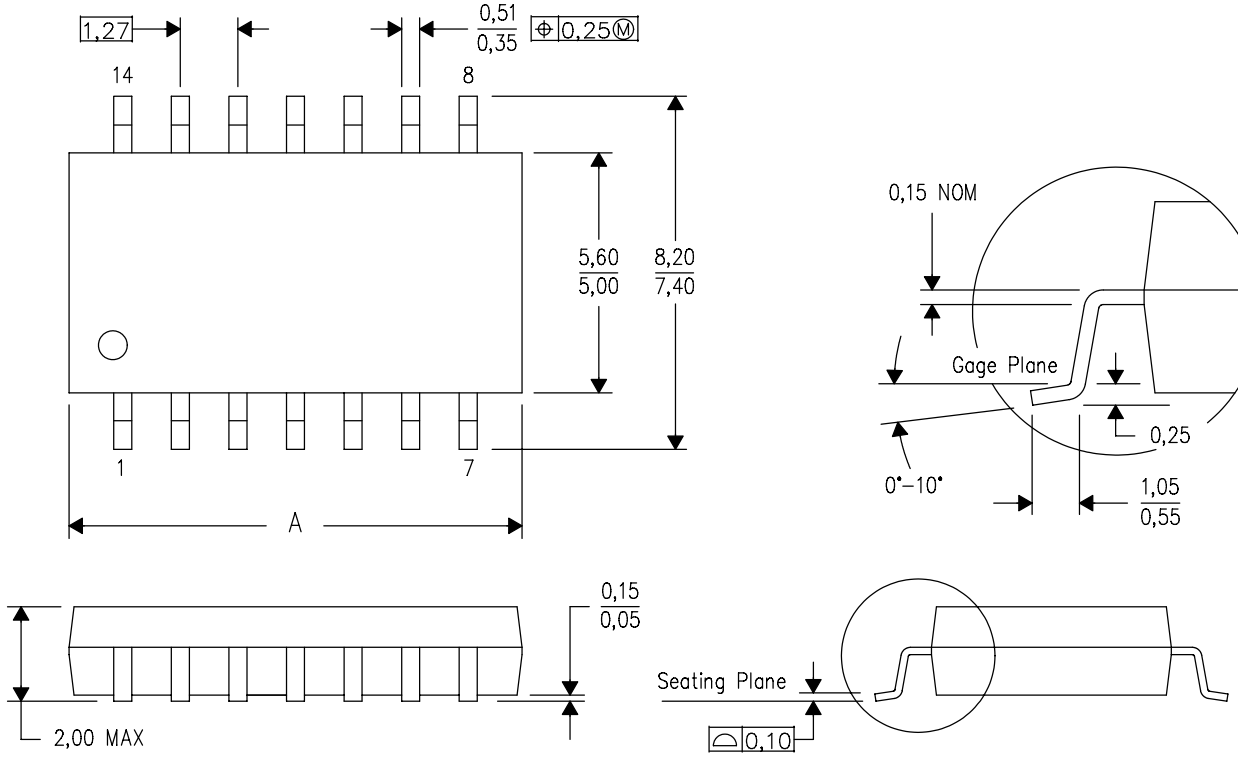
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

CAT5113

100-tap Digital Potentiometer (POT)

Description

The CAT5113 is a single digital POT designed as an electronic replacement for mechanical potentiometers. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5113 contains a 100-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_W. The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without affecting the stored setting. Wiper-control of the CAT5113 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digital POT can be used as a three-terminal resistive divider or as a two-terminal variable resistor.

Features

- 100-position Linear Taper Potentiometer
- Non-volatile EEPROM Wiper Storage
- 10 nA Ultra-low Standby Current
- Single Supply Operation: 2.5 V – 6.0 V
- Increment Up/Down Serial Interface
- Resistance Values: 1 kΩ, 10 kΩ, 50 kΩ and 100 kΩ
- Available in PDIP, SOIC, TSSOP and MSOP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Tamper-proof Calibrations
- Contrast, Brightness and Volume Controls
- Motor Controls and Feedback Systems
- Programmable Analog Functions

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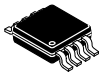
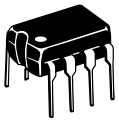
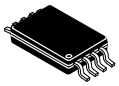
SOIC−8
V SUFFIX
CASE 751BD



MSOP−8
Z SUFFIX
CASE 846AD

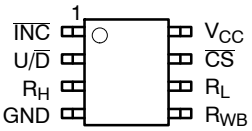


PDIP−8
L SUFFIX
CASE 646AA



TSSOP−8
Y SUFFIX
CASE 948AL

PIN CONFIGURATIONS



PDIP (L), SOIC (V), MSOP (Z)

TSSOP (Y)

(Top Views)

PIN FUNCTION

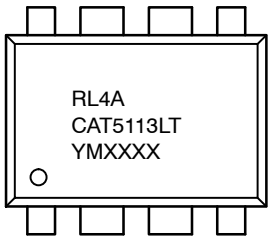
Pin Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_W	Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

DEVICE MARKING INFORMATION

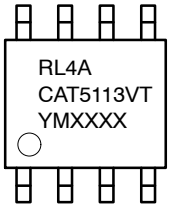
PDIP



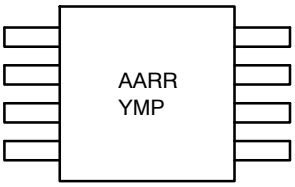
R = Resistance:
- 0 = 1 kΩ
- 2 = 10 kΩ
- 4 = 50 kΩ
- 5 = 100 kΩ

L = Assembly Location
4 = Lead Finish – NiPdAu
A = Product Revision (Fixed as “A”)
CAT5113L = Device Code (PDIP)
CAT5113V = Device Code (SOIC)
T = Temperature Range (Industrial)
Y = Production Year (Last Digit)
M = Production Month (1–9, A, B, C)
XXXX = Last Four Digits of Assembly Lot Number

SOIC



MSOP



AARR = CAT5113ZI–10–T3
AARC = CAT5113ZI–50–T3
AARG = CAT5113ZI–00–T3
Y = Production Year (Last Digit)
M = Production Month (1–9, A, B, C)
P = Product Revision

TSSOP

A3 = Device Code
R = Resistance:
- 2 = 10 kΩ
- 4 = 50 kΩ
- 5 = 100 kΩ

L = Assembly Location
4 = Lead Finish – NiPdAu
Y = Production Year (Last Digit)
M = Production Month (1–9, A, B, C)
XXX = Last Three Digits of Assembly Lot Number

Functional Diagram

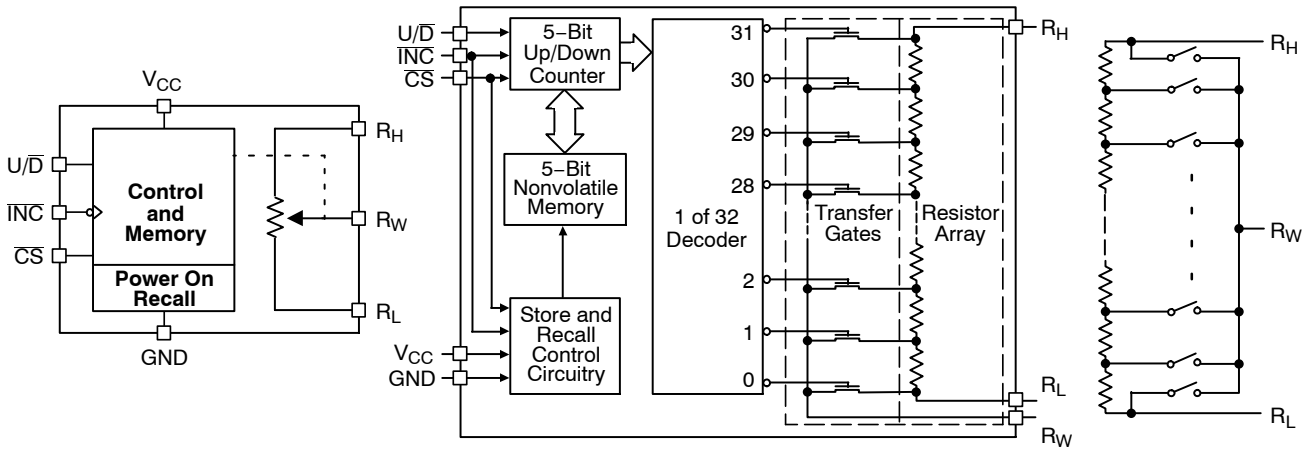


Figure 1. General

Figure 2. Detailed

Figure 3. Electronic Potentiometer Implementation

Pin Description

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high−to−low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_W: Wiper Potentiometer Terminal

R_W is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. Voltage applied to the R_W terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the CAT5113 and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper.

Device Operation

The CAT5113 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_W equivalent to the mechanical potentiometer's wiper. There are 100 available tap positions including the resistor end points, R_H and R_L. There are 99 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a seven−bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5113 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and seven-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5113 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5113 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

Table 1. OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V_{CC} to GND	−0.5 to +7	V
Inputs $\overline{CS}$ to GND	−0.5 to V_{CC} +0.5	V
$\overline{INC}$ to GND	−0.5 to V_{CC} +0.5	V
U/$\overline{D}$ to GND	−0.5 to V_{CC} +0.5	V
H to GND	−0.5 to V_{CC} +0.5	V
L to GND	−0.5 to V_{CC} +0.5	V
W to GND	−0.5 to V_{CC} +0.5	V
Operating Ambient Temperature Commercial (‘C’ or Blank suffix)	0 to 70	°C
Industrial (‘I’ suffix)	−40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	−65 to 150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP} (Note 1)	ESD Susceptibility	MIL−STD−883, Test Method 3015	2000			V
I_{LTH} (Notes 1, 2)	Latch-Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL−STD−883, Test Method 1008	100			Years
N_{END}	Endurance	MIL−STD−883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} + 1 V

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V to +6 V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.5	–	6.0	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6 V, f = 1 MHz, I_W = 0	–	–	100	μA
		V_{CC} = 6 V, f = 250 kHz, I_W = 0	–	–	50	μA
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 6 V	–	–	1000	μA
		V_{CC} = 3 V	–	–	500	μA
I_{SB1} (Note 3)	Supply Current (Standby)	$\overline{CS}$ = V_{CC} – 0.3 V U/$\overline{D}$, $\overline{INC}$ = V_{CC} – 0.3 V or GND	–	0.01	1	μA
LOGIC INPUTS						
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	–	–	10	μA
I_{IL}	Input Leakage Current	V_{IN} = 0 V	–	–	–10	μA
V_{IH2}	CMOS High Level Input Voltage	2.5 V ≤ V_{CC} ≤ 6 V	V_{CC} x 0.7	–	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		–0.3	–	V_{CC} x 0.2	V
POTENTIOMETER CHARACTERISTICS						
R_{POT}	Potentiometer Resistance	–01 Device		1		kΩ
		–10 Device		10		
		–50 Device		50		
		–00 Device		100		
	Pot. Resistance Tolerance				±20	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			1		%
INL	Integral Linearity Error	I_W ≤ 2 μA		0.5	1	LSB
DNL	Differential Linearity Error	I_W ≤ 2 μA		0.25	0.5	LSB
R_{WI}	Wiper Resistance	V_{CC} = 5 V, I_W = 1 mA			400	Ω
		V_{CC} = 2.5 V, I_W = 1 mA			1000	Ω
I_W	Wiper Current	(Note 4)	–4.4		4.4	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC				20	ppm/°C
V_N	Noise	100 kHz / 1 kHz		8/24		nV/√Hz
$C_H/C_L/C_W$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10 kΩ		1.7		MHz

3. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} + 1 V
4. This parameter is not 100% tested.

Table 5. AC TEST CONDITIONS

V_{CC} Range	2.5 V ≤ V_{CC} ≤ 6 V
Input Pulse Levels	0.2 V_{CC} to 0.7 V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V_{CC}

Table 6. AC OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +6.0 V, V_H = V_{CC}, V_L = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 5)	Max	Units
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100	–	–	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	–	–	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	–	–	ns
t_{IL}	$\overline{INC}$ LOW Period	250	–	–	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	–	–	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	–	–	μs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	–	–	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	–	–	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	–	1	5	μs
t_{CYC}	$\overline{INC}$ Cycle Time	1	–	–	μs
t_R, t_F (Note 6)	$\overline{INC}$ Input Rise and Fall Time	–	–	500	μs
t_{PU} (Note 6)	Power-up to Wiper Stable	–	–	1	ms
t_{WR}	Store Cycle	–	5	10	ms

5. Typical values are for T_A = 25°C and nominal supply voltage.
6. This parameter is periodically sampled and not 100% tested.
7. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

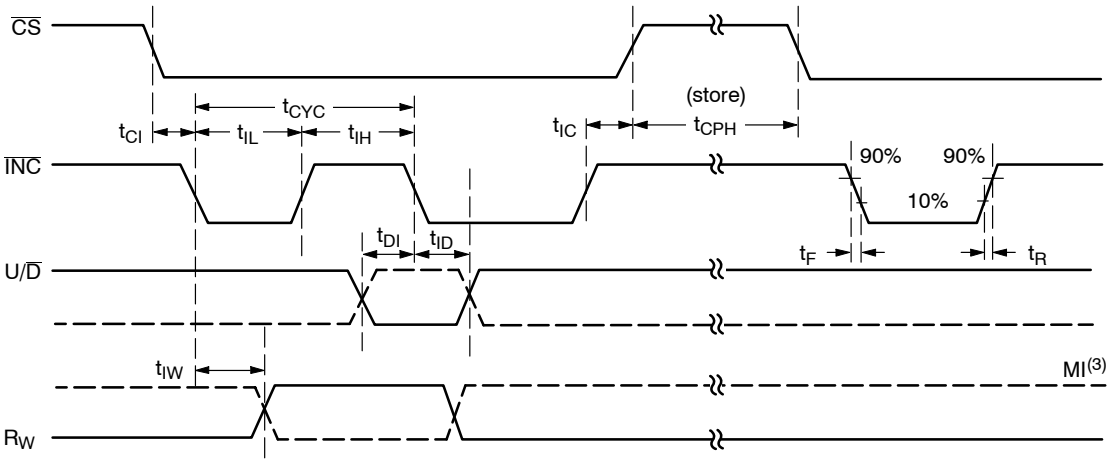


Figure 4. A.C. Timing

APPLICATIONS INFORMATION

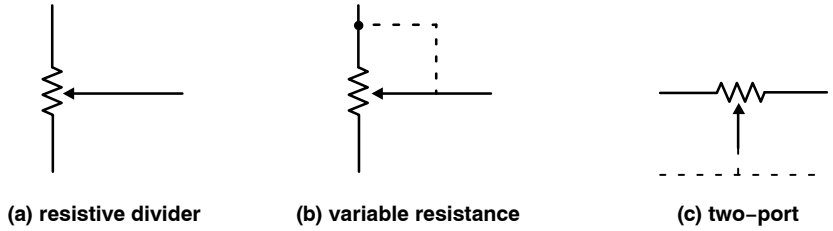


Figure 5. Potentiometer Configuration

Applications

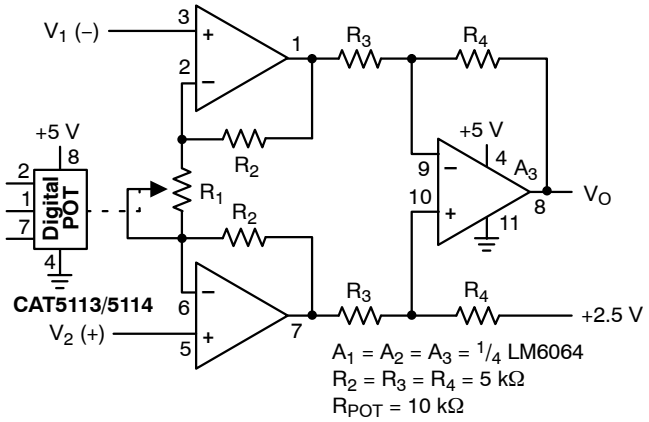


Figure 6. Programmable Instrumentation Amplifier

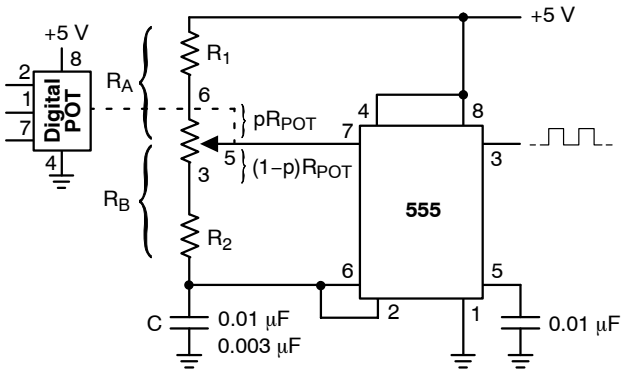


Figure 7. Programmable Sq. Wave Oscillator (555)

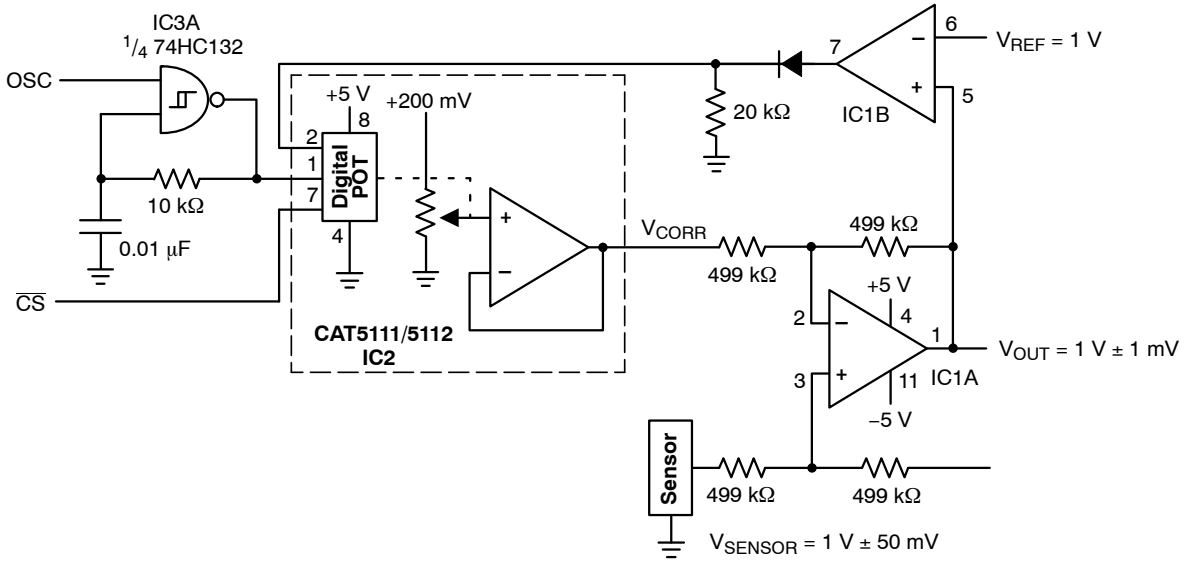


Figure 8. Sensor Auto Referencing Circuit

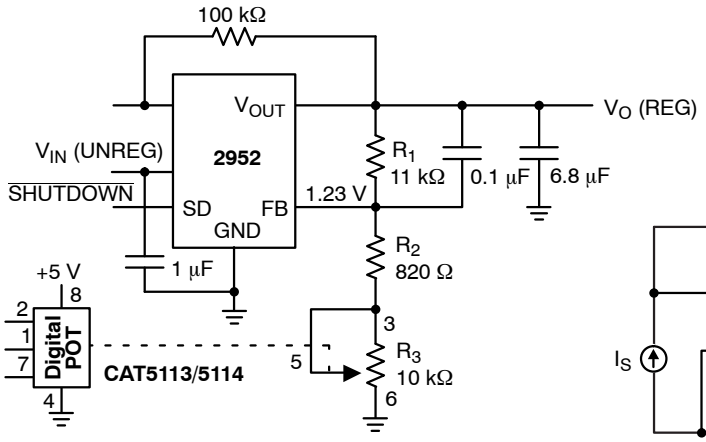


Figure 9. Programmable Voltage Regulator

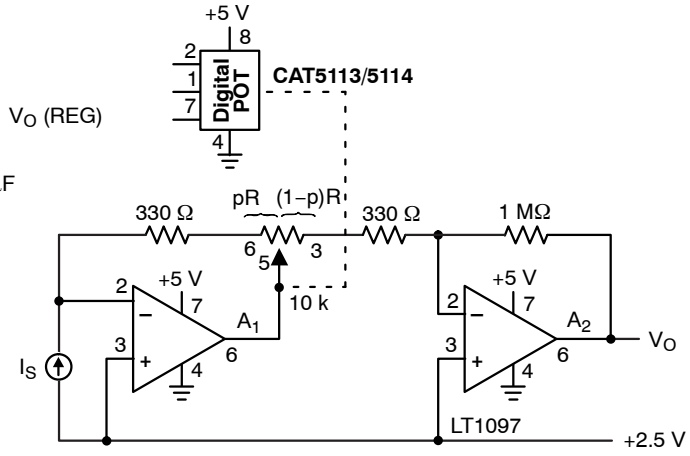


Figure 10. Programmable I to V Converter

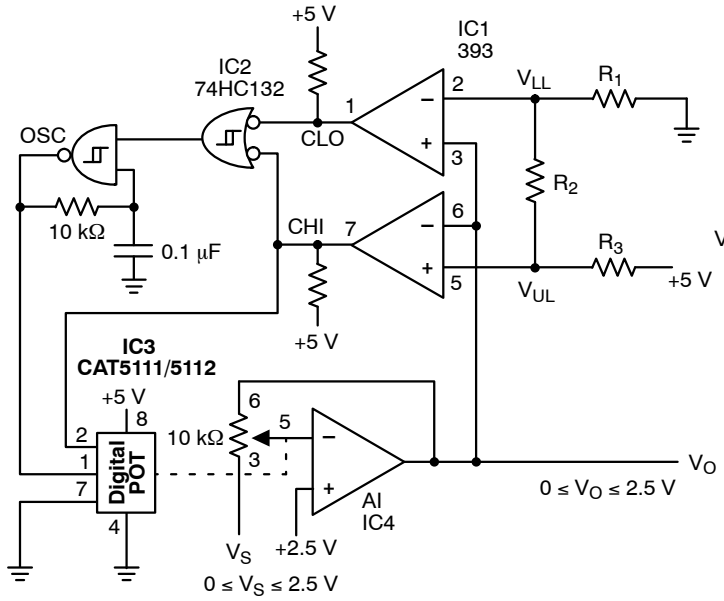


Figure 11. Automatic Gain Control

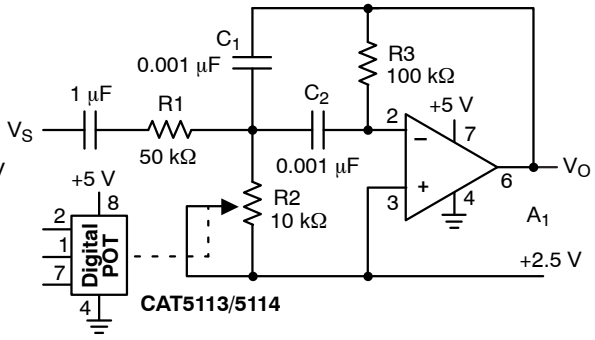


Figure 12. Programmable Bandpass Filter

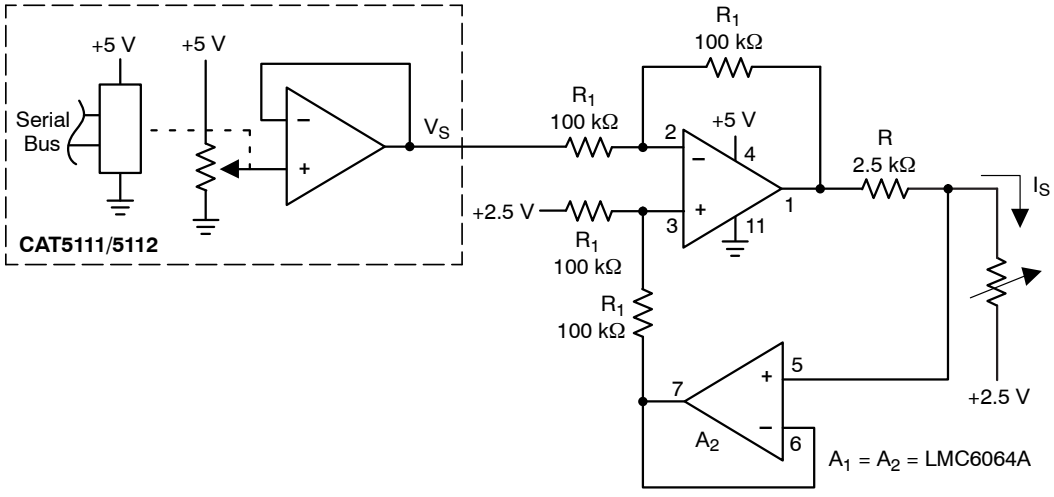


Figure 13. Programmable Current Source/Sink

Table 7. ORDERING INFORMATION

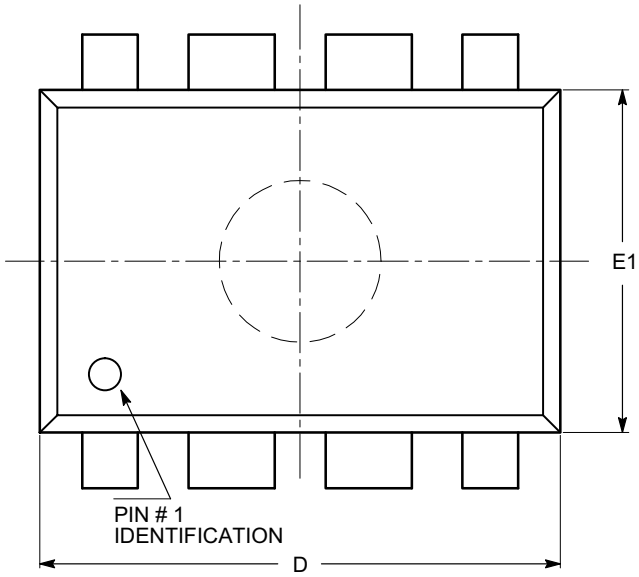
Orderable Part Number	Resistance (kΩ)	Lead Finish	Package−Pins	Shipping†
CAT5113LI−01−G	1	NiPdAu	PDIP−8 (Pb-Free)	50 Units / Rail
CAT5113LI−10−G	10			
CAT5113LI−50−G	50			
CAT5113LI−00−G	100			
CAT5113VI−01−GT3	1	NiPdAu	SOIC−8 (Pb-Free)	3000 / Tape & Reel
CAT5113VI−10−GT3	10			
CAT5113VI−50−GT3	50			
CAT5113VI−00−GT3	100			
CAT5113YI−01−GT3	1	NiPdAu	TSSOP−8 (Pb-Free)	3000 / Tape & Reel
CAT5113YI−10−GT3	10			
CAT5113YI−50−GT3	50			
CAT5113YI−00−GT3	100			
CAT5113ZI−01−T3	1	Matte-Tin	MSOP−8 (Pb-Free)	3000 / Tape & Reel
CAT5113ZI−10−T3	10			
CAT5113ZI−50−T3	50			
CAT5113ZI−00−T3	100			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. All packages are RoHS-compliant (Pb-Free, Halogen-Free).
9. The standard lead finish is NiPdAu, except MSOP package is Matte-Tin.
10. Contact factory for Matte-Tin finish availability for PDIP, SOIC and TSSOP packages.

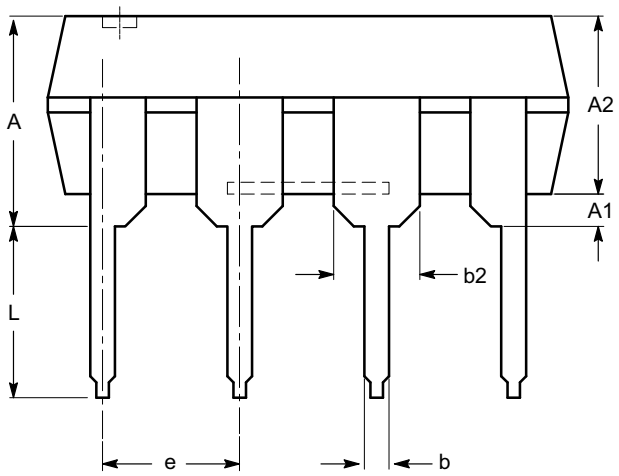
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA
ISSUE A

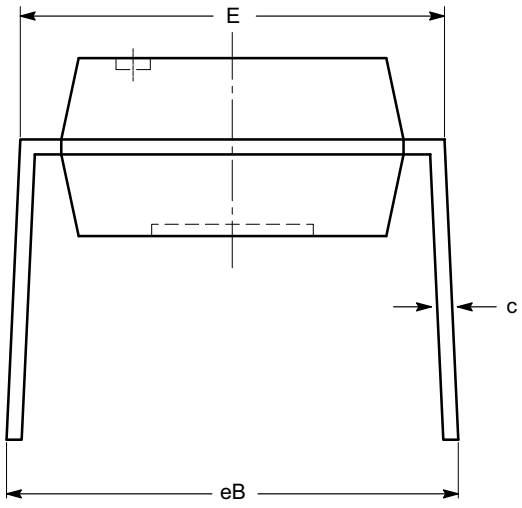


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

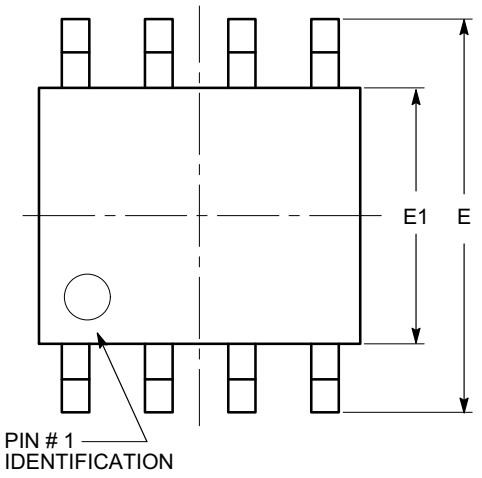


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

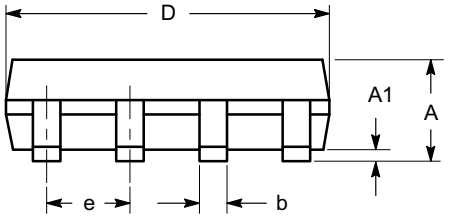
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD
ISSUE O

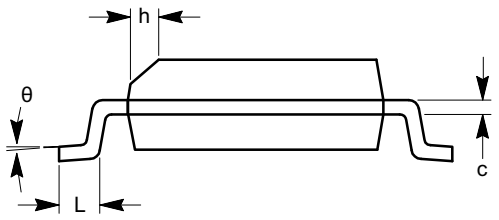


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

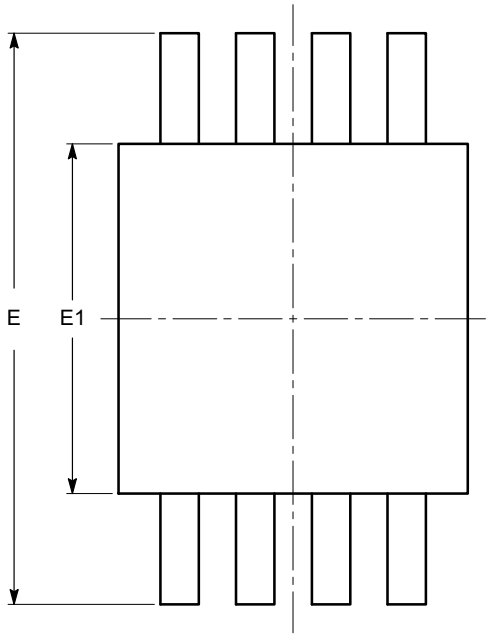


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

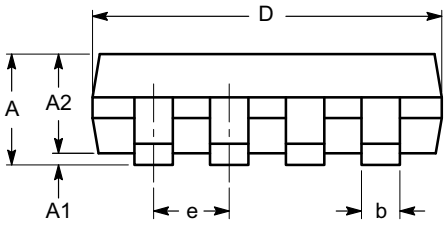
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD
ISSUE O

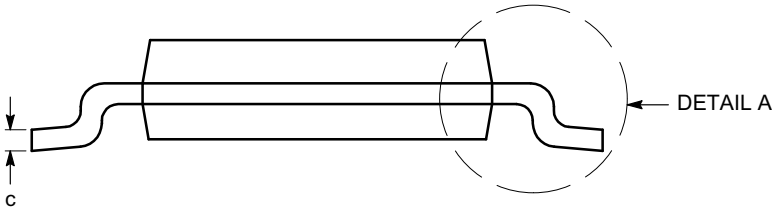


TOP VIEW

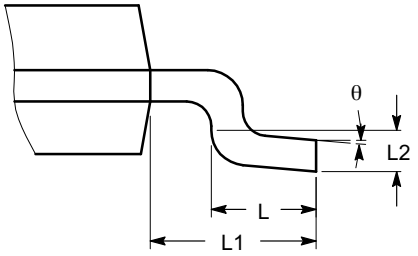
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0°		6°



SIDE VIEW



END VIEW

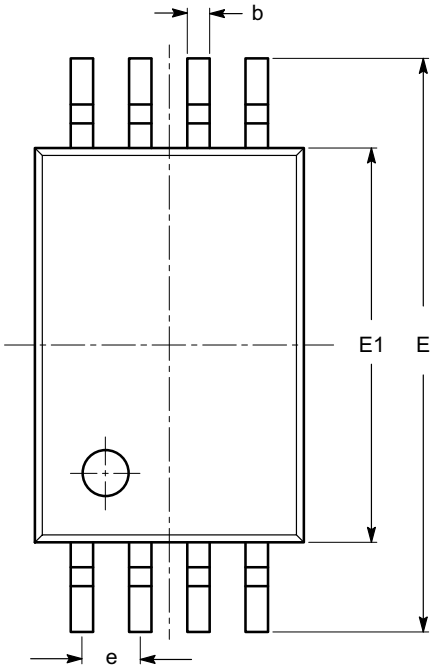


DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

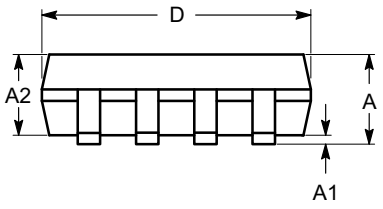
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL
ISSUE O

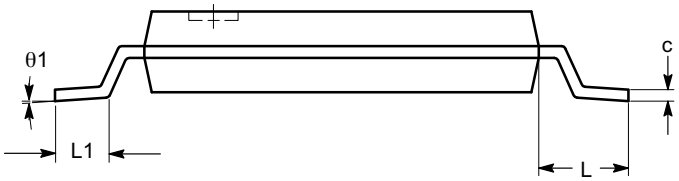


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers

1 Features

- High Performance
  - 150 MHz, –3 dB Bandwidth (V_{CC} = ±15 V)
  - 51 V/µs Slew Rate
  - –100 dB Third Harmonic Distortion at 250 kHz
- Low Noise
  - 1.3 nV/√Hz Input-Referred Noise
- Differential-Input/Differential-Output
  - Balanced Outputs Reject Common-Mode Noise
  - Reduced Second-Harmonic Distortion Due to Differential Output
- Wide Power-Supply Range
  - V_{CC} = 5 V Single Supply to ±15 V Dual Supply
- $I_{CC(SD)}$ = 860 µA in Shutdown Mode (THS4130)

2 Applications

- Single-Ended To Differential Conversion
- Differential ADC Driver
- Differential Antialiasing
- Differential Transmitter And Receiver
- Output Level Shifter

3 Description

The THS413x device is one in a family of fully-differential input/differential output devices fabricated using Texas Instruments' state-of-the-art BiComI complementary bipolar process.

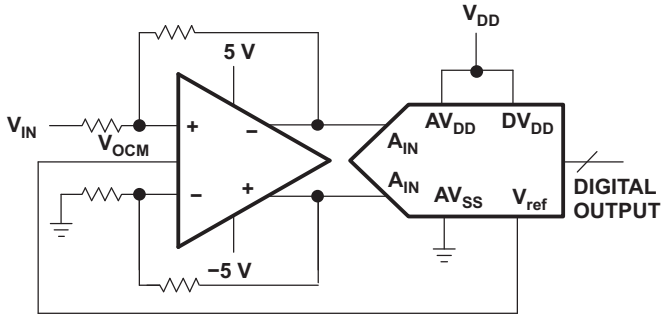
The THS413x is made of a true fully-differential signal path from input to output. This design leads to an excellent common-mode noise rejection and improved total harmonic distortion.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4130	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	HVSSOP (8)	3.00 mm x 3.00 mm
THS4131	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	HVSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical A/D Application Circuit



Total Harmonic Distortion vs Frequency

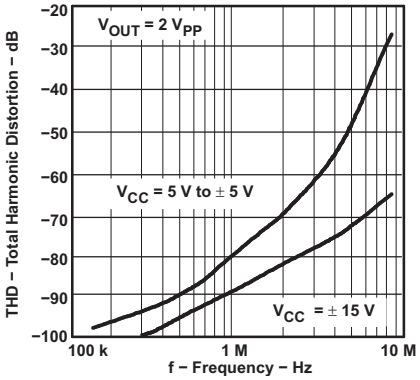


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (May 2011) to Revision I — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision G (January 2010) to Revision H — **Page**

- Changed footnote A in Figure 45. ... 25

Changes from Revision F (January 2006) to Revision G — **Page**

- Changed DGK package specifications in the *Dissipation Rating* table ... 7

5 Device Comparison Tables

Table 1. Available Device Packages

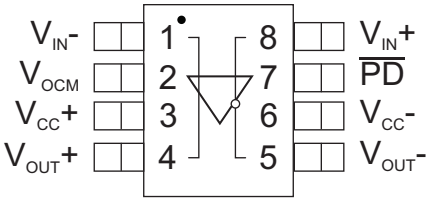
PACKAGED DEVICES						
T_A	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)	SYMBOL	MSOP (DGK)	SYMBOL	EVALUATION MODULES
0°C to +70°C	THS4130CD	THS4130CDGN	AOB	THS4130CDGK	ATP	THS4130EVM
	THS4131CD	THS4131CDGN	AOD	THS4131CDGK	ATQ	THS4131EVM
–40°C to +85°C	THS4130ID	THS4130IDGN	AOC	THS4130IDGK	ASO	—
	THS4131ID	THS4131IDGN	AOE	THS4131IDGK	ASP	—

Table 2. Device Description Table

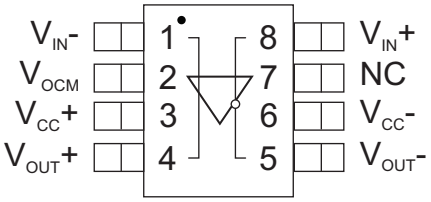
DEVICE	DESCRIPTION
THS412x	100 MHz, 43 V/µs, 3.7 nV/√Hz
THS414x	160 MHz, 450 V/µs, 6.5 nV/√Hz
THS415x	180 MHz, 850 V/µs, 9 nV/√Hz

6 Pin Configuration and Functions

D, DGN, or DGK Package
8-Pin SOIC, VSSOP, or HVSSOP
THS4130 Top View



D, DGN, or DGK Package
8-Pin SOIC, VSSOP, or HVSSOP
THS4131 Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	THS4130	THS4131		
NC	—	7	—	No connect
$\overline{PD}$	7	—	I	Active low powerdown pin
V_{CC+}	3	3	I/O	Positive supply voltage pin
$V_{CC–}$	6	6	I/O	Negative supply voltage pin
$V_{IN–}$	1	1	I	Negative input pin
V_{OCM}	2	2	I	Common mode input pin
V_{OUT+}	4	4	O	Positive output pin
$V_{OUT–}$	5	5	O	Negative output pin
V_{IN+}	8	8	I	Positive input pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage		$-V_{CC}$	$+V_{CC}$	V
V_{CC-} to V_{CC+}	Supply voltage		–33	33	V
I_O(2)	Output current			150	mA
V_{ID}	Differential input voltage		–6	6	V
	Continuous total power dissipation		See *Dissipation Ratings*		
T_J(3)	Maximum junction temperature			150	°C
T_J(4)	Maximum junction temperature, continuous operation, long-term reliability			125	°C
T_A	Operating free-air temperature	C-suffix	0	70	°C
		I-suffix	–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS413x may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD thermally-enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

7.2 ESD Ratings

			VALUE	UNIT
THS4130: D, DGN, OR DGK PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(1)	±1500	
THS4131: D, DGN, OR DGK PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{cc+} to V_{cc-}	Dual supply	±2.5		±15	V
	Single supply	5		30	
T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

7.4 Thermal Information

THERMAL METRIC[1]		THS413x			UNIT
		D (SOIC)	DGN (VSSOP)	DGK (HVSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.5	55.8	182.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	61.6	72.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	34.5	103.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	13.8	11.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	34.4	101.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics[1]

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 1, R_f = 390 Ω		125		MHz
		V_{CC} = ±5	Gain = 1, R_f = 390 Ω		135		
		V_{CC} = ±15	Gain = 1, R_f = 390 Ω		150		
	Small-signal bandwidth (–3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 2, R_f = 750 Ω		80		
		V_{CC} = ±5	Gain = 2, R_f = 750 Ω		85		
		V_{CC} = ±15	Gain = 2, R_f = 750 Ω		90		
SR	Slew rate[2]	Gain = 1			52		V/µs
t_s	Settling time to 0.1%	Step voltage = 2 V, gain = 1			78		ns
	Settling time to 0.01%	Step voltage = 2 V, gain = 1			213		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, V_O= 2 V_{PP}	V_{CC} = 5	f = 250 kHz		–95		dBc
			f = 1 MHz		–81		
		V_{CC} = ±5	f = 250 kHz		–96		
			f = 1 MHz		–80		
		V_{CC} = ±15	f = 250 kHz		–97		
			f = 1 MHz		–80		
	V_O = 4 V_{PP}	V_{CC} = ±5	f = 250 kHz		–91		
			f = 1 MHz		–75		
		V_{CC} = ±15	f = 250 kHz		–91		
			f = 1 MHz		–75		
SFDR	Spurious-free dynamic range, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, f = 250 kHz	V_O= 2 V_{PP}	V_{CC} = ±2.5		97		dB
			V_{CC} = ±5		98		
			V_{CC} = ±15		99		
		V_O = 4 V_{PP}	V_{CC} = ±5		93		
			V_{CC} = ±15		95		

(1) The full range temperature is 0°C to +70°C for the C-suffix, and –40°C to +85°C for the I-suffix.
(2) Slew rate is measured from an output level range of 25% to 75%.

Electrical Characteristics(1) (continued)

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Third intermodulation distortion		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			–53		dBc
Third-order intercept		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			41.5		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			1.3		nV/√Hz
I_n	Input current noise	f = 10 kHz			1		pA/√Hz
DC PERFORMANCE							
	Open-loop gain	T_A = +25°C		71	78		dB
		T_A = full range		69			
$V_{(OS)}$	Input offset voltage	T_A = +25°C			0.2	2	mV
		T_A = full range				3	
	Common-mode input offset voltage, referred to V_{OCM}	T_A = +25°C			0.2	3.5	
	Input offset voltage drift	T_A = full range			4.5		µV/°C
I_{IB}	Input bias current	T_A = full range			2	6	µA
I_{OS}	Input offset current	T_A = full range			100	500	nA
	Offset drift				2		nA/°C
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range		80	95		dB
V_{ICR}	Common-mode input voltage range			–3.7 7 to 4.3	–4 to 4.5		V
R_I	Input resistance	Measured into each input terminal			34		MΩ
C_I	Input capacitance, closed loop				4		pF
r_o	Output resistance	Open loop			41		Ω
OUTPUT CHARACTERISTICS							
	Output voltage swing	V_{CC} = 5 V	T_A = +25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range	1.3 to 3.7	±4		
		V_{CC} = ±5 V	T_A = +25°C	±3.7			
			T_A = full range	±3.6			
		V_{CC} = ±15 V	T_A = +25°C	±10.5	±12.4		
			T_A = full range	±10.2			

Electrical Characteristics(1) (continued)

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = +25°C	25	45		mA
			T_A = full range	20			
		V_{CC} = ±5 V, R_L = 7 Ω	T_A = +25°C	30	55		
			T_A = full range	28			
		V_{CC} = ±15 V, R_L = 7 Ω	T_A = +25°C	60	85		
			T_A = full range	65			
POWER SUPPLY							
V_{CC}	Supply voltage range	Single supply		4		33	V
		Split supply		±2		±16.5	
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = +25°C		12.3	15	mA
			T_A = full range			16	
		V_{CC} = ±15 V	T_A = +25°C		14		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)(3)	V = –5 V	T_A = +25°C		0.86	1.4	mA
			T_A = full range			1.5	
PSRR	Power-supply rejection ratio (dc)		T_A = +25°C	73	98		dB
			T_A = full range	70			

(3) For detailed information on the behavior of the power-down circuit, see the *Power-Down Mode* section.

7.6 Dissipation Ratings

PACKAGE	θ_{JA}(1) (°C/W)	θ_{JC} (°C/W)	POWER RATING(2)	
			T_A= +25°C	T_A = +85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	134	72	750 mW	300 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and long-term reliability.

7.7 Typical Characteristics

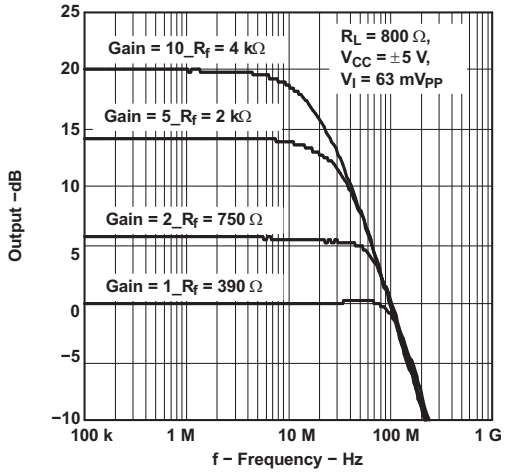


Figure 1. Small-Signal Frequency Response

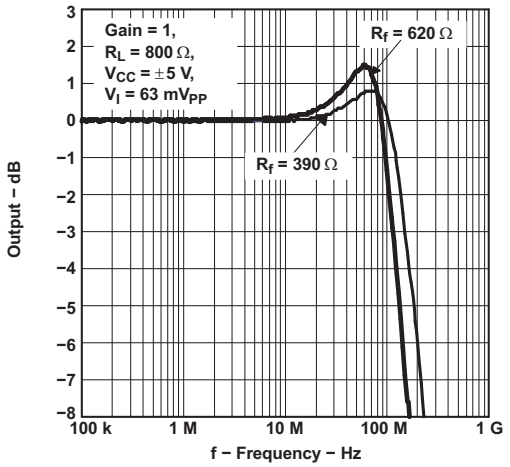


Figure 2. Small-Signal Frequency Response

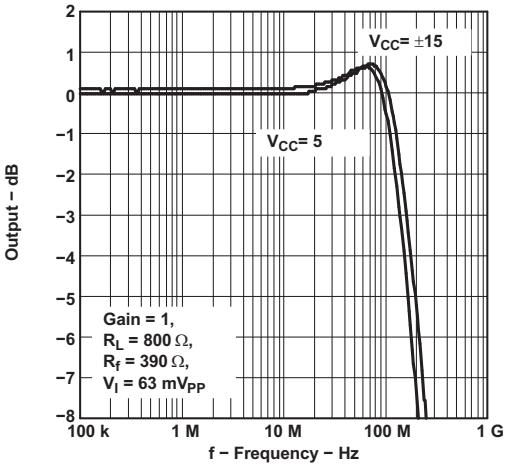


Figure 3. Small-Signal Frequency Response (Various Supplies)

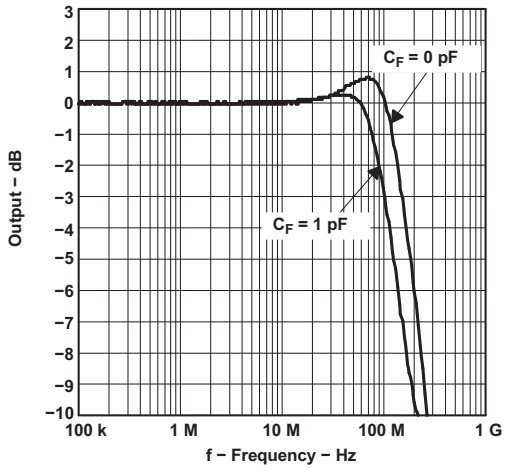


Figure 4. Small-Signal Frequency Response (Various C_F)

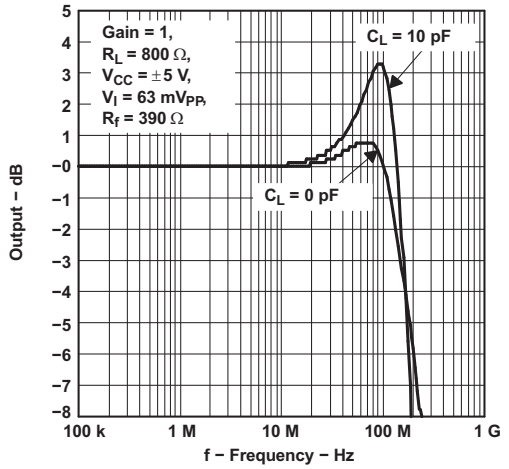


Figure 5. Small-Signal Frequency Response (Various C_L)

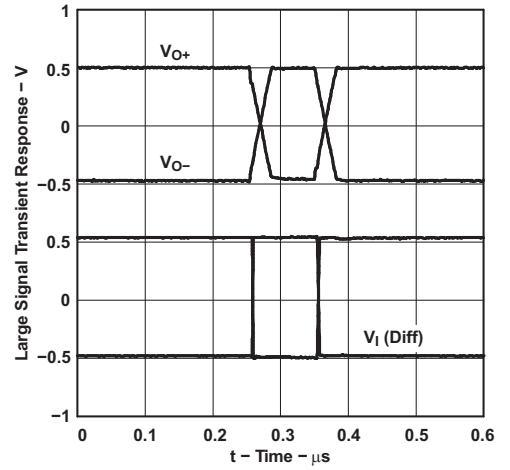


Figure 6. Large-Signal Transient Response (Differential In/Single Out)

Typical Characteristics (continued)

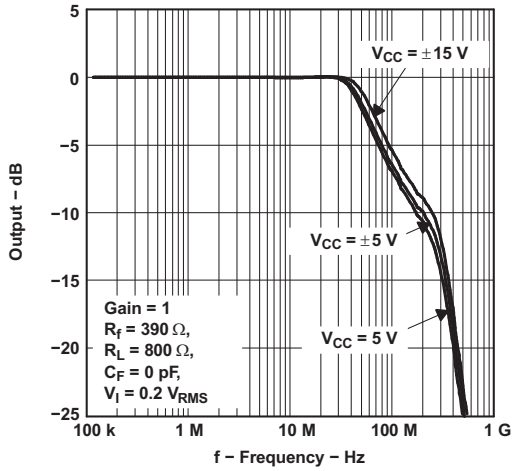


Figure 7. Large-Signal Frequency Response

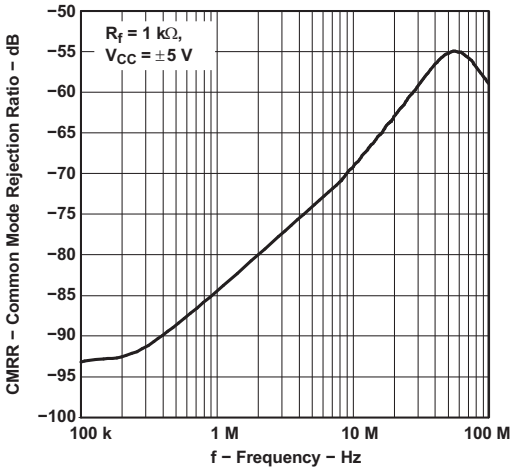


Figure 8. Common-Mode Rejection Ratio vs Frequency

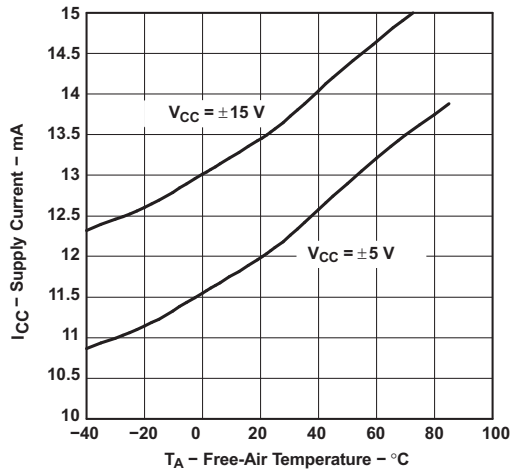


Figure 9. Supply Current vs Free-Air Temperature

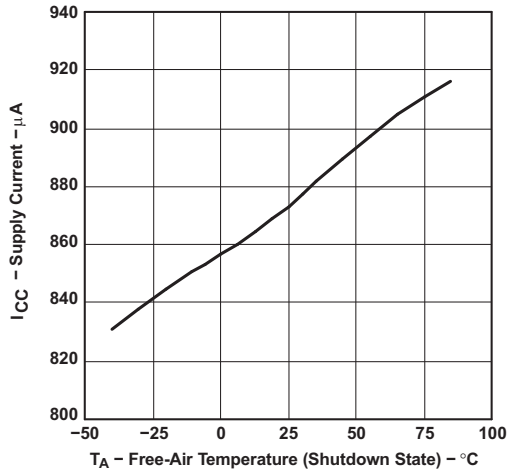


Figure 10. Supply Current vs Free-Air Temperature (Shutdown State)

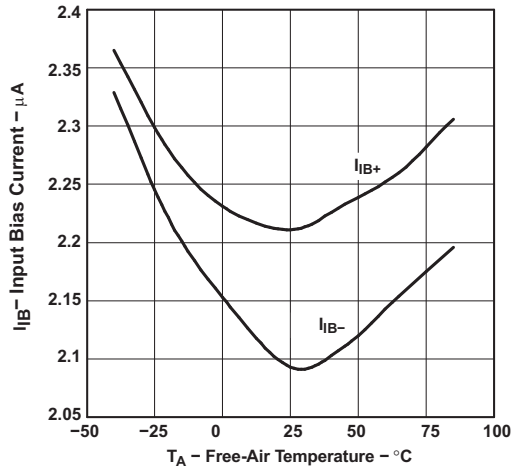


Figure 11. Input Bias Current vs Free-Air Temperature

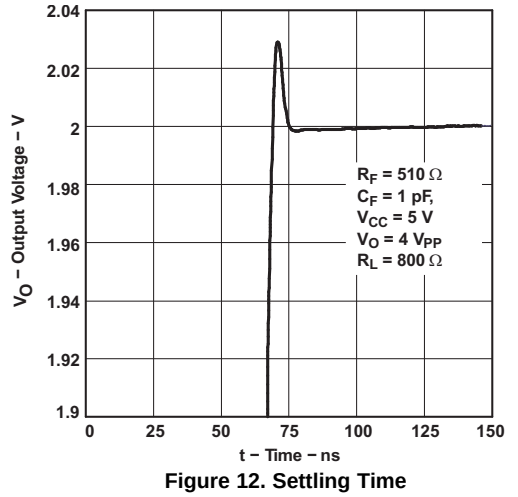


Figure 12. Settling Time

Typical Characteristics (continued)

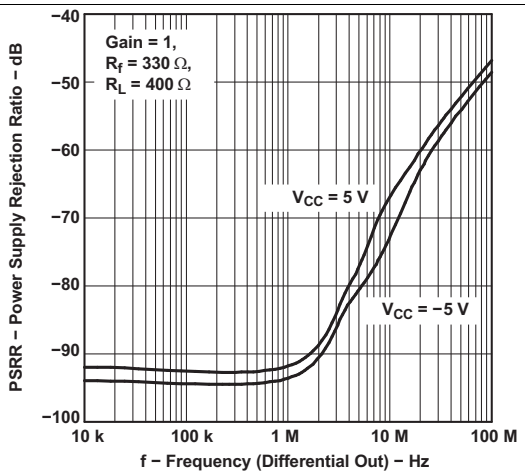


Figure 13. Power-Supply Rejection Ratio vs Frequency (Differential Out)

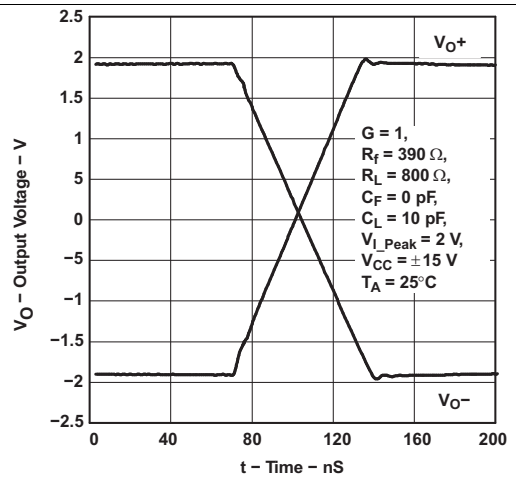


Figure 14. Large-Signal Transient Response

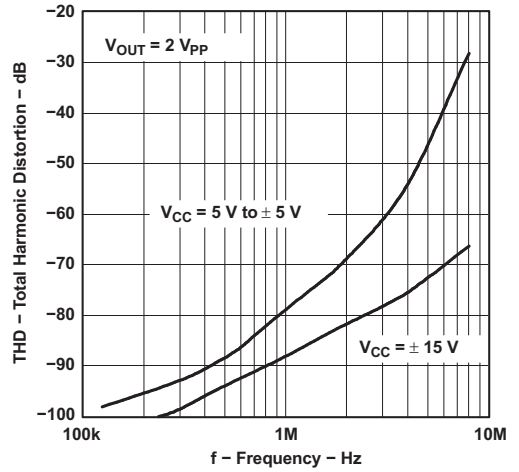


Figure 15. Total Harmonic Distortion vs Frequency

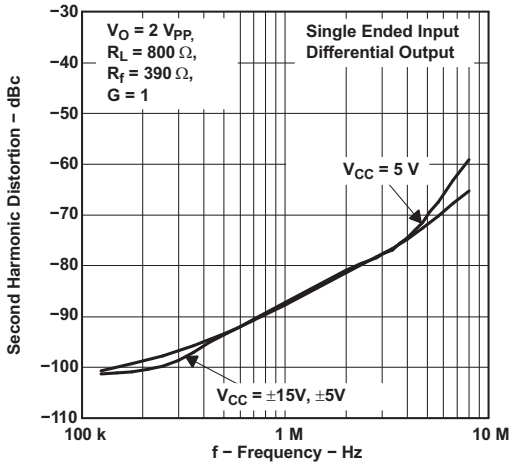


Figure 16. Second-Harmonic Distortion vs Frequency

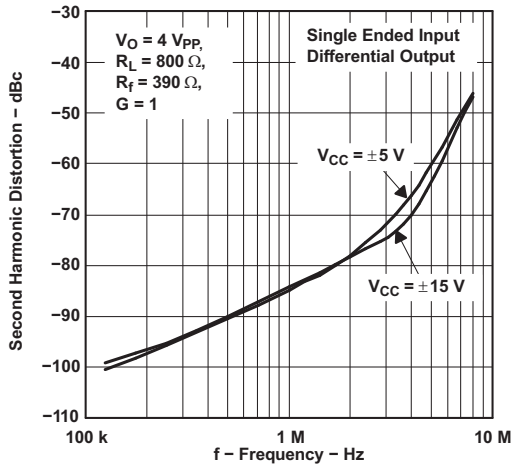


Figure 17. Second-Harmonic Distortion vs Frequency

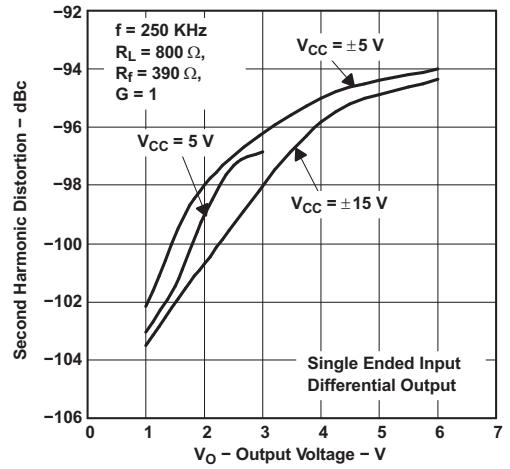


Figure 18. Second-Harmonic Distortion vs Output Voltage

Typical Characteristics (continued)

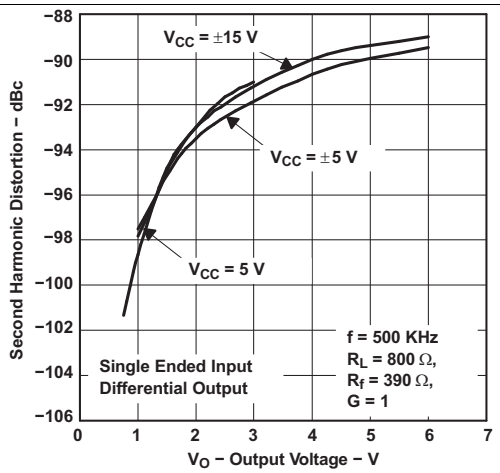


Figure 19. Second-Harmonic Distortion vs Output Voltage

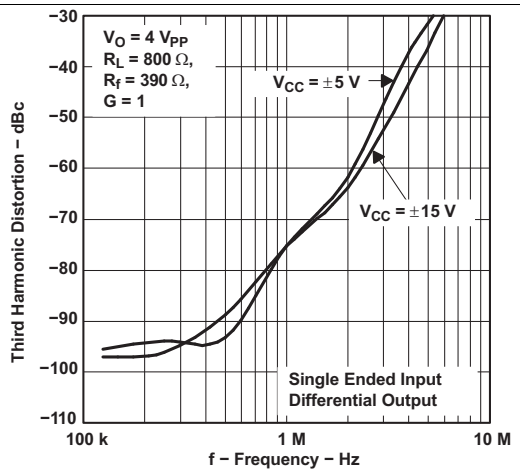


Figure 20. Third-Harmonic Distortion vs Frequency

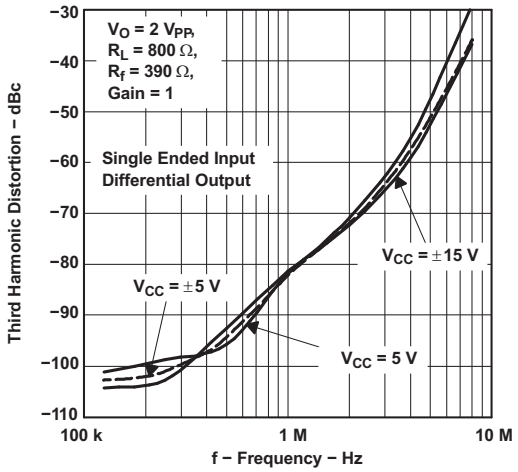


Figure 21. Third-Harmonic Distortion vs Frequency

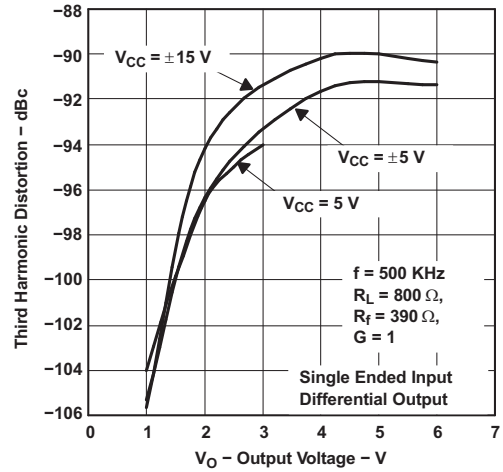


Figure 22. Third-Harmonic Distortion vs Output Voltage

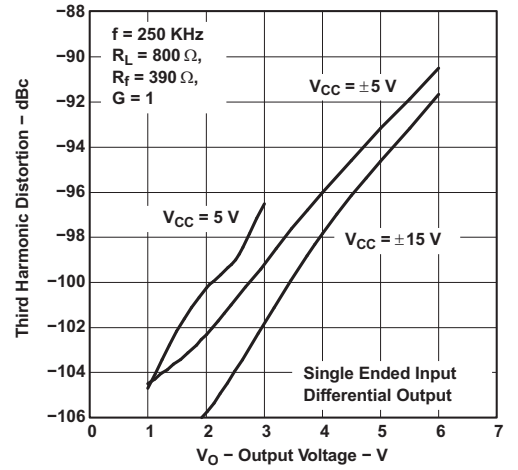


Figure 23. Third-Harmonic Distortion vs Output Voltage

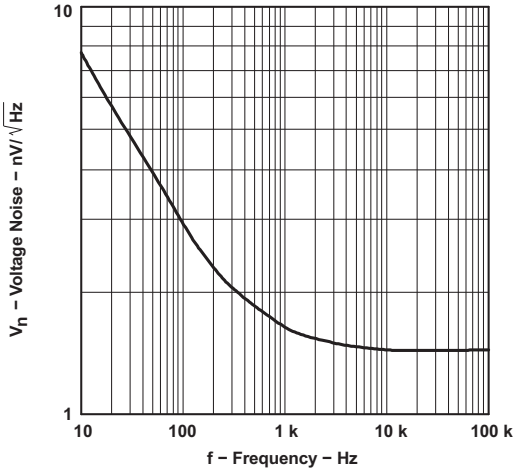


Figure 24. Voltage Noise vs Frequency

Typical Characteristics (continued)

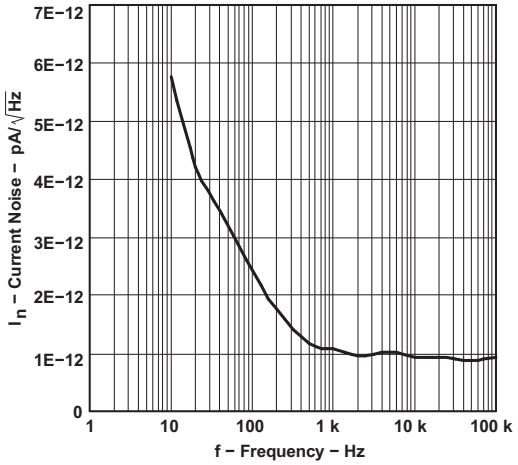


Figure 25. Current Noise vs Frequency

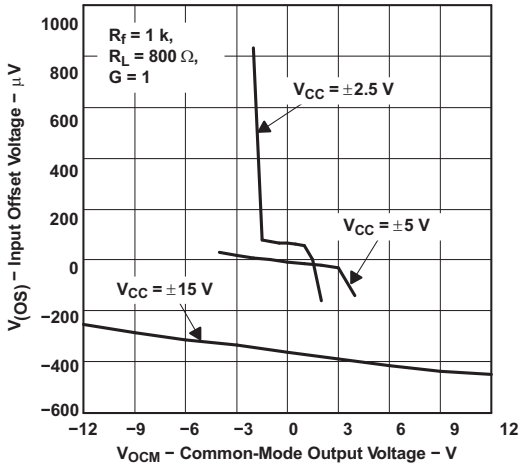


Figure 26. Input Offset Voltage vs Common-Mode Output Voltage

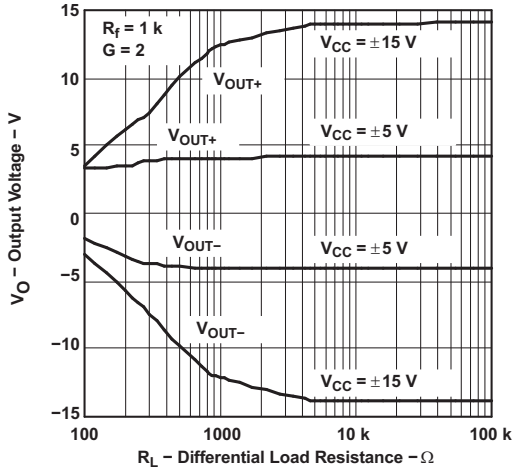


Figure 27. Output Voltage vs Differential Load Resistance

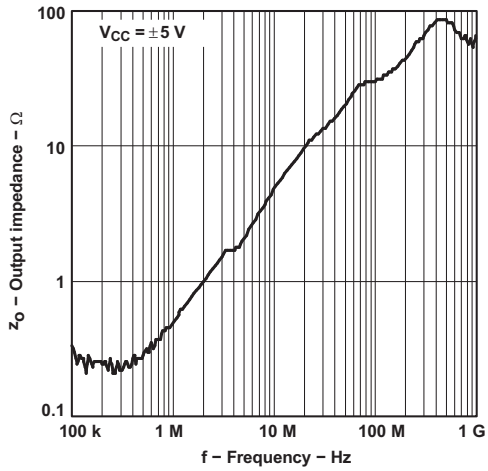


Figure 28. Output Impedance vs Frequency

8 Detailed Description

8.1 Overview

The THS413x is a fully-differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully-differential amplifiers are *differential in/differential out*.

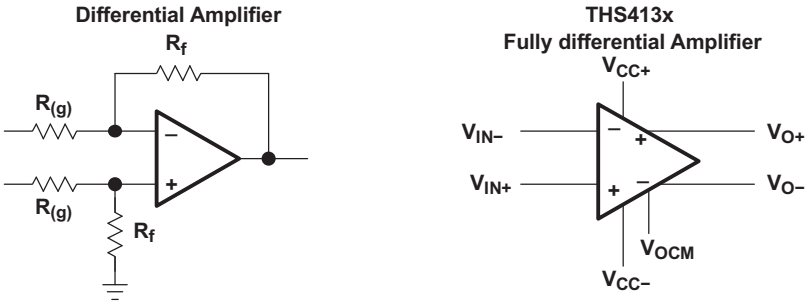


Figure 29. Differential Amplifier Versus a Fully-Differential Amplifier

To understand the THS413x fully-differential amplifiers, the definition for the pin outs of the amplifier are provided.

$$\text{Input voltage definition } V_{ID} = (V_{I+}) - (V_{I-})\ V_{IC} = \frac{(V_{I+}) + (V_{I-})}{2} \tag{1}$$

$$\text{Output voltage definition } V_{OD} = (V_{O+}) - (V_{O-})\ \ V_{OC} = \frac{(V_{O+}) + (V_{O-})}{2} \tag{2}$$

$$\text{Transfer function } \ V_{OD} = V_{ID} \times A_{(f)} \tag{3}$$

$$\text{Output common mode voltage } \ V_{OC} = V_{OCM} \tag{4}$$

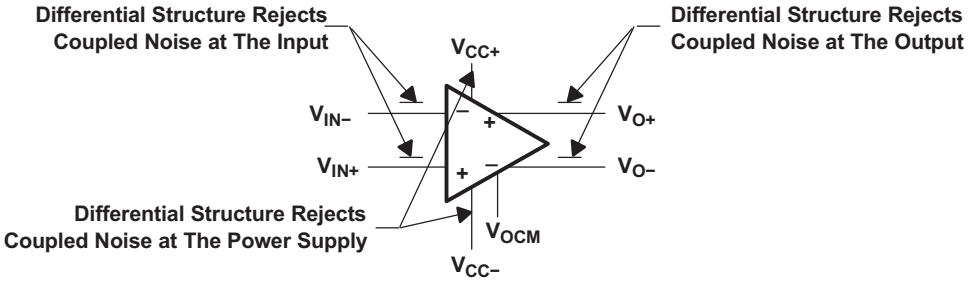


Figure 30. Definition of the Fully-Differential Amplifier

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I \tag{5}$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I \tag{6}$$

Fully-differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully-differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it is not as practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully-differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been

Overview (continued)

able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully-differential amplifier. The final result indicates twice as much dynamic range. Figure 31 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS413x fully-differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second-harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

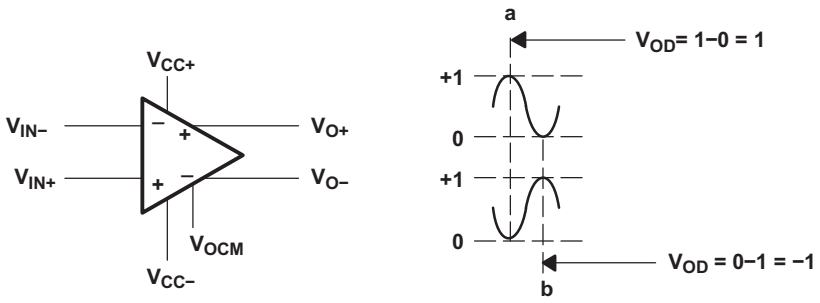


Figure 31. Fully-Differential Amplifier With Two 1-V_{PP} Signals

Similar to the standard inverting amplifier configuration, input impedance of a fully-differential amplifier is selected by the input resistor, $R_{(g)}$. If input impedance is a constraint in design, the designer may choose to implement the differential amplifier as an instrumentation amplifier. This configuration improves the input impedance of the fully-differential amplifier. Figure 32 depicts the general format of instrumentation amplifiers.

The general transfer function for this circuit is:

$$\frac{V_{OD}}{V_{IN1} - V_{IN2}} = \frac{R_f}{R_{(g)}}\left(1 + \frac{2R2}{R1}\right) \quad (7)$$

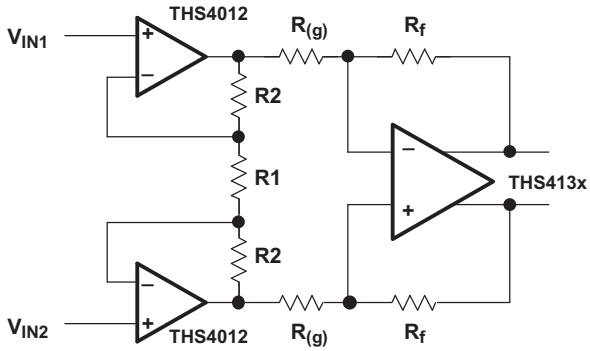
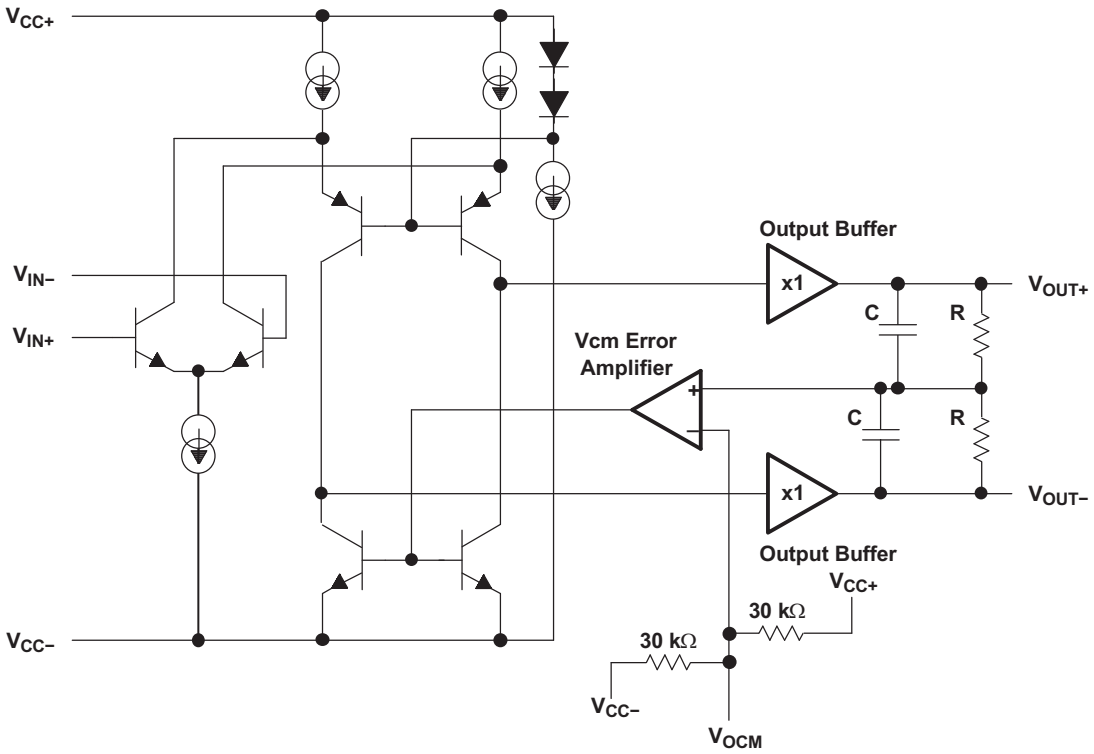


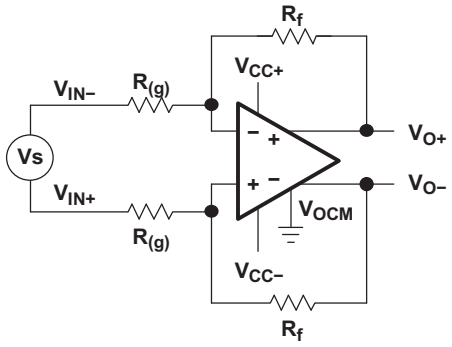
Figure 32. Instrumentation Amplifier

8.2 Functional Block Diagram



8.3 Feature Description

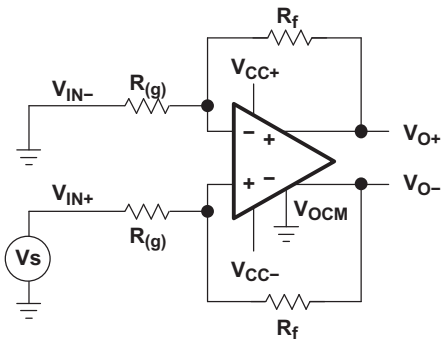
Figure 33 and Figure 34 depict the differences between the operation of the THS413x fully-differential amplifier in two different modes. Fully-differential amplifiers can work with differential input or can be implemented as single in/differential out.



Note: For proper operation, maintain symmetry by setting $R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)} \Rightarrow A = R_f/R_{(g)}$

Figure 33. Amplifying Differential Signals

Feature Description (continued)



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	390	390
2	374	750
5	402	2010
10	402	4020

Figure 34. Single In With Differential Out

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The power-down mode is used when power saving is required. The power-down terminal ($\overline{PD}$) found on the THS413x is an active low terminal. If it is left as a no-connect terminal, the device always stays on due to an internal 50 kΩ resistor to V_{CC}. The threshold voltage for this terminal is approximately 1.4 V above $V_{CC–}$. This means that if the $\overline{PD}$ terminal is 1.4 V above $V_{CC–}$, the device is active. If the $\overline{PD}$ terminal is less than 1.4 V above $V_{CC–}$, the device is off. For example, if $V_{CC–}$ = –5 V, then the device is on when PD reaches –3.6 V, (–5 V + 1.4 V = –3.6 V). By the same calculation, the device is off below –3.6 V. It is recommended to pull the terminal to $V_{CC–}$ in order to turn the device off. Figure 35 shows the simplified version of the power-down circuit. While in the power-down state, the amplifier goes into a high-impedance state. The amplifier output impedance is typically greater than 1 MΩ in the power-down state.

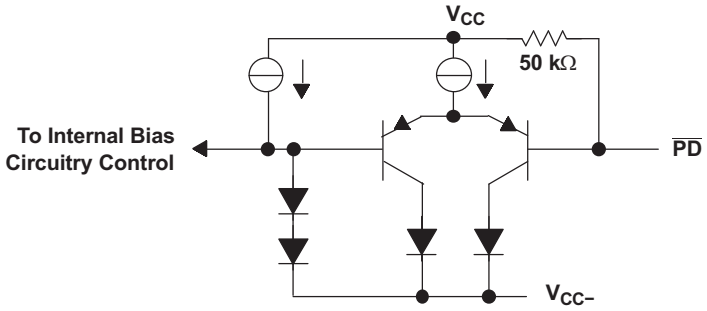


Figure 35. Simplified Power-Down Circuit

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be very low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed loop output impedance is shown in Figure 36.

Device Functional Modes (continued)

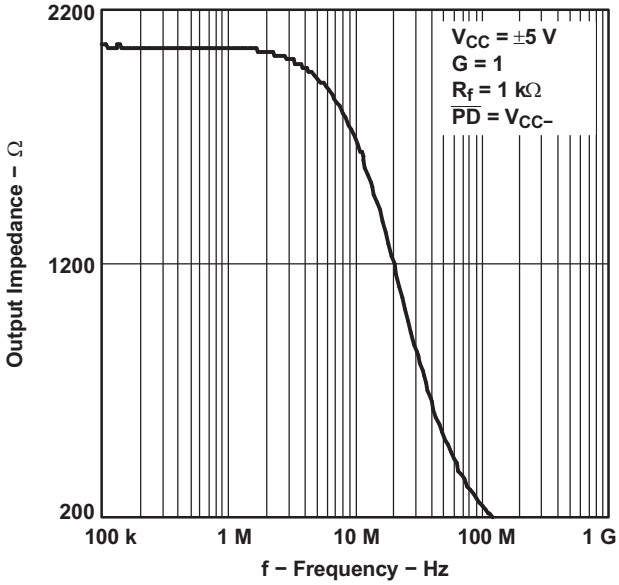


Figure 36. Output Impedance (in Power-Down) vs Frequency

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Resistor Matching

Resistor matching is important in fully-differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistor. CMRR, PSRR, and cancellation of the second-harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM}pin, it is set to the midrail voltage internally defined as:

$$\frac{(V_{CC+})+(V_{CC-})}{2} \tag{8}$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input in the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1 µF capacitor on the V_{OCM} pin as a bypass capacitor. The *Functional Block Diagram* shows the simplified diagram of the THS413x.

9.1.2 Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS413x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 37. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

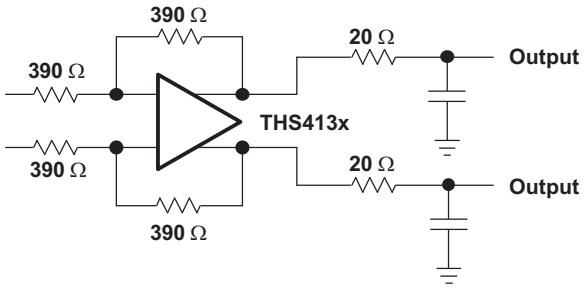


Figure 37. Driving a Capacitive Load

9.1.3 Data Converters

Data converters are one of the most popular applications for the fully-differential amplifiers. Figure 38 shows a typical configuration of a fully-differential amplifier attached to a differential analog-to-digital converter (ADC).

Application Information (continued)

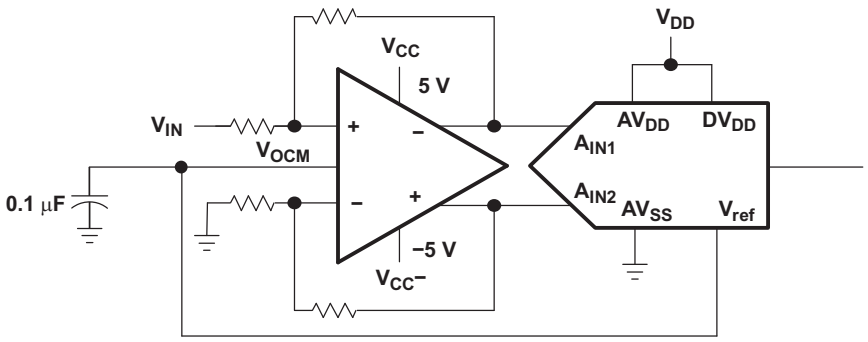


Figure 38. Fully-Differential Amplifier Attached to a Differential ADC

Fully-differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{CC}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range.

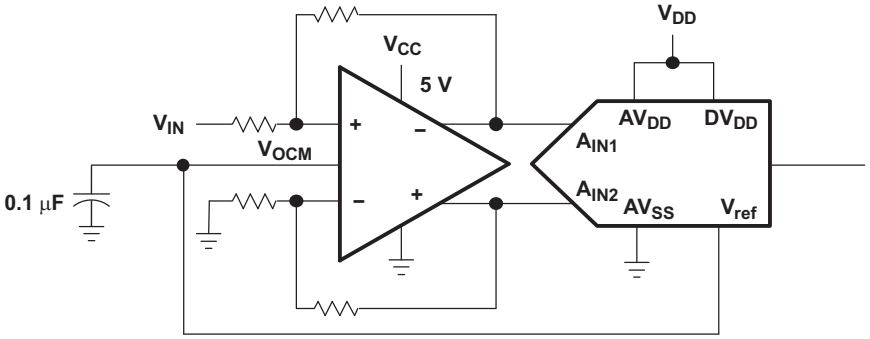


Figure 39. Fully-Differential Amplifier Using a Single Supply

9.1.4 Single-Supply Applications

Some single-supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the circuit configuration of Figure 40 is suggested to bring the common-mode input voltage within the specifications of the amplifier.

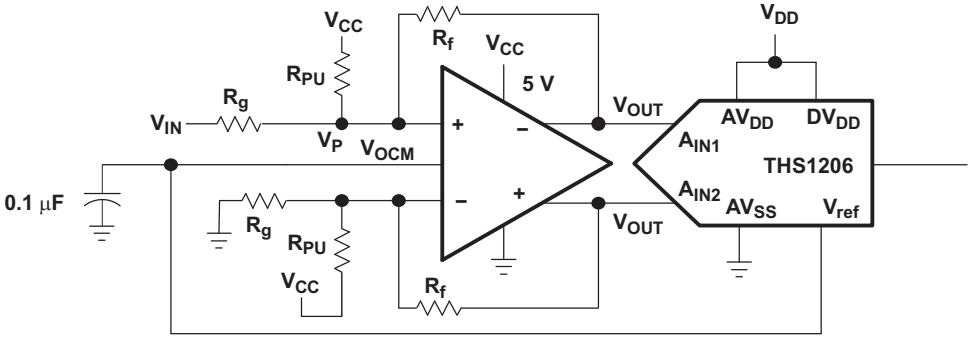


Figure 40. Circuit With Improved Common-Mode Input Voltage

Equation 9 is used to calculate R_{PU}:

Application Information (continued)

$$R_{PU} = \frac{V_P - V_{CC}}{(V_{IN} - V_P)\frac{1}{RG} + (V_{OUT} - V_P)\frac{1}{RF}} \quad (9)$$

9.2 Typical Application

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. Figure 41 presents a method by which the noise may be filtered in the THS413x.

Figure 41 shows a typical application design example for the THS413x device in active low-pass filter topology driving and ADC.

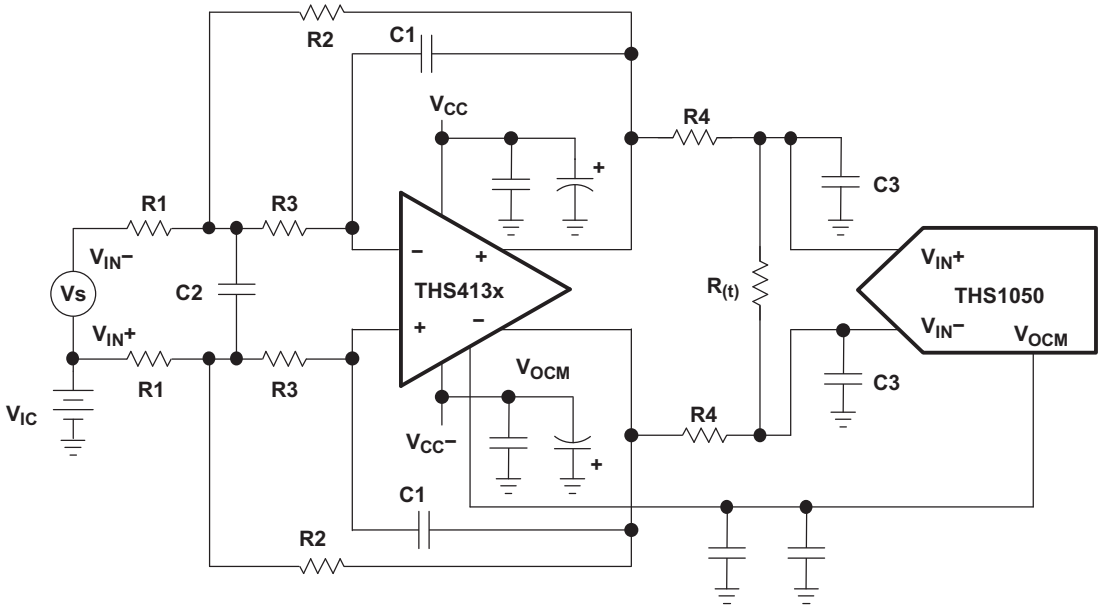


Figure 41. Antialias Filtering

9.2.1 Design Requirements

Table 3 shows example design parameters and values for the typical application design example in Figure 41.

Table 3. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC coupled with output common mode control capability
Filter requirement	500 kHz, Multiple feedback low pass filter

9.2.2 Detailed Design Procedure

9.2.2.1 Active Antialias Filtering

Figure 41 shows a multiple-feedback (MFB) lowpass filter. The transfer function for this filter circuit is:

$$H_d(f) = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}} \right) \text{ Where } K = \frac{R2}{R1} \quad (10)$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \text{ and } Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \quad (11)$$

K sets the pass band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \text{ and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \quad (12)$$

where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2 \times mn}} \text{ and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \quad (13)$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

9.2.3 Application Curve

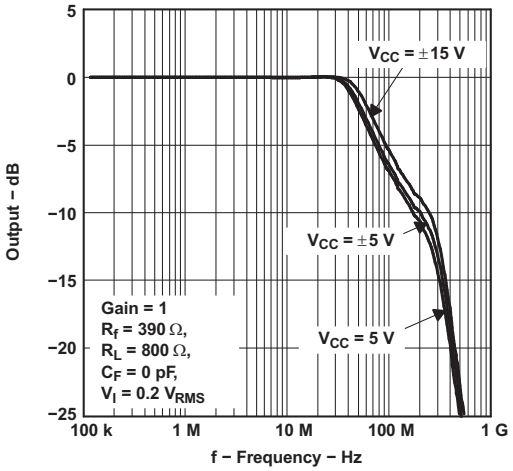


Figure 42. Large-Signal Frequency Response

10 Power Supply Recommendations

The THS413x device was designed to be operated on power supplies ranging from 2.5V to 15V. Single power supplies ranging from 5V to 30V can also be used. TI recommends using power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, it is important to provide isolation between digital signal noise and the analog input pins. The THS413x is connected to power supplies through pin 3 (V_{CC+}) and pin 6 (V_{CC-}). Each supply pin should be decoupled to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, the THS413x device should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

11 Layout

11.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS413x device, follow proper printed-circuit board (PCB) high-frequency design techniques. A general set of guidelines is given below. In addition, a THS413x device evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board are the best implementation.
- Short trace runs/compact part placements—Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

11.2 Layout Example

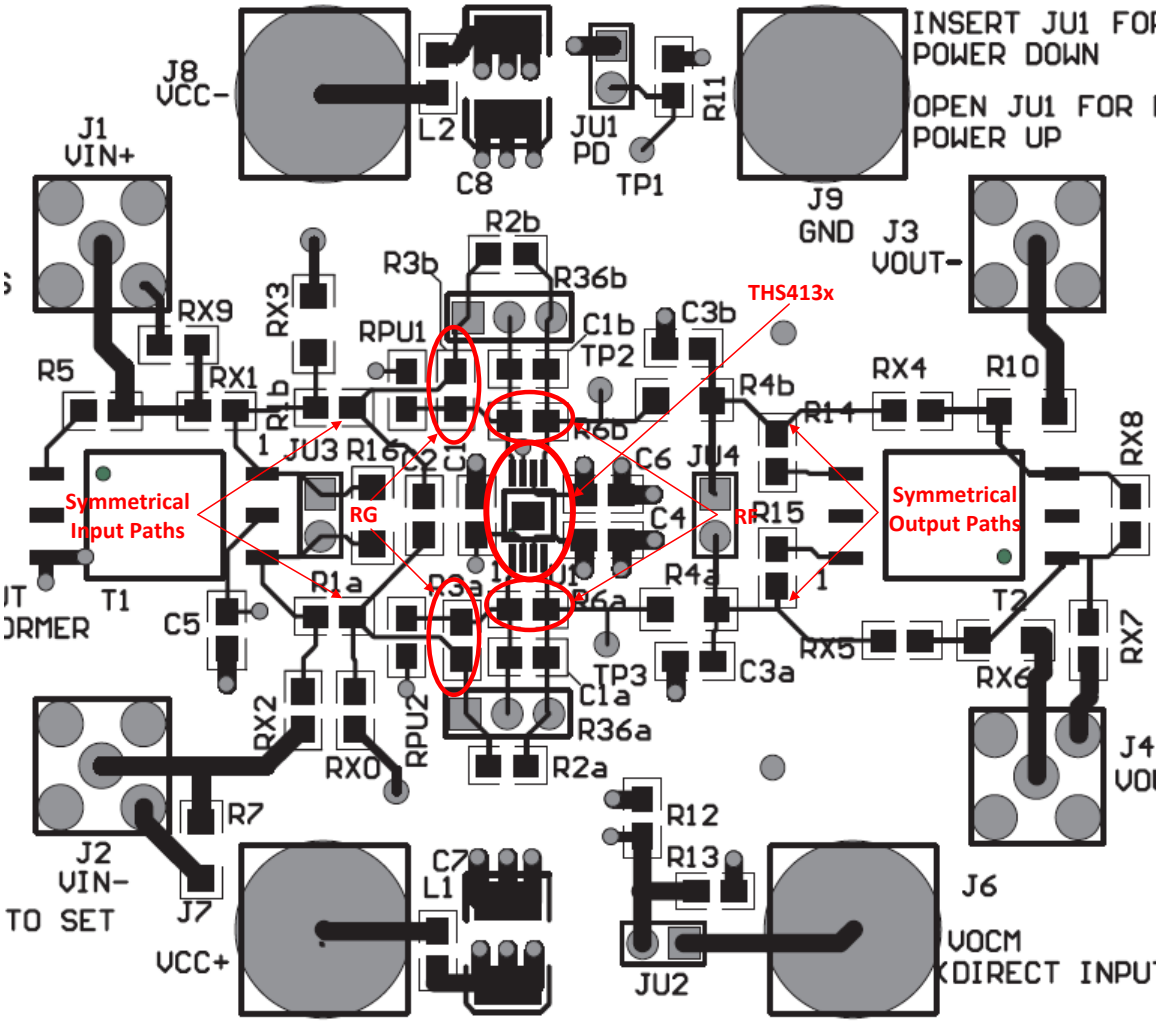


Figure 43. THS413x EVM Top Layer

Layout Example (continued)

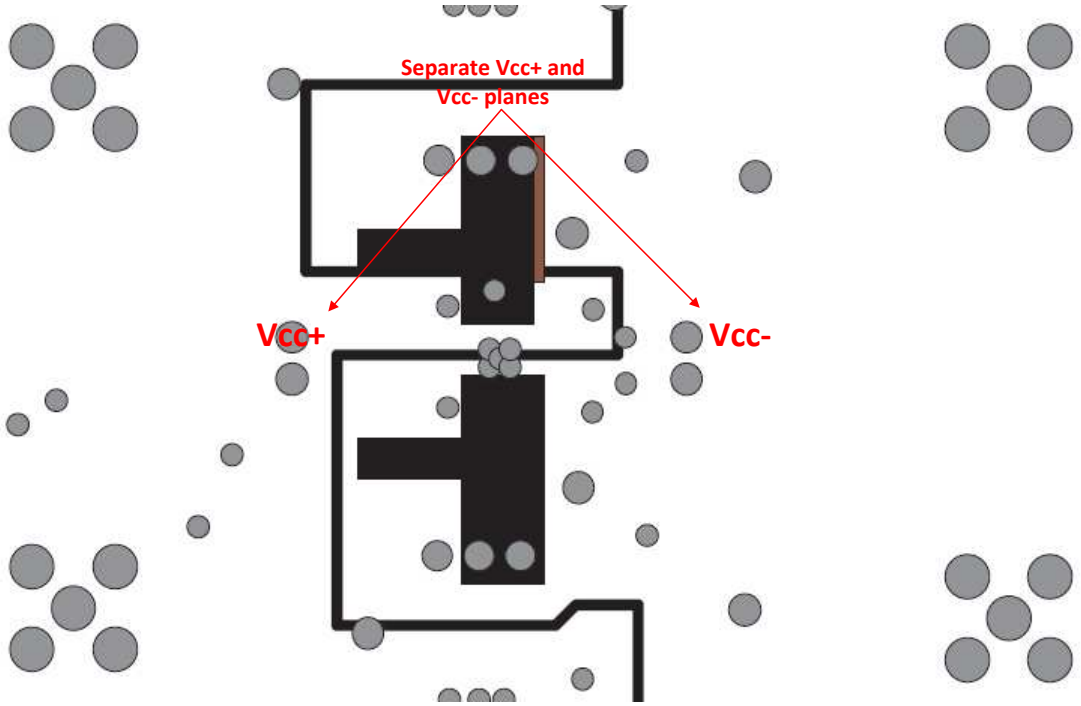


Figure 44. THS413x EVM Layer 3

11.3 General PowerPAD Design Considerations

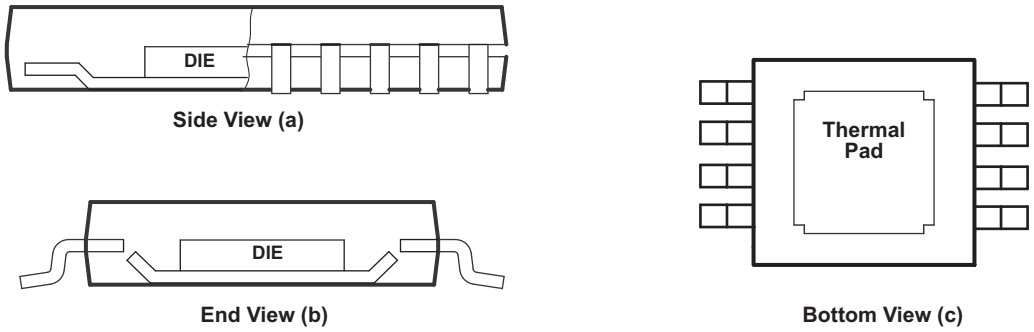
The THS413x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted (see Figure 45**a** and Figure 45**b**). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 45**c**). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of heatsinking.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, (*PowerPAD Thermally-Enhanced Package*, SLMA002). This document can be found on the TI website (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to SLMA002 when ordering.

General PowerPAD Design Considerations (continued)



A. The thermal pad (PowerPAD) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+}. Typically, the thermal pad is connected to the ground plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

Figure 45. Views of Thermally-Enhanced DGN Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

EVM User's Guide for High-Speed Fully-Differential Amplifier, SLOU101

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
THS4130	Click here	Click here	Click here	Click here	Click here
THS4131	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4130CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATP	Samples
THS4130CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4131CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4131CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

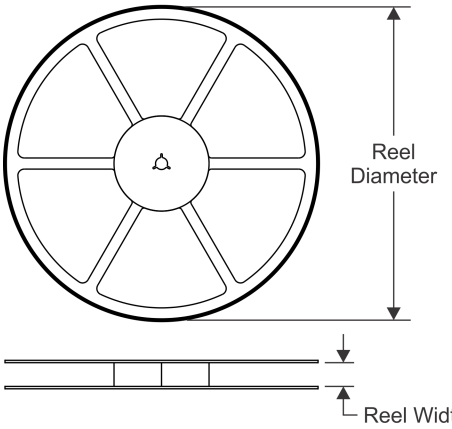
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

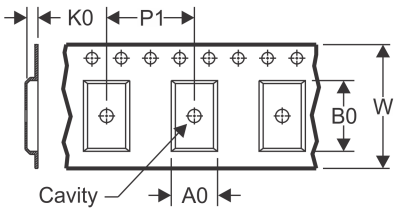
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

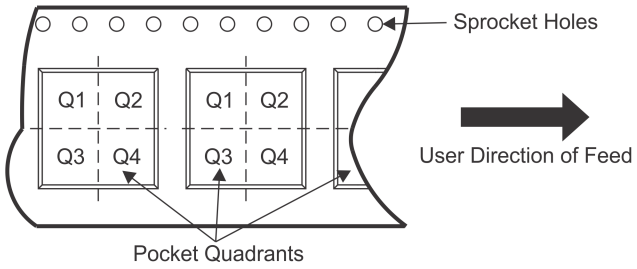


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

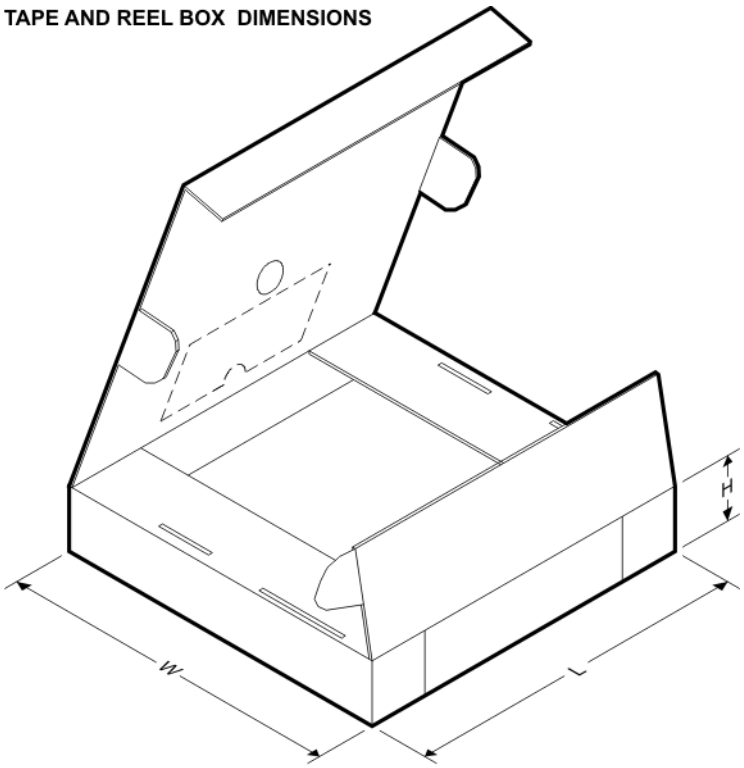
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4130CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

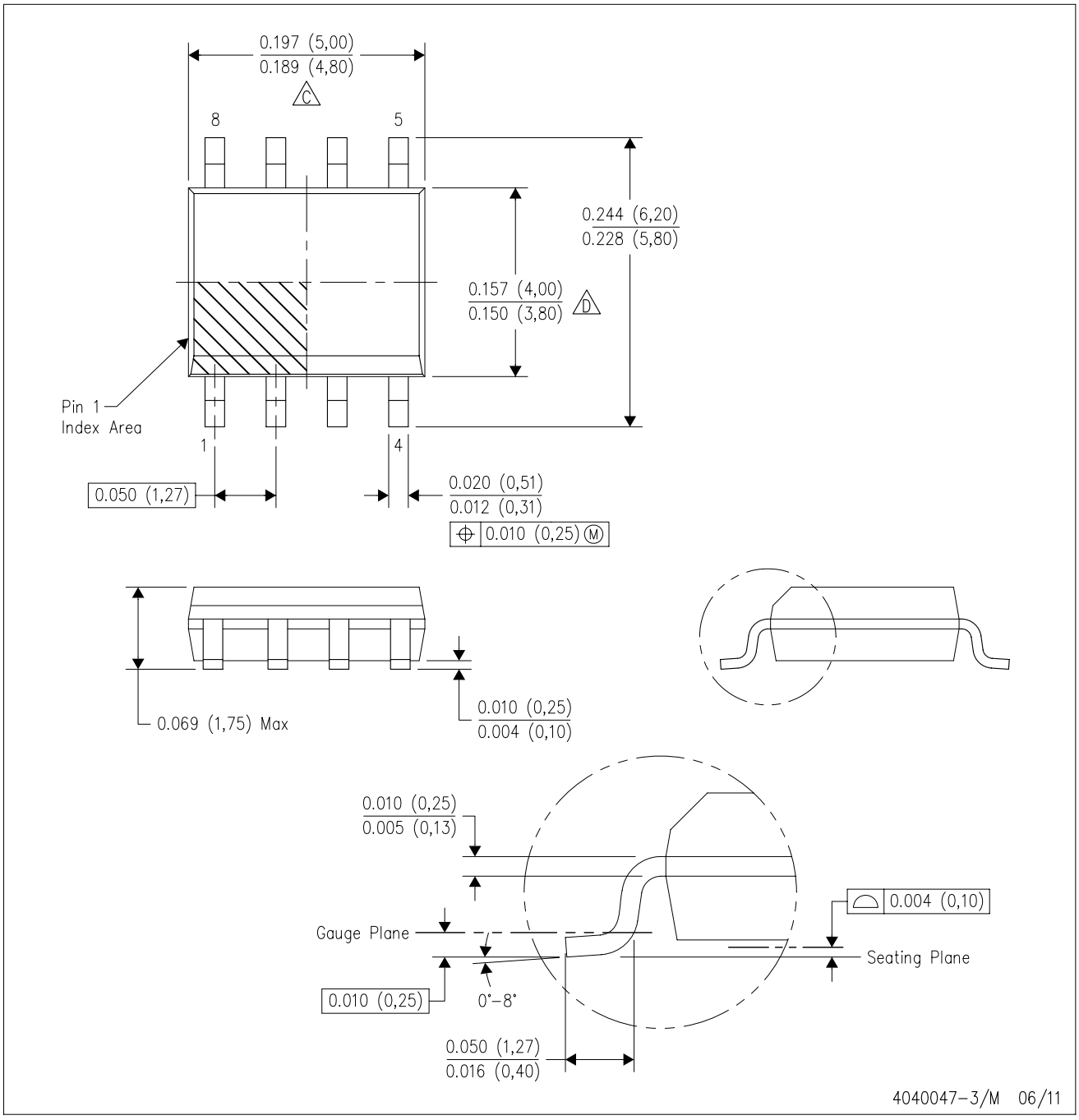
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

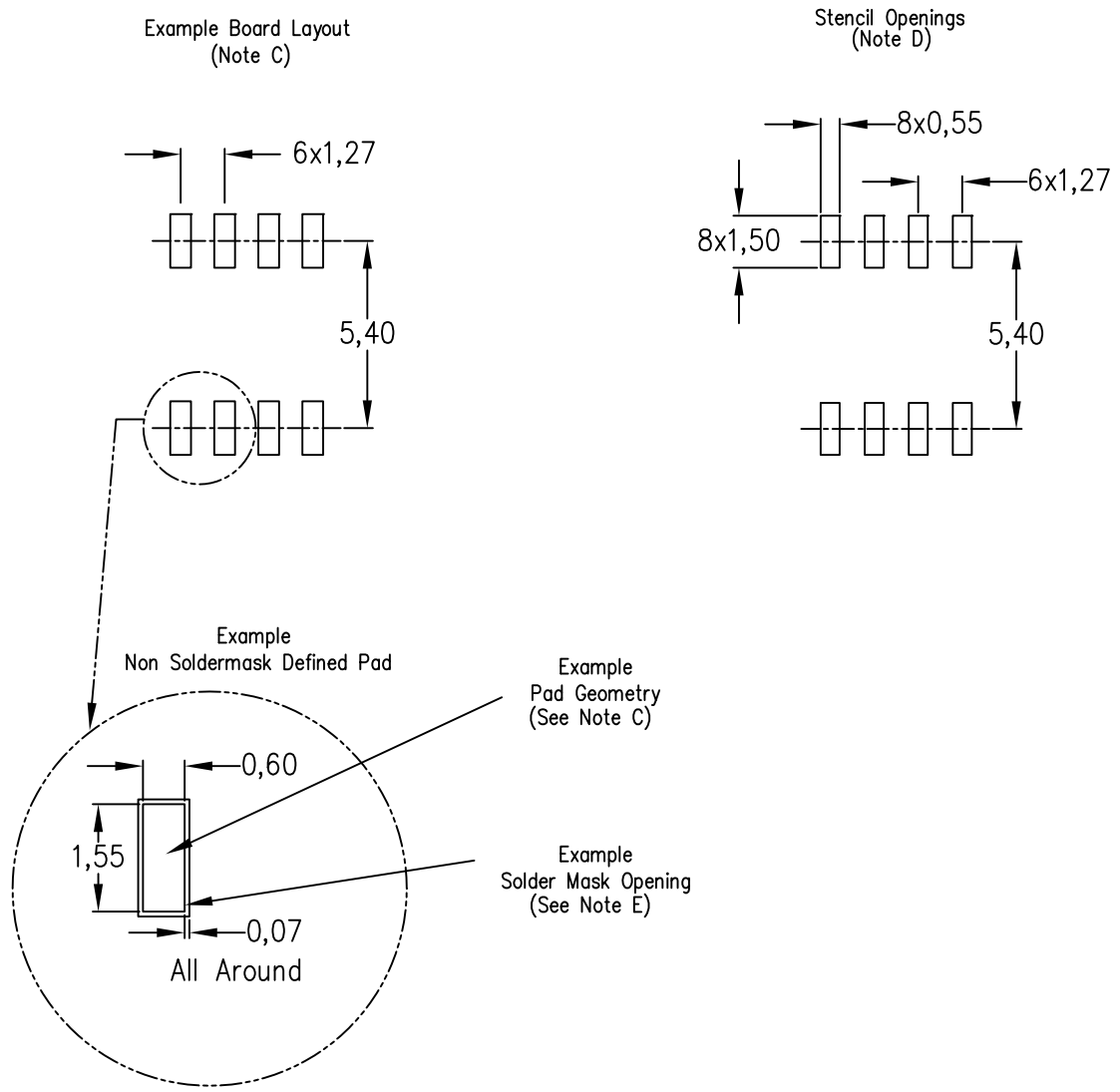
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4130CDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4130IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4130IDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4130IDR	SOIC	D	8	2500	367.0	367.0	38.0
THS4131CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131CDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4131CDR	SOIC	D	8	2500	367.0	367.0	38.0
THS4131IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131IDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4131IDR	SOIC	D	8	2500	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



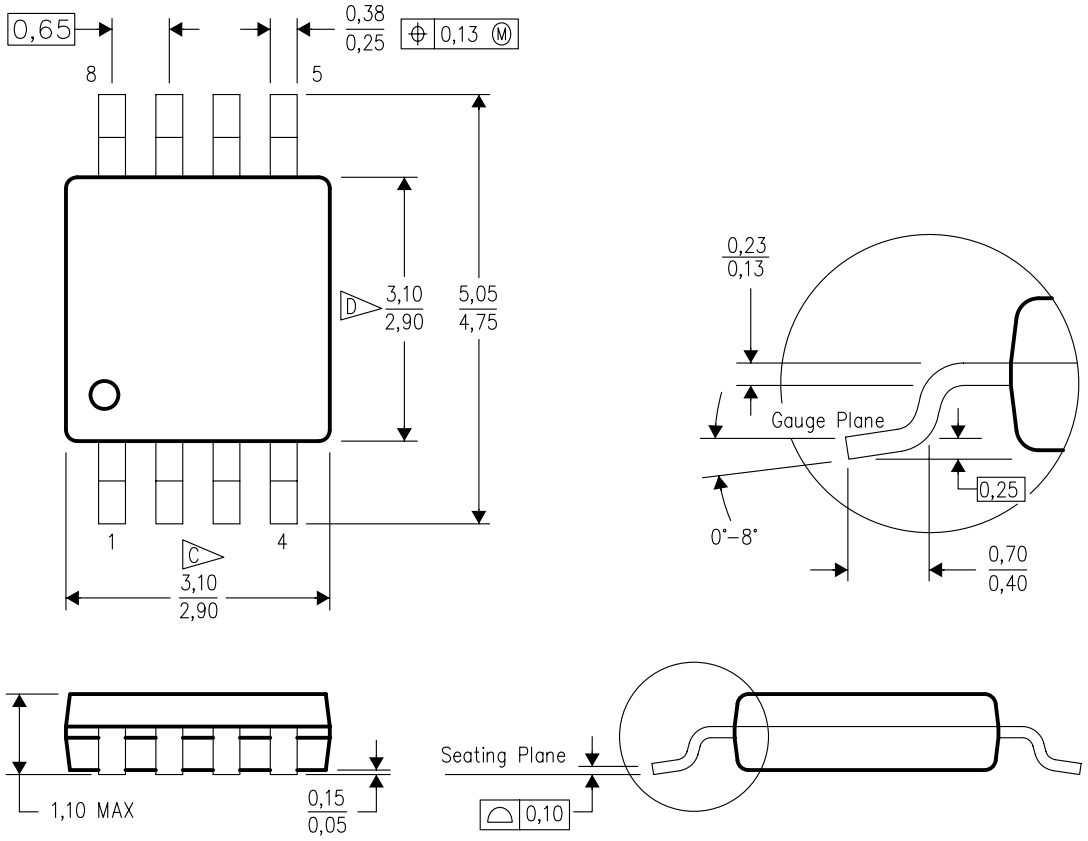
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

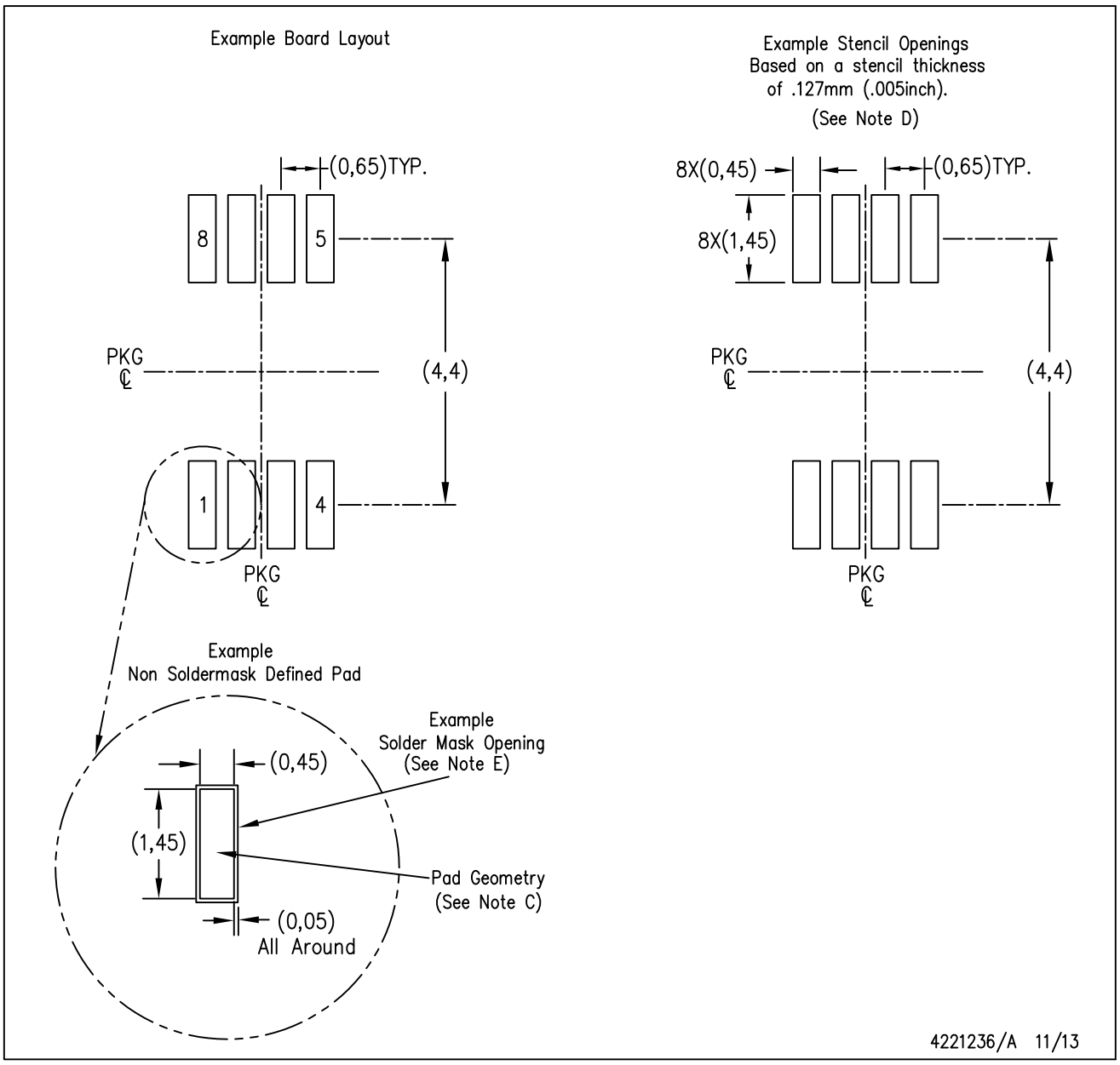
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

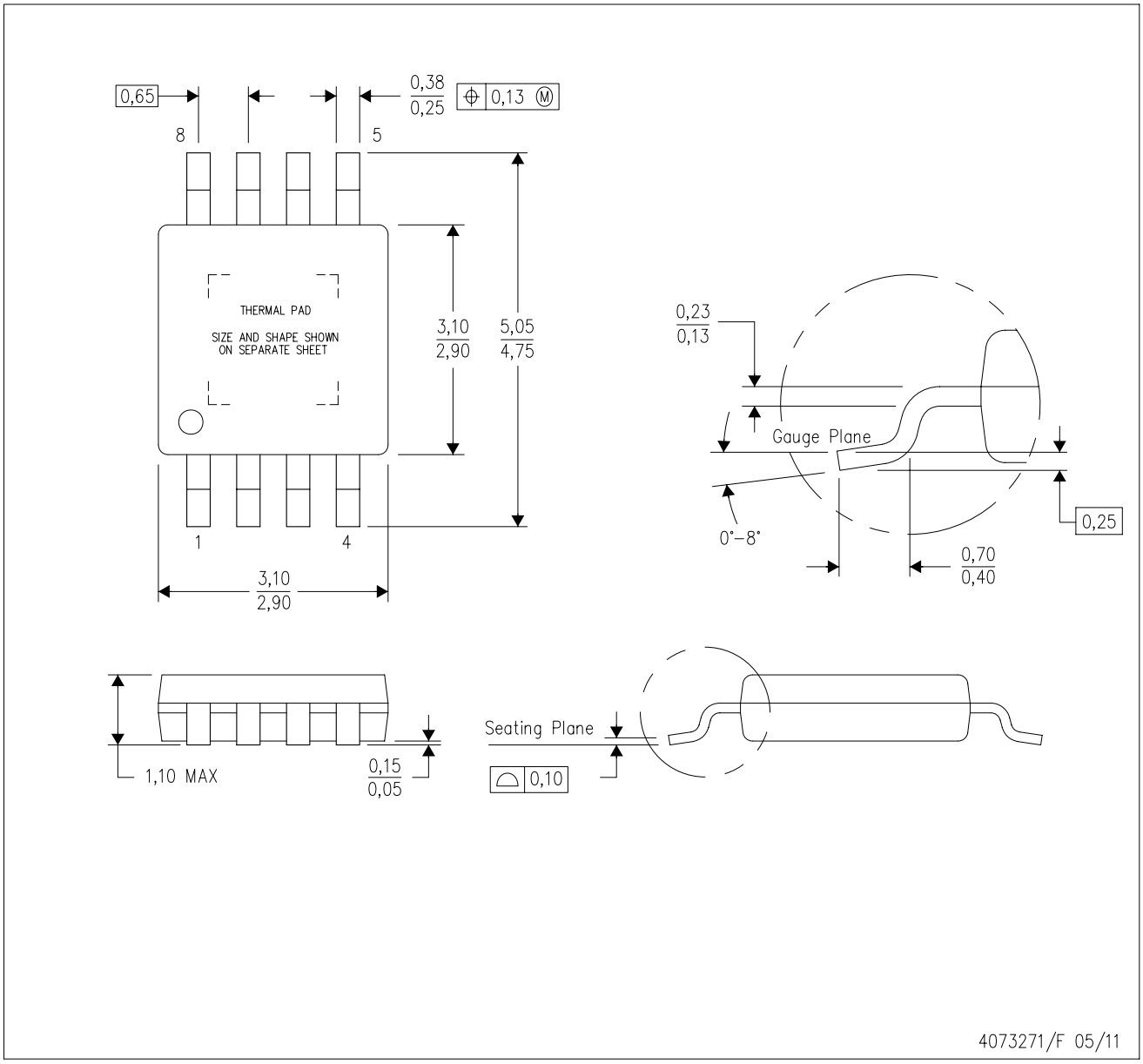
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

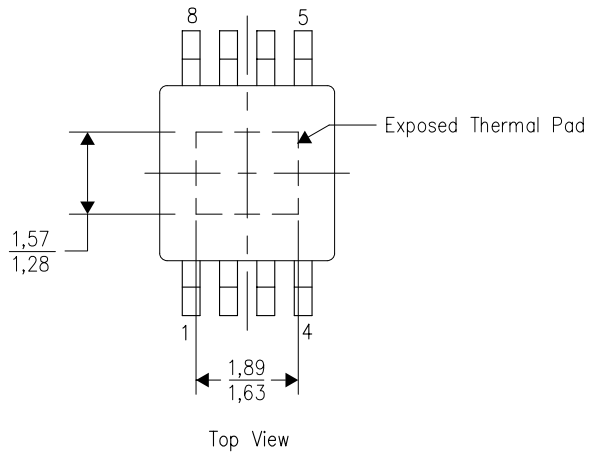
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

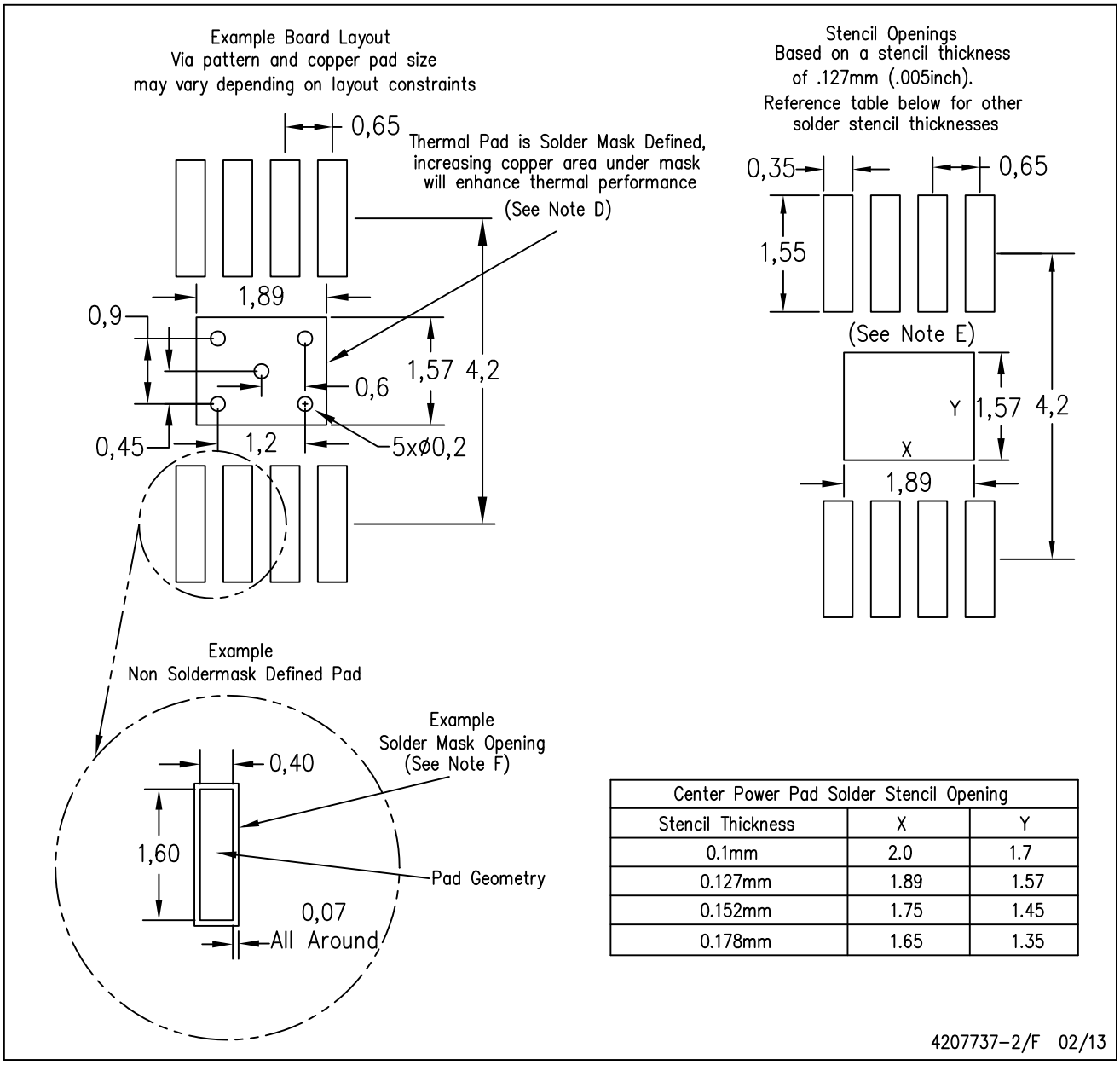
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

3mA, 100MHz, 750V/µs Operational Amplifier with Shutdown

FEATURES

- **100MHz Gain Bandwidth**
- **750V/µs Slew Rate**
- **3.6mA Maximum Supply Current**
- **50µA Supply Current in Shutdown**
- 8nV/√Hz Input Noise Voltage
- Unity-Gain Stable
- 1.5mV Maximum Input Offset Voltage
- 4µA Maximum Input Bias Current
- 400nA Maximum Input Offset Current
- 40mA Minimum Output Current, V_{OUT} = ±3V
- ±3.5V Minimum Input CMR, V_S = ±5V
- 30ns Settling Time to 0.1%, 5V Step
- Specified at ±5V, Single 5V Supplies
- Operating Temperature Range: –40°C to 85°C
- Low Profile (1mm) SOT-23 (ThinSOT™) and S8 Packages

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

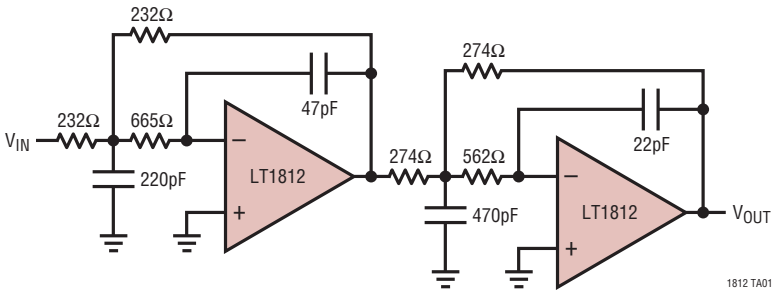
The LT®1812 is a low power, high speed, very high slew rate operational amplifier with excellent DC performance. The LT1812 features reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth. A power saving shutdown feature reduces supply current to 50µA. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier.

The output drives a 100Ω load to ±3.5V with ±5V supplies. On a single 5V supply, the output swings from 1.1V to 3.9V with a 100Ω load connected to 2.5V. The amplifier is stable with a 1000pF capacitive load which makes it useful in buffer and cable driver applications.

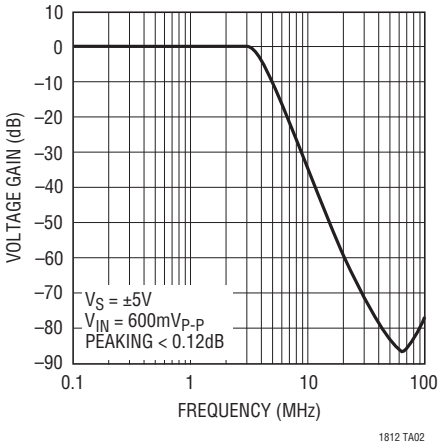
The LT1812 is manufactured on Linear Technology's advanced low voltage complementary bipolar process. The dual version is the LT1813. For higher supply voltage single, dual and quad operational amplifiers with up to 70MHz gain bandwidth, see the LT1351 through LT1365 data sheets.

TYPICAL APPLICATION

4MHz, 4th Order Butterworth Filter



Filter Frequency Response

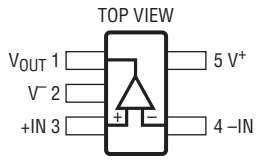


ABSOLUTE MAXIMUM RATINGS

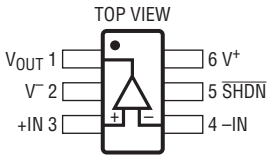
(Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Differential Input Voltage (Transient Only, Note 2) ..... ±3V
Input Voltage, Shutdown Voltage..... $\pm V_S$
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 8)..... –40°C to 85°C
Specified Temperature Range
(Note 8)..... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

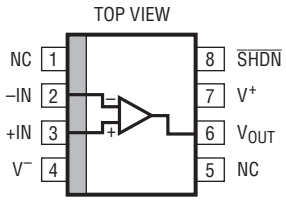
PIN CONFIGURATION



S5 PACKAGE
5-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W
(NOTE 9)



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 230°C/W
(NOTE 9)



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W
(NOTE 9)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1812CS5#PBF	LT1812CS5#TRPBF	LTLH	5-Lead Plastic TSOT-23	0°C to 70°C
LT1812IS5#PBF	LT1812IS5#TRPBF	LTLJ	5-Lead Plastic TSOT-23	–40°C to 85°C
LT1812CS6#PBF	LT1812CS6#TRPBF	LTLK	6-Lead Plastic TSOT-23	0°C to 70°C
LT1812IS6#PBF	LT1812IS6#TRPBF	LTLL	6-Lead Plastic TSOT-23	–40°C to 85°C
LT1812CS8#PBF	LT1812CS8#TRPBF	1812	8-Lead Plastic SO	0°C to 70°C
LT1812IS8#PBF	LT1812IS8#TRPBF	1812I	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = 0V unless otherwise noted (Note 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.4	1.5	mV
I_{OS}	Input Offset Current			30	400	nA
I_B	Input Bias Current			–0.9	±4	µA
e_n	Input Noise Voltage Density	f = 10kHz		8		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz		1		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = ±3.5V Differential	3	10 1.5		MΩ MΩ
C_{IN}	Input Capacitance			2		pF
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5	4.2 –4.2	 –3.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	75	85		dB
	Minimum Supply Voltage			±1.25	±2	V
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±5.5V	78	97		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 100Ω	1.5 1.0	3.0 2.5		V/mV V/mV
V_{OUT}	Maximum Output Swing	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	±3.80 ±3.35	±4.0 ±3.5		V V
I_{OUT}	Maximum Output Current	V_{OUT} = ±3V, 30mV Overdrive	±40	±60		mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 1V Overdrive (Note 3)	±75	±110		mA
SR	Slew Rate	A_V = –1 (Note 5)	500	750		V/µs
FPBW	Full Power Bandwidth	3V Peak (Note 6)		40		MHz
GBW	Gain Bandwidth Product	f = 200kHz	75	100		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V, R_L = 100Ω		2		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω		25		%
t_{PD}	Propagation Delay	A_V = 1, 50% V_{IN} to 50% V_{OUT}, 0.1V, R_L = 100Ω		2.8		ns
t_s	Settling Time	5V Step, 0.1%, A_V = –1		30		ns
THD	Total Harmonic Distortion	f = 1MHz, V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 500Ω		–76		dB
	Differential Gain	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.12		%
	Differential Phase	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.07		DEG
R_{OUT}	Output Resistance	A_V = 1, f = 1MHz		0.4		Ω
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)	 –100	0 –50	±1	µA µA
I_S	Supply Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)		3 50	3.6 100	mA µA

T_A = 25°C, V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V unless otherwise noted (Note 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.5	2.0	mV
I_{OS}	Input Offset Current			30	400	nA
I_B	Input Bias Current			–1.0	±4	µA
e_n	Input Noise Voltage Density	f = 10kHz		8		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz		1		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = 1.5V to 3.5V Differential	3	10 1.5		MΩ MΩ

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = 0V unless otherwise noted (Note 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance			2		pF
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5	4 1	 1.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V	73	82		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω V_{OUT} = 1.5V to 3.5V, R_L = 100Ω	1.0 0.7	2.0 1.5		V/mV V/mV
V_{OUT}	Maximum Output Swing (Positive)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	3.9 3.7	4.1 3.9		V V
	Maximum Output Swing (Negative)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive		0.9 1.1	1.1 1.3	V V
I_{OUT}	Maximum Output Current	V_{OUT} = 3.5V or 1.5V, 30mV Overdrive	±25	±40		mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 2.5V, 1V Overdrive (Note 3)	±55	±80		mA
SR	Slew Rate	A_V = –1 (Note 5)	200	350		V/µs
FPBW	Full Power Bandwidth	1V Peak (Note 6)		55		MHz
GBW	Gain Bandwidth Product	f = 200kHz	65	94		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V, R_L = 100Ω		2.1		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω		25		%
t_{PD}	Propagation Delay	A_V = 1, 50% V_{IN} to 50% V_{OUT}, 0.1V, R_L = 100Ω		3		ns
t_s	Settling Time	2V Step, 0.1%, A_V = –1		30		ns
THD	Total Harmonic Distortion	f = 1MHz, V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 500Ω		–75		dB
	Differential Gain	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.22		%
	Differential Phase	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.21		DEG
R_{OUT}	Output Resistance	A_V = 1, f = 1MHz		0.45		Ω
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)	 –50	0 –20	±1 	µA µA
I_S	Supply Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)		2.7 20	3.6 50	mA µA

0°C ≤ T_A ≤ 70°C, V_S = ±5V, V_{CM} = 0V unless otherwise noted (Note 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			2	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	15	µV/°C
I_{OS}	Input Offset Current				500	nA
I_B	Input Bias Current				±5	µA
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5		 –3.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	73			dB
	Minimum Supply Voltage				±2	V
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±5.5V	76			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 100Ω	1.0 0.7			V/mV V/mV
V_{OUT}	Maximum Output Swing	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	±3.70 ±3.25			V V
I_{OUT}	Maximum Output Current	V_{OUT} = ±3V, 30mV Overdrive	±35			mA

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_S = ±5V, V_{CM} = 0V unless otherwise noted (Note 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 1V Overdrive (Note 3)	±60			mA
SR	Slew Rate	A_V = –1 (Note 5)	400			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	65			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)	 –150		±1.5	µA µA
I_S	Supply Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)			4.6 150	mA µA

0°C ≤ T_A ≤ 70°C, V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V unless otherwise noted (Note 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			2.5	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	15	µV/°C
I_{OS}	Input Offset Current				500	nA
I_B	Input Bias Current				±5	µA
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5		 1.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V	71			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω V_{OUT} = 1.5V to 3.5V, R_L = 100Ω	0.7 0.5			V/mV V/mV
V_{OUT}	Maximum Output Swing (Positive)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	3.8 3.6			V V
	Maximum Output Swing (Negative)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive			1.2 1.4	V V
I_{OUT}	Maximum Output Current	V_{OUT} = 3.5V or 1.5V, 30mV Overdrive	±20			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 2.5V, 1V Overdrive (Note 3)	±45			mA
SR	Slew Rate	A_V = –1 (Note 5)	150			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	55			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)	 –75		±1.5	µA µA
I_S	Supply Current	$\overline{SHDN}$ > V^- + 2.0V (On) (Note 11) $\overline{SHDN}$ < V^- + 0.4V (Off) (Note 11)			4.5 75	mA µA

–40°C ≤ T_A ≤ 85°C. V_S = ±5V, V_{CM} = 0V unless otherwise noted (Notes 8, 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			3	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	30	µV/°C
I_{OS}	Input Offset Current				600	nA
I_B	Input Bias Current				±6	µA
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5		 –3.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	72			dB
	Minimum Supply Voltage				±2	V
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±5.5V	75			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 100Ω	0.8 0.6			V/mV V/mV

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$. $V_S = \pm5V$, $V_{CM} = 0V$ unless otherwise noted (Notes 8, 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Maximum Output Swing	$R_L = 500\Omega$, 30mV Overdrive $R_L = 100\Omega$, 30mV Overdrive	±3.60 ±3.15			V V
I_{OUT}	Maximum Output Current	$V_{OUT} = \pm3V$, 30mV Overdrive	±30			mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0V$, 1V Overdrive (Note 3)	±55			mA
SR	Slew Rate	$A_V = -1$ (Note 5)	350			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	60			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN} > V^- + 2.0V$ (On) (Note 11) $\overline{SHDN} < V^- + 0.4V$ (Off) (Note 11)	 –200		±2	µA µA
I_S	Supply Current	$\overline{SHDN} > V^- + 2.0V$ (On) (Note 11) $\overline{SHDN} < V^- + 0.4V$ (Off) (Note 11)			5 200	mA µA

$-40°C \le T_A \le 85°C$, $V_S = 5V$, $V_{CM} = 2.5V$, R_L to 2.5V unless otherwise noted (Notes 8, 10).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			3.5	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	30	µV/°C
I_{OS}	Input Offset Current				600	nA
I_B	Input Bias Current				±6	µA
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5		 1.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.5V$ to 3.5V	70			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = 1.5V$ to 3.5V, $R_L = 500\Omega$ $V_{OUT} = 2.0V$ to 3.0V, $R_L = 100\Omega$	0.6 0.4			V/mV V/mV
V_{OUT}	Maximum Output Swing (Positive)	$R_L = 500\Omega$, 30mV Overdrive $R_L = 100\Omega$, 30mV Overdrive	3.7 3.5			V V
	Maximum Output Swing (Negative)	$R_L = 500\Omega$, 30mV Overdrive $R_L = 100\Omega$, 30mV Overdrive			1.3 1.5	V V
I_{OUT}	Maximum Output Current	$V_{OUT} = 3.5V$ or 1.5V, 30mV Overdrive	±17			mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 2.5V$, 1V Overdrive (Note 3)	±40			mA
SR	Slew Rate	$A_V = -1$ (Note 5)	125			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	50			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN} > V^- + 2.0V$ (On) (Note 11) $\overline{SHDN} < V^- + 0.4V$ (Off) (Note 11)	 –100		±2	µA µA
I_S	Supply Current	$\overline{SHDN} > V^- + 2.0V$ (On) (Note 11) $\overline{SHDN} < V^- + 0.4V$ (Off) (Note 11)			5 100	mA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Differential inputs of ±3V are appropriate for transient operation only, such as during slewing. Large sustained differential inputs can cause excessive power dissipation and may damage the part.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between ±2V on the output with ±3V input for ±5V supplies and $2V_{P-P}$ on the output with a $3V_{P-P}$ input for single 5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate: $FPBW = SR/2\pi V_P$

Note 7: This parameter is not 100% tested.

Note 8: The LT1812C is guaranteed to meet specified performance from 0°C to 70°C. The LT1812C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1812I is guaranteed to meet specified performance from –40°C to 85°C.

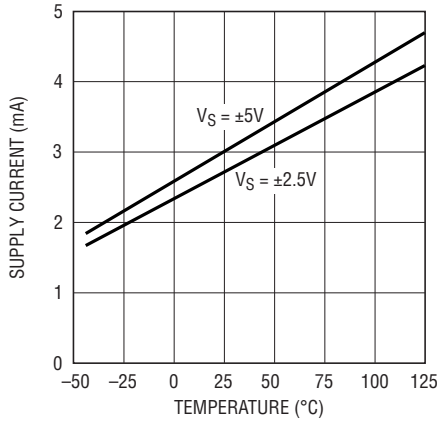
Note 9: Thermal resistance varies with the amount of PC board metal connected to the package. The nominal values are for short traces connected to the pins. The thermal resistance can be substantially reduced by connecting Pin 2 of the 5-lead or 6-lead TSOT-23 or Pin 4 of the SO-8 to a large metal area.

Note 10: For the 8-lead SO and 6-lead TSOT-23 parts, the electrical characteristics apply to the "ON" state, unless otherwise noted. These parts are in the "ON" state when either $\overline{SHDN}$ is not connected, or $\overline{SHDN} > V^- + 2.0V$.

Note 11: The shutdown ($\overline{SHDN}$) feature is not available on the 5-lead SOT-23 parts. These parts are always in the "ON" state.

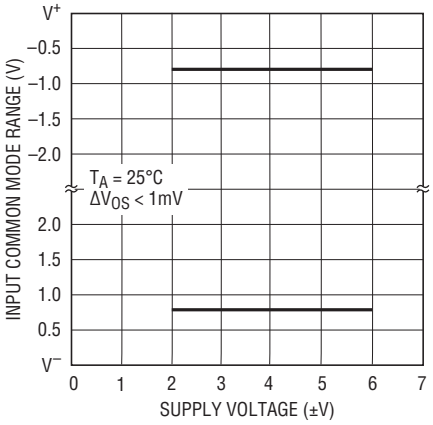
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



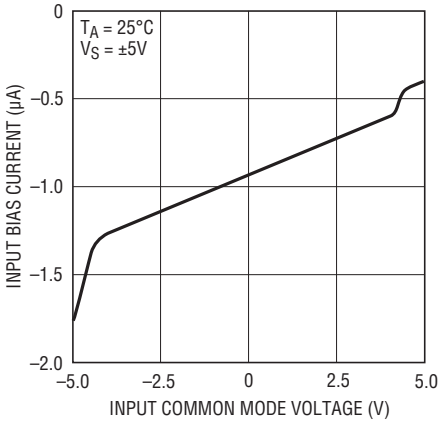
1812 G01

Input Common Mode Range vs Supply Voltage



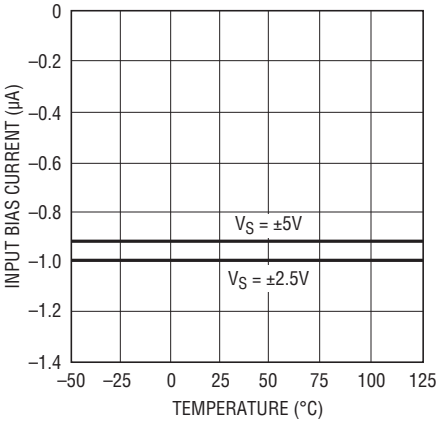
1812 G02

Input Bias Current vs Common Mode Voltage



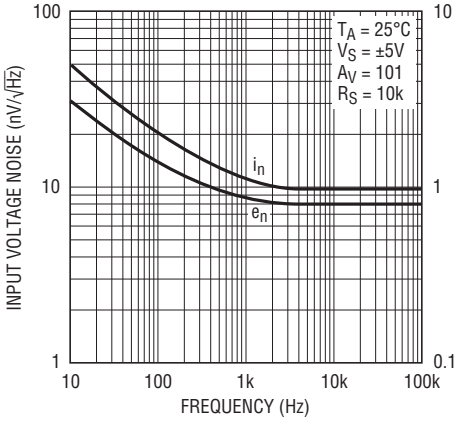
1812 G03

Input Bias Current vs Temperature



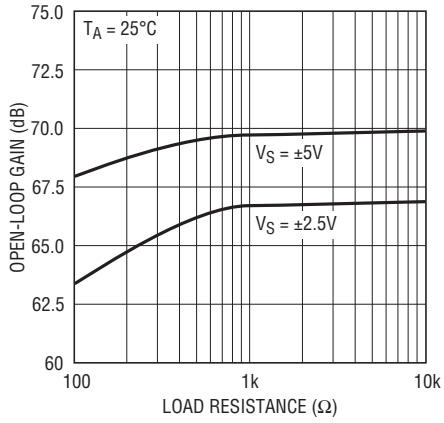
1812 G04

Input Noise Spectral Density



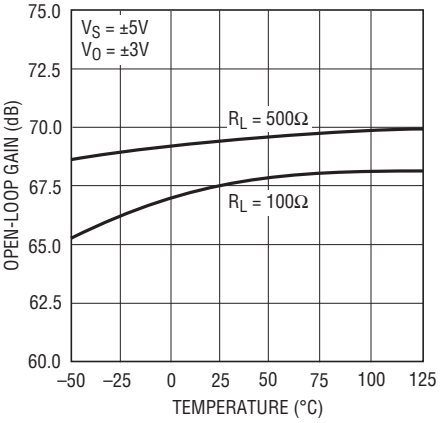
1812 G05

Open-Loop Gain vs Resistive Load



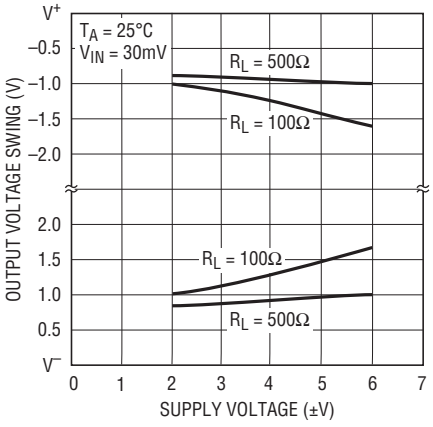
1812 G06

Open-Loop Gain vs Temperature



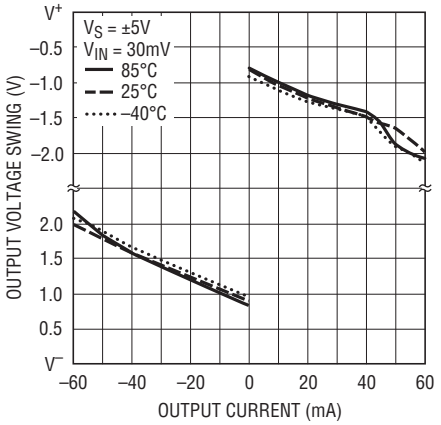
1812 G07

Output Voltage Swing vs Supply Voltage



1812 G08

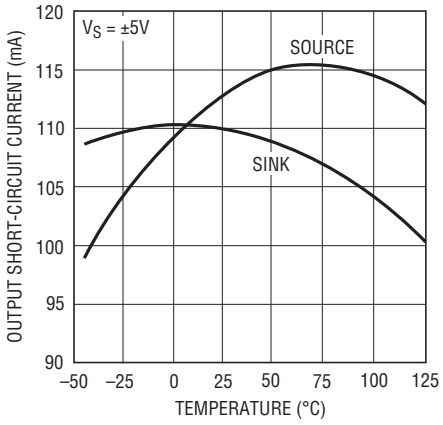
Output Voltage Swing vs Load Current



1812 G09

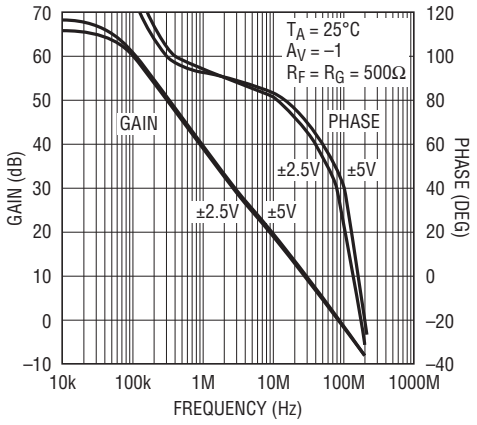
TYPICAL PERFORMANCE CHARACTERISTICS

Output Short-Circuit Current vs Temperature



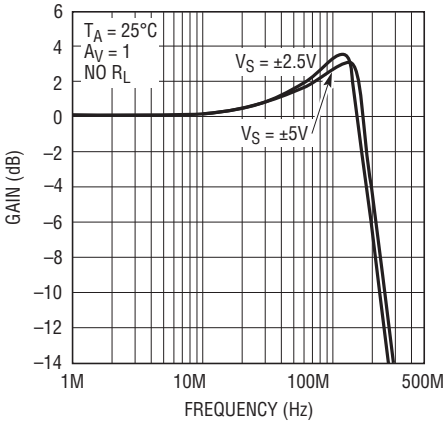
1812 G10

Open-Loop Gain and Phase vs Frequency



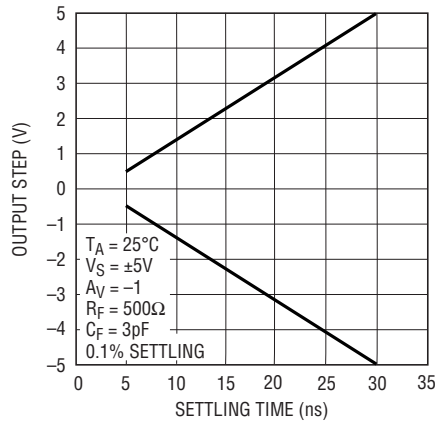
1812 G13

Gain vs Frequency



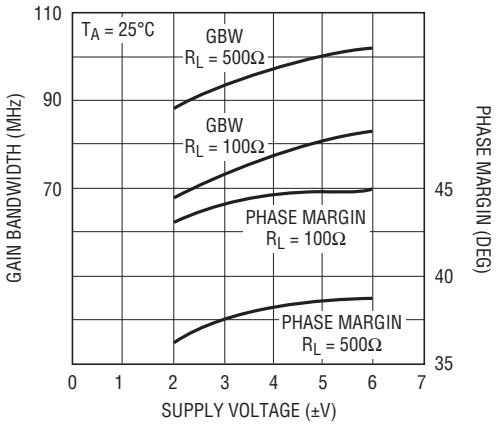
1812 G16

Settling Time vs Output Step



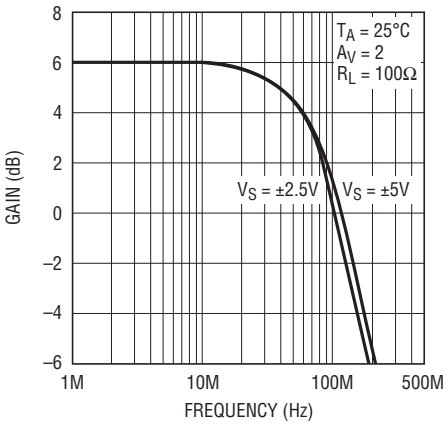
1812 G11

Gain Bandwidth and Phase Margin vs Supply Voltage



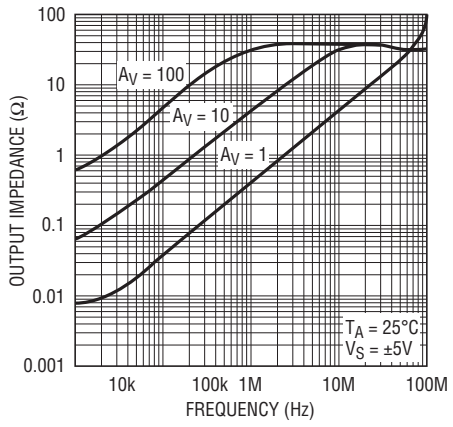
1812 G19

Gain vs Frequency



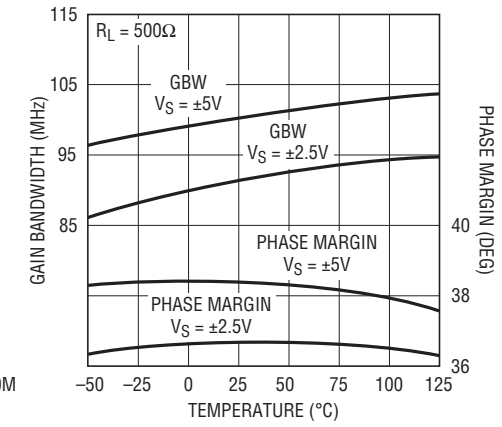
1812 G17

Output Impedance vs Frequency



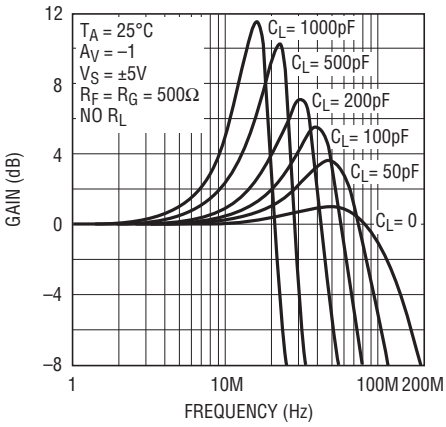
1812 G12

Gain Bandwidth and Phase Margin vs Temperature



1812 G15

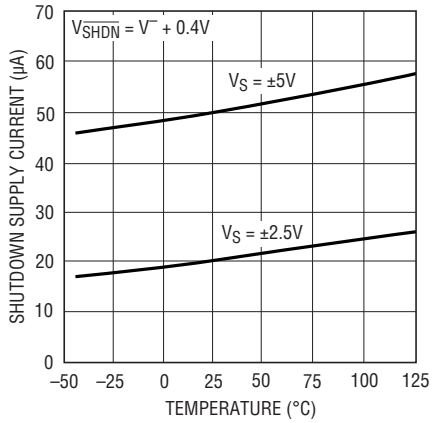
Gain vs Frequency



1812 G18

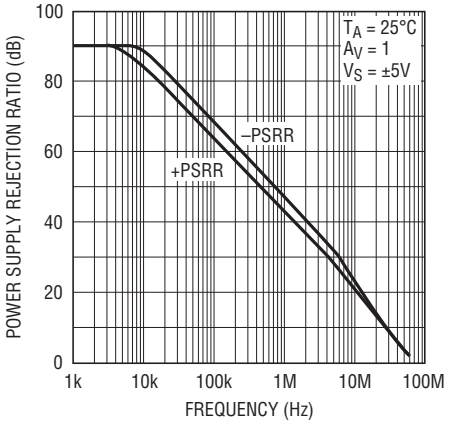
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Supply Current vs Temperature



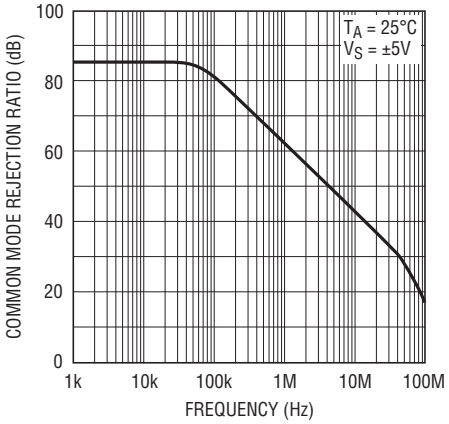
1812 G14

Power Supply Rejection Ratio vs Frequency



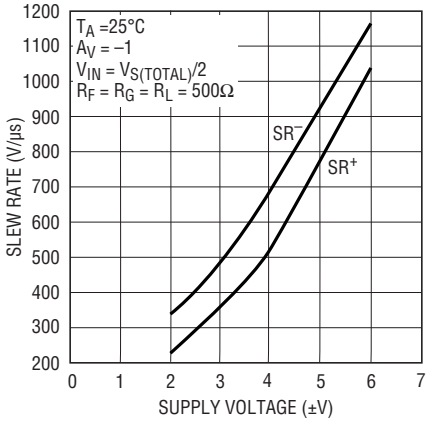
1812 G20

Common Mode Rejection Ratio vs Frequency



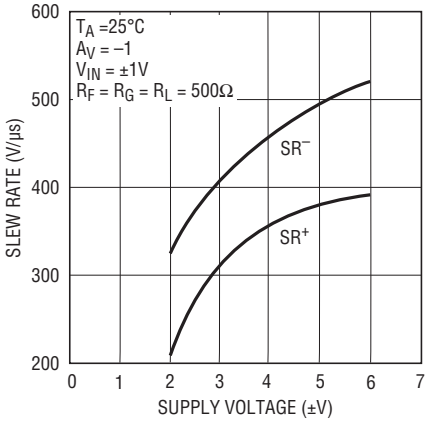
1812 G21

Slew Rate vs Supply Voltage



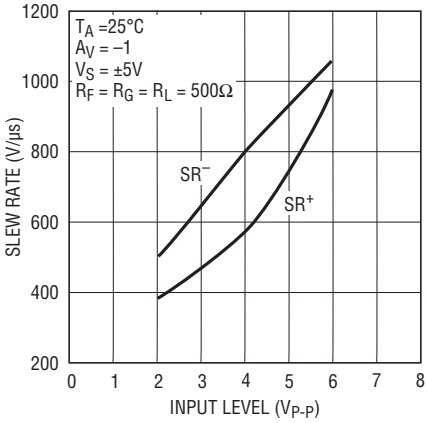
1812 G22

Slew Rate vs Supply Voltage



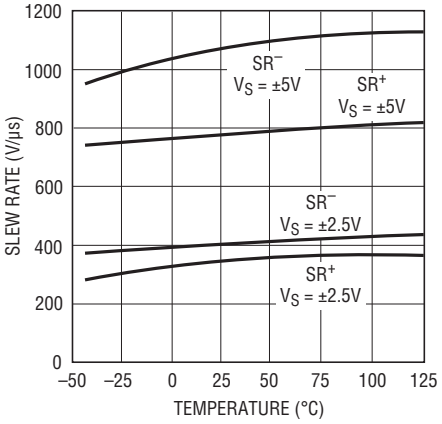
1812 G23

Slew Rate vs Input Level



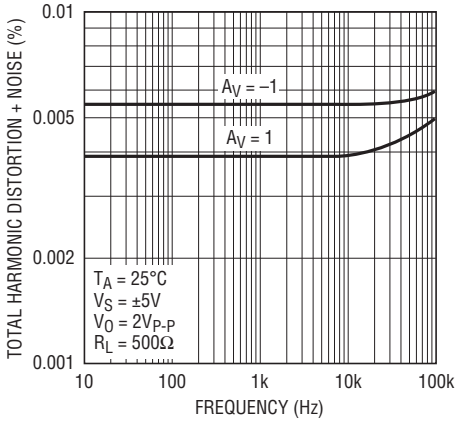
1812 G24

Slew Rate vs Temperature



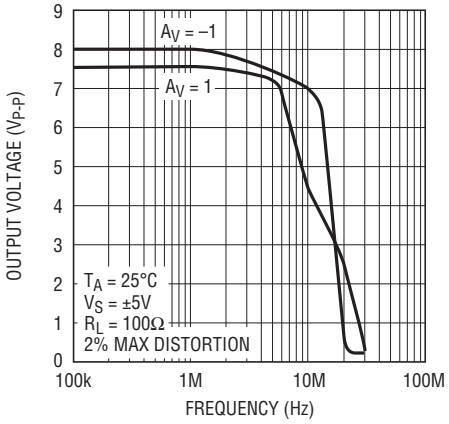
1812 G25

Total Harmonic Distortion + Noise vs Frequency



1812 G26

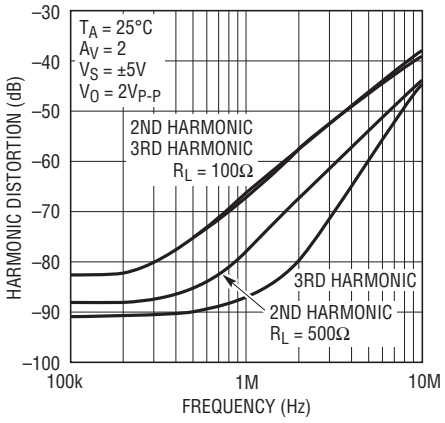
Undistorted Output Swing vs Frequency



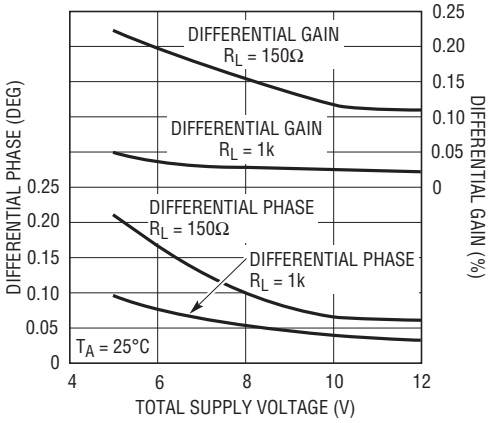
1812 G27

TYPICAL PERFORMANCE CHARACTERISTICS

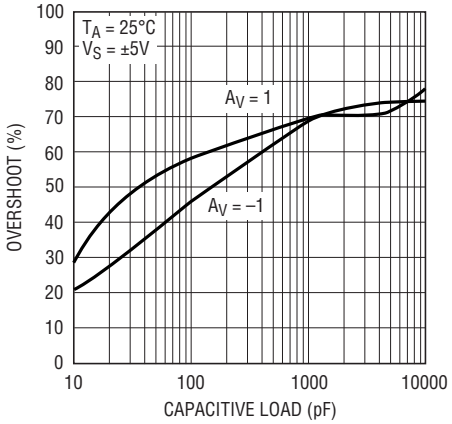
2nd and 3rd Harmonic Distortion vs Frequency



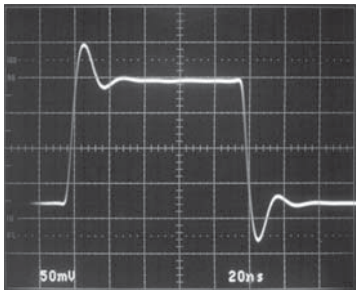
Differential Gain and Phase vs Supply Voltage



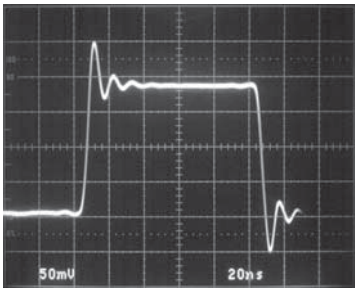
Capacitive Load Handling



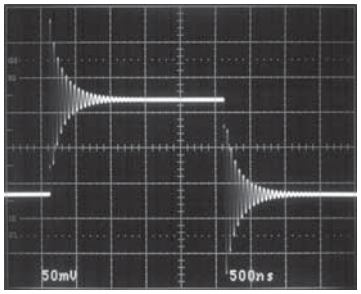
Small-Signal Transient, A_V = –1



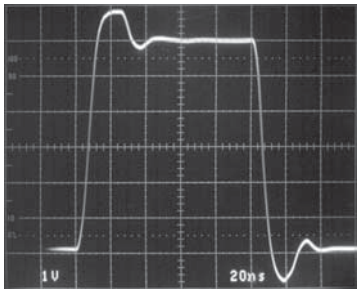
Small-Signal Transient, A_V = 1



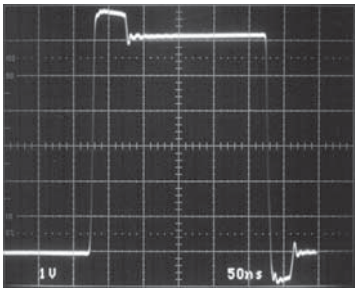
Small-Signal Transient, A_V = 1, C_L = 1000pF



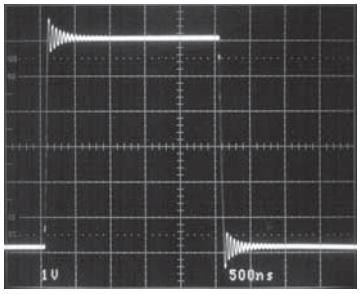
Large-Signal Transient, A_V = –1



Large-Signal Transient, A_V = 1



Large-Signal Transient, A_V = 1, C_L = 1000pF



APPLICATIONS INFORMATION

Layout and Passive Components

The LT1812 amplifier is more tolerant of less than ideal layouts than other high speed amplifiers. For maximum performance (for example, fast settling) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications, use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. If feedback resistors greater than 2k are used, a parallel capacitor of value

$$C_F > R_G \bullet C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is 1 and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be an I-to-V converter.

Input Considerations

Each of the LT1812 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 3V without damage and need no clamping or source resistance for protection.

The device should not be used as a comparator because with sustained differential inputs, excessive power dissipation may result.

Capacitive Loading

The LT1812 is stable with a 1000pF capacitive load, which is outstanding for a 100MHz amplifier. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity, a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Slew Rate

The slew rate is proportional to the differential input voltage. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 5V output step in a gain of 10 has a 0.5V input step, whereas in unity gain there is a 5V input step. The LT1812 is tested for slew rate in a gain of –1. Lower slew rates occur in higher gain configurations.

Shutdown

The LT1812 has a shutdown pin ($\overline{SHDN}$, Pin 8) for conserving power. When this pin is open or biased at least 2V above the negative supply, the part operates normally. When pulled down to V^-, the supply current drops to about 50µA. Typically, the turn-off delay is 1µs and the turn-on delay 0.5µs. The current out of the $\overline{SHDN}$ pin is also typically 50µA. In shutdown mode, the amplifier output is not isolated from the inputs, so the LT1812 shutdown feature cannot be used for multiplexing applications. The 50µA typical shutdown current is exclusive of any output (load) current. In order to prevent load current (and maximize the power savings), either the load needs to be disconnected, or the input signal needs to be 0V. Even in shutdown mode, the LT1812 can still drive significant current into a load. For example, in an A_V = 1 configuration, when driven with a 1V DC input, the LT1812 drives 2mA into a 100Ω load. It takes about 500µs for the load current to reach this value.

Power Dissipation

The LT1812 combines high speed and large output drive in a small package. It is possible to exceed the maximum junction temperature under certain conditions. Maximum

APPLICATIONS INFORMATION

junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$T_J = T_A + (P_D \bullet \theta_{JA})$ (Note 9)

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current. The worst-case load induced power occurs when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$P_{DMAX} = (V^+ – V^–)(I_{SMAX}) + (V^+/2)^2/R_L$ or

$P_{DMAX} = (V^+ – V^–)(I_{SMAX}) + (V^+ – V_{OMAX})(V_{OMAX}/R_L)$

Example: LT1812CS5 at 70°C, $V_S = \pm 5V$, $R_L = 100\Omega$

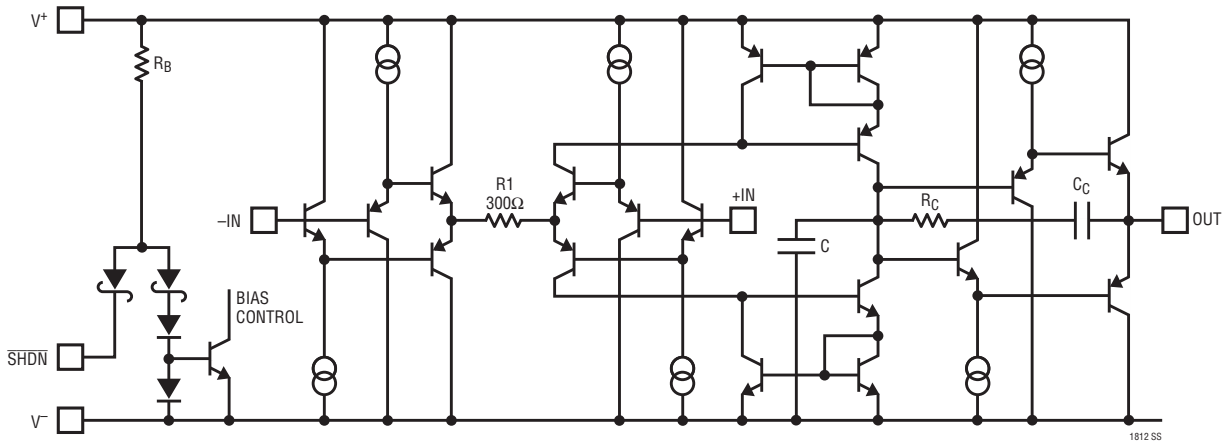
$P_{DMAX} = (10V)(4.5mA) + (2.5V)^2/100\Omega = 108mW$

$T_{JMAX} = 70°C + (108mW)(250°C/W) = 97°C$

Circuit Operation

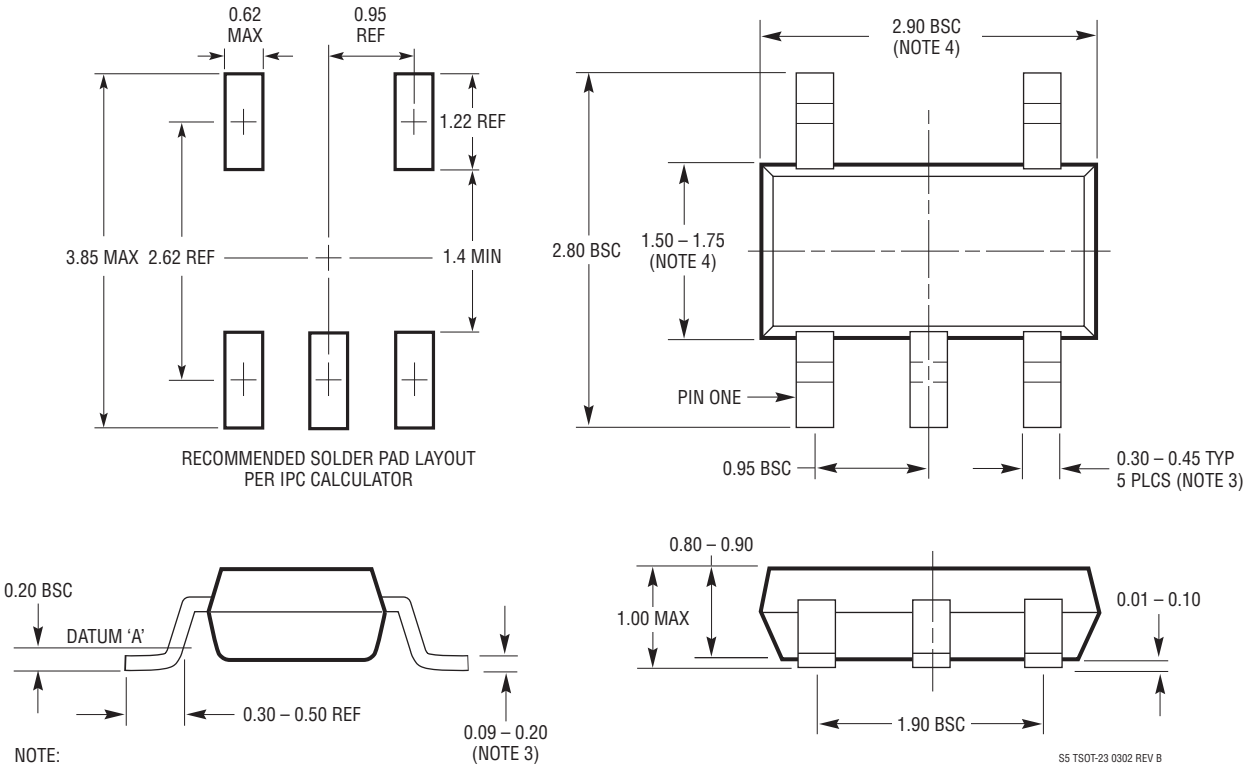
The LT1812 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. The inputs are buffered by complementary NPN and PNP emitter followers that drive a 300Ω resistor. The input voltage appears across the resistor generating currents that are mirrored into the high impedance node. Complementary followers form an output stage that buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving capacitive loads (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain cross away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that the total phase lag does not exceed 180 degrees (zero phase margin) and the amplifier remains stable. In this way, the LT1812 is stable with up to 1000pF capacitive loads in unity gain, and even higher capacitive loads in higher closed-loop gain configurations.

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

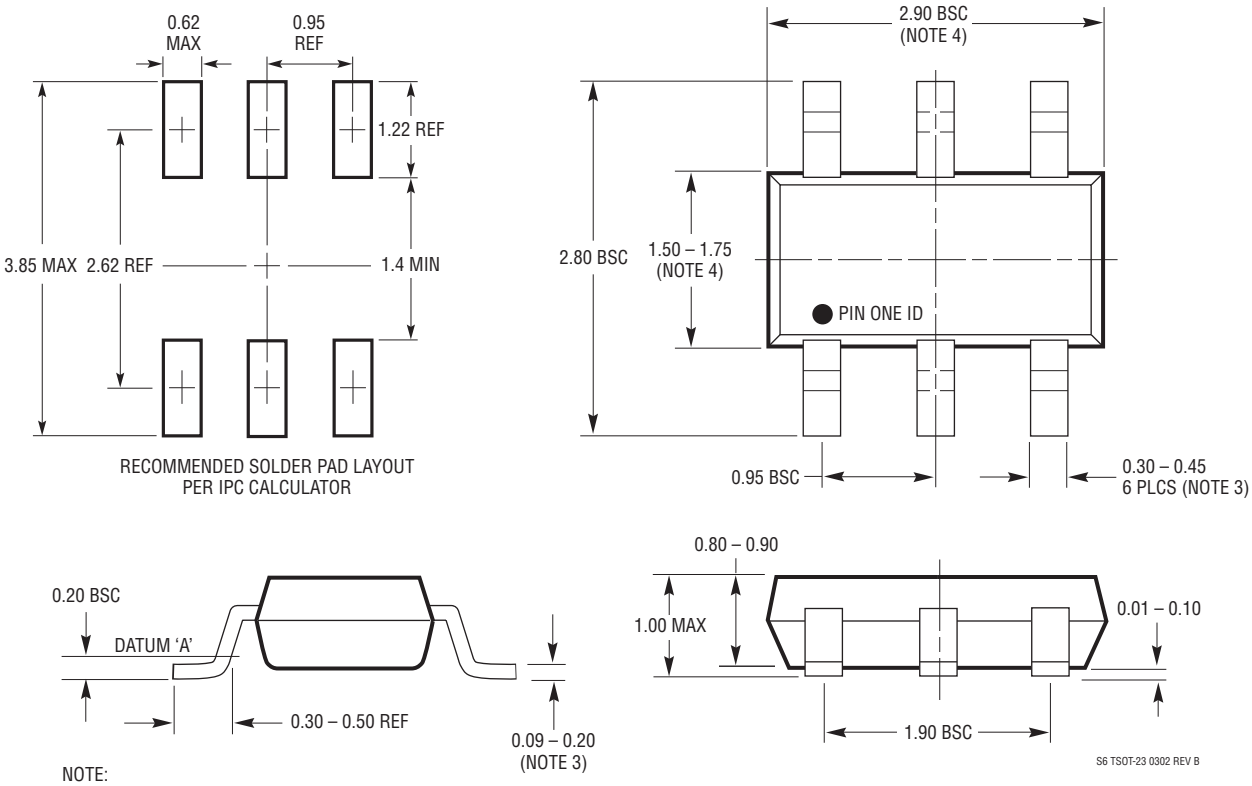
S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

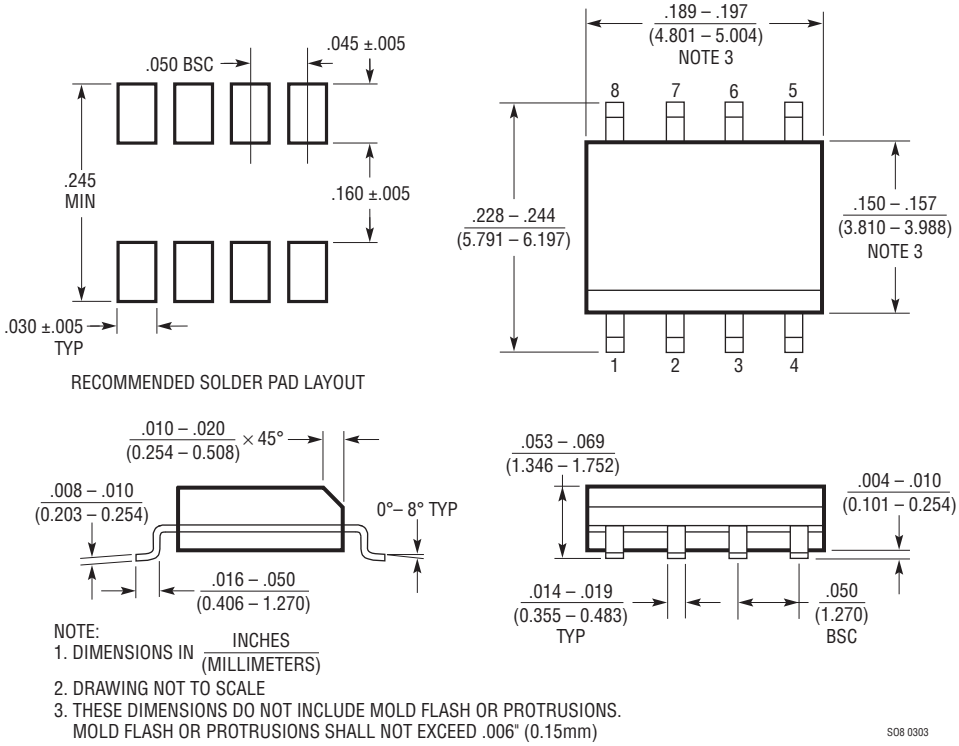
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

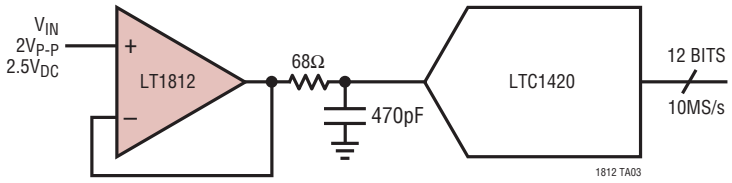


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

TYPICAL APPLICATION

Single 5V Supply 10MS/s 12-Bit ADC Buffer



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1360/LT1361/LT1362	Single/Dual/Quad 50MHz, 800V/µs, C-Load™ Amplifiers	4mA Supply Current, 1mV Max V_{OS}, 1µA Max I_B
LT1363/LT1364/LT1365	Single/Dual/Quad 70MHz, 1000V/µs, C-Load Amplifiers	50mA Output Current, 1.5mV Max V_{OS}, 2µA Max I_B
LT1395/LT1396/LT1397	Single/Dual/Quad 400MHz Current Feedback Amplifiers	4.6mA Supply Current, 800V/µs, 80mA Output Current
LT1806	325MHz, 140V/µs Rail-to-Rail I/O Op Amp	Low Noise 3.5nV/$\sqrt{Hz}$
LT1809	180MHz, 350V/µs Rail-to-Rail I/O Op Amp	Low Distortion –90dBc at 5MHz
LT1813	Dual 3mA, 100MHz, 750V/µs Operational Amplifier	Dual Version of the LT1812

C-Load is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0909 REV B • PRINTED IN USA

DB2S308

Silicon epitaxial planar type

For high speed switching circuits

■ Features

- Low forward voltage V_F
- Short reverse recovery time t_{rr}
- Halogen-free / RoHS compliant
  (EU RoHS / UL-94 V-0 / MSL: Level 1 compliant)

■ Marking Symbol: C2

■ Packaging

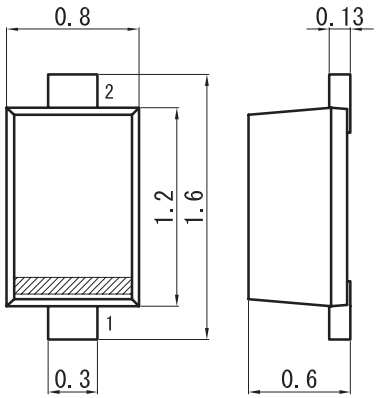
DB2S30800L Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25°C$

Parameter	Symbol	Rating	Unit
Reverse voltage	V_R	30	V
Repetitive peak reverse voltage	V_{RRM}	30	V
Forward current (Average)	$I_{F(AV)}$	100	mA
Peak forward current	I_{FM}	200	mA
Non-repetitive peak forward surge current *1	I_{FSM}	1	A
Junction temperature	T_j	125	°C
Operating ambient temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note) ∗1: 50 Hz sine wave 1 cycle (Non-repetitive peak current)

Unit: mm



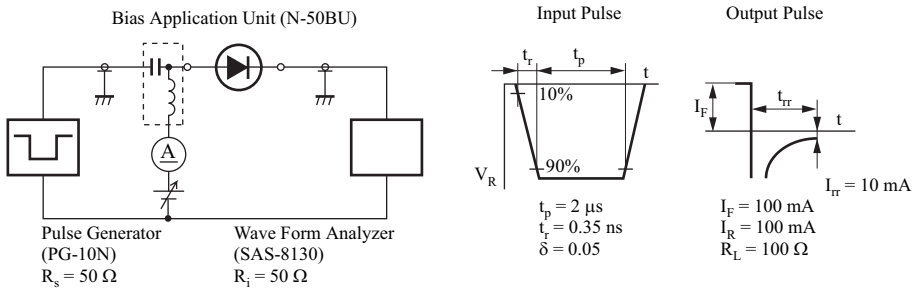
1: Cathode
2: Anode

Panasonic	SSMini2-F5-B
JEITA	SC-79
Code	SOD-523

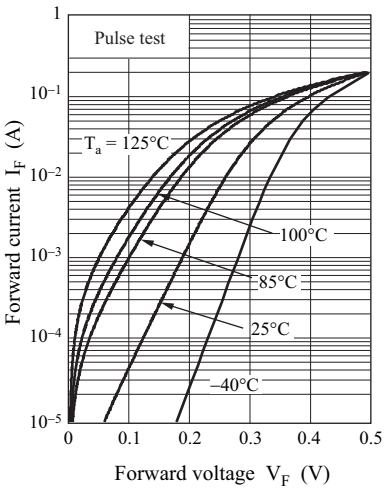
■ Electrical Characteristics $T_a = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Forward voltage	V_{F1}	$I_F = 10$ mA			0.29	V
	V_{F2}	$I_F = 100$ mA			0.42	
Reverse current	I_{R1}	$V_R = 10$ V			25	μA
	I_{R2}	$V_R = 30$ V			120	
Terminal capacitance	C_t	$V_R = 10$ V, f = 1 MHz		2.9		pF
Reverse recovery time *1	t_{rr}	$I_F = I_R = 100$ mA, $I_{rr} = 10$ mA, $R_L = 100\ \Omega$		1.3		ns

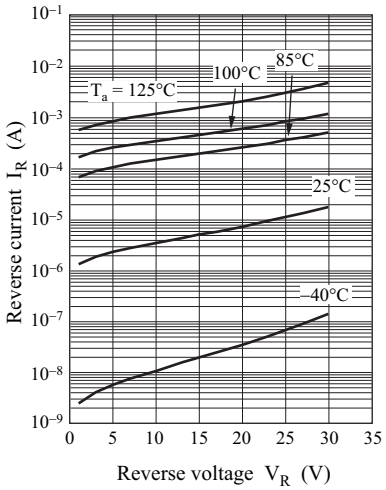
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 measuring methods for diodes.
2. This product is sensitive to electric shock (static electricity, etc.). Due attention must be paid on the charge of a human body and the leakage of current from the operating equipment.
3. Absolute frequency of input and output is 250 MHz
∗1: t_{rr} measurement circuit



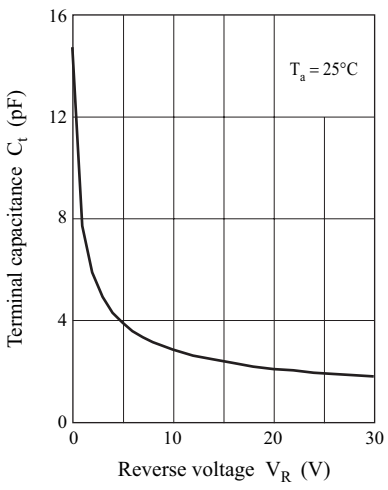
I_F — V_F



I_R — V_R

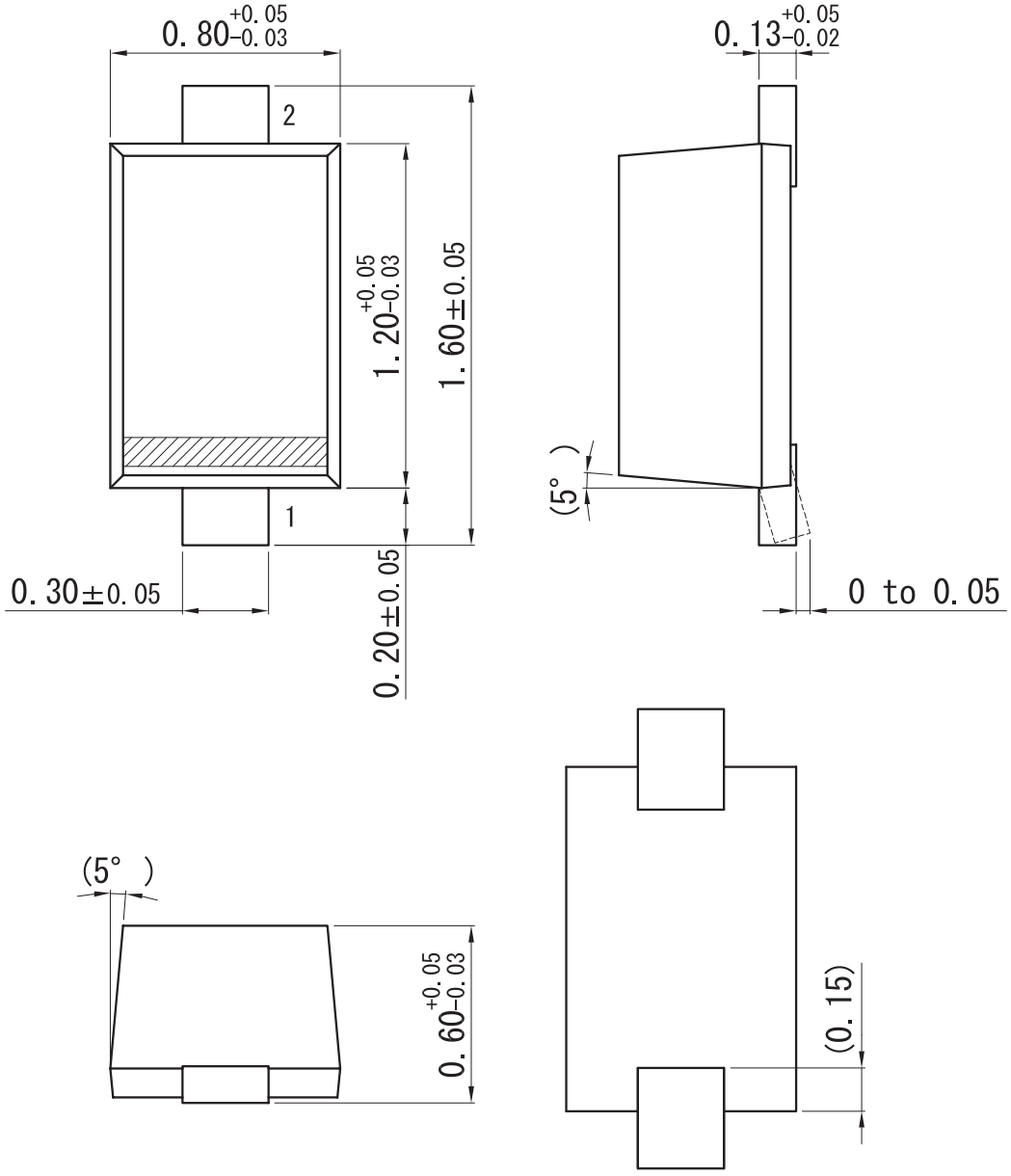


C_t — V_R

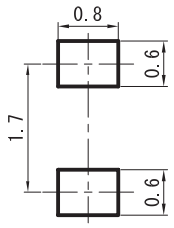


SSMini2-F5-B

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information de-scribed in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Please consult with our sales staff in advance for information on the following applications, moreover please exchange documents separately on terms of use etc.: Special applications (such as for in-vehicle equipment, airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, medical equipment and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
Unless exchanging documents on terms of use etc. in advance, it is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application.

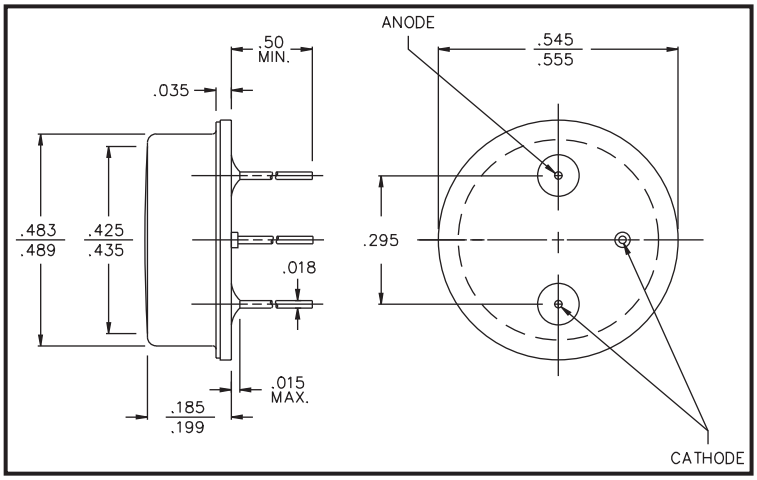
(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. We do not guarantee quality for disassembled products or the product re-mounted after removing from the mounting board.
When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

(7) When reselling products described in this book to other companies without our permission and receiving any claim of request from the resale destination, please understand that customers will bear the burden.

No.010618



FEATURES

- TO-8 hermetic package
- Circular active area
- Low capacitance

ELECTRO-OPTICAL CHARACTERISTICS AT 25°C

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Active Area	4mm DIA.		12		mm^2
Responsivity, $\mathcal{R}$	@ 632nm	0.35	0.40		A/W
Dark Current, Idr	V_R = 10V		3	7	nA
Reverse Breakdown Voltage, V_R	I_R = 10A	25	60		Volts
Capacitance, C	V_R = 10V		25		pF
Rise Time	V_R = 10V		15		nsec
Series Resistance	V_f = 1V		35	100	Ohms

THERMAL PARAMETERS

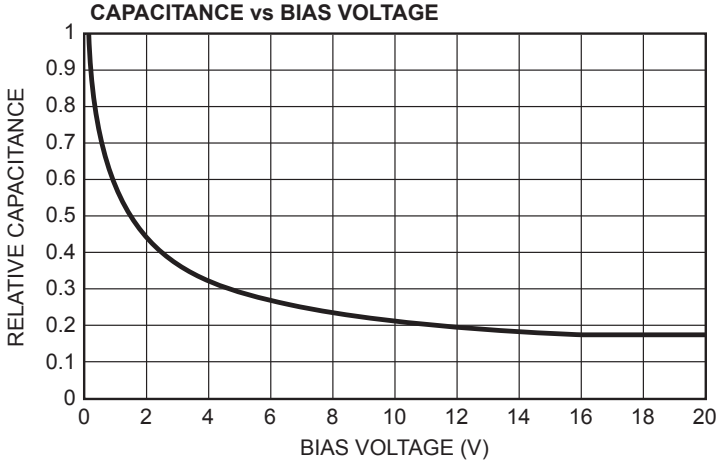
Storage and Operating Temperature Range	-55°C TO 100°C
Maximum Junction Temperature	100°C
Lead Soldering Temperature[1]	260°

[1] 1/16" from case for 10 seconds.

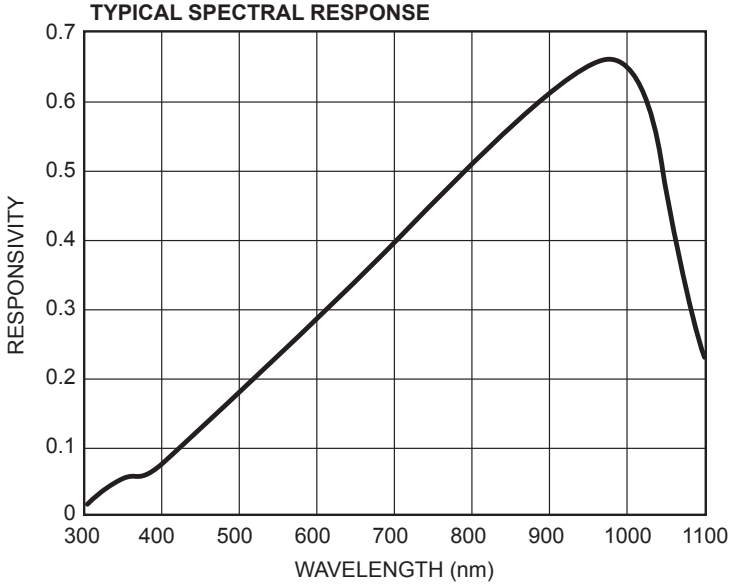
OPTO DIODE
1260 Calle Suerte, Camarillo, California 93012
Phone: (805) 499-0335, Fax: (805) 499-8108
Email: sales@optodiode.com, Website: www.optodiode.com

Revision February 26, 2013

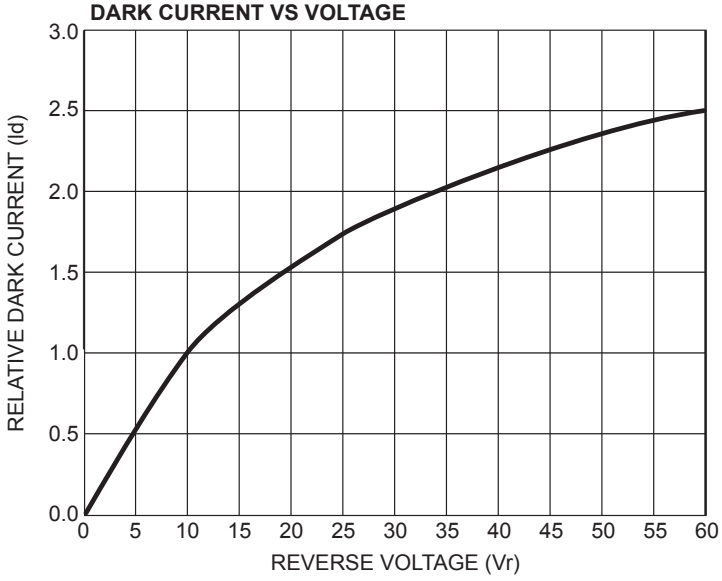
CAPACITANCE vs BIAS VOLTAGE



TYPICAL SPECTRAL RESPONSE



DARK CURRENT VS VOLTAGE



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Sprague-Goodman

ENGINEERING BULLETIN
SG-305K.1
Supercedes SG-305J

CERAMIC DIELECTRIC TRIMMER CAPACITORS

SPRAGUE GOODMAN

Sprague-Goodman Electronics, Inc.
1700 SHAMES DRIVE, WESTBURY, NY 11590
TEL: 516-334-8700 • FAX: 516-334-8771
E-MAIL: info@spraguegoodman.com

SURFTRIM® SURFACE MOUNT
GKRP SERIES

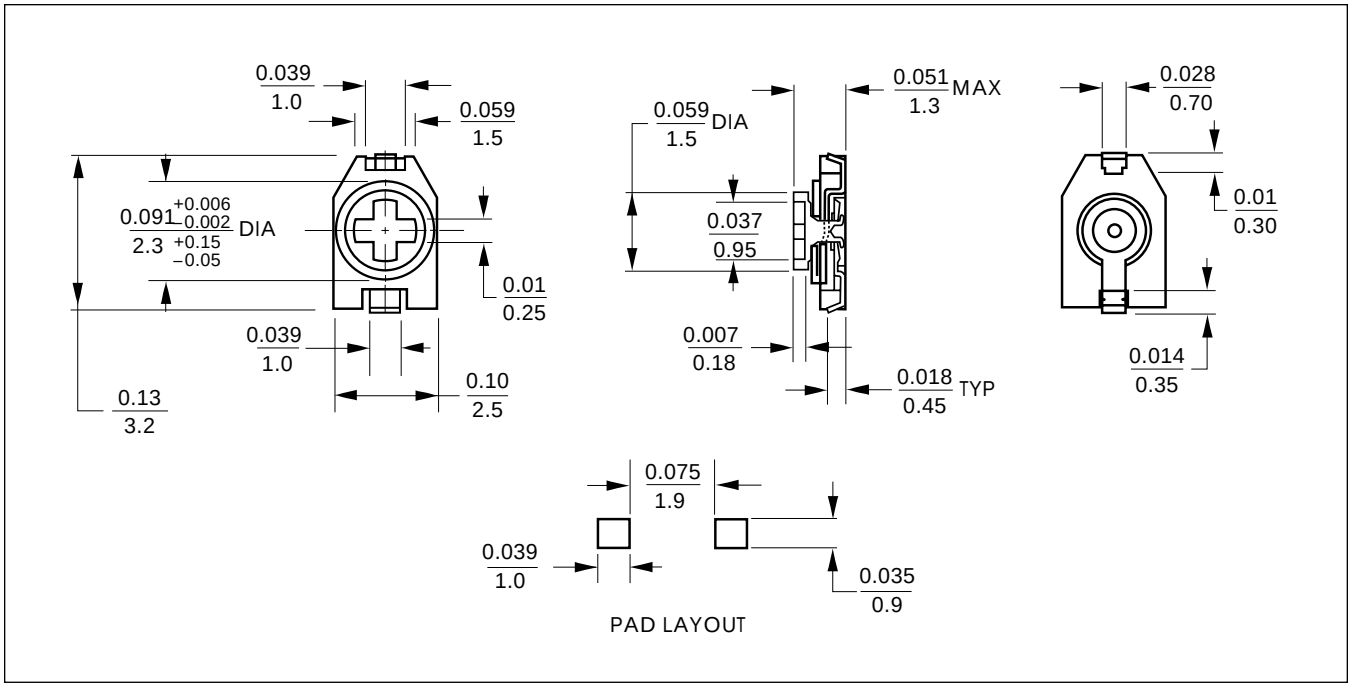
FEATURES
- Sealed for washability
- Low mounting profile.
- Carrier and reel packaging standard.
- NPO temperature coefficient (up to 10 pF max).
- Self resonant frequency above 1 GHz.

SPECIFICATIONS
Operating Temperature Range: –40°C to +85°C
Voltage Rating: 25 VDC
Dielectric Withstanding Voltage: 75 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 10 to 150 g-cm (0.14 to 2.1 oz-in)

3.2 x 2.5 x 1.3 mm Models

Capacitance (pF)		TCC (ppm / °C)	Q min (1 MHz)	Carrier and Reel Pack Model No.
min	max			
3.0	5.0	0 ± 500	150	GKRP5R066
3.0	10.0	0 ± 500	150	GKRP10066
5.0	20.0	N750 ± 500	150	GKRP20066
7.0	30.0	N750 ± 500	150	GKRP30066

Carrier and reel specifications on page 11.



All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.

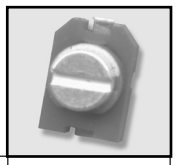
GKYB ECONOMY SERIES

FEATURES

- Suitable for reflow soldering.
- Superior Setting Drift Performance
- Low Mounting Profile (only 1.7 mm)
- Available in carrier and reel packaging.

SPECIFICATIONS

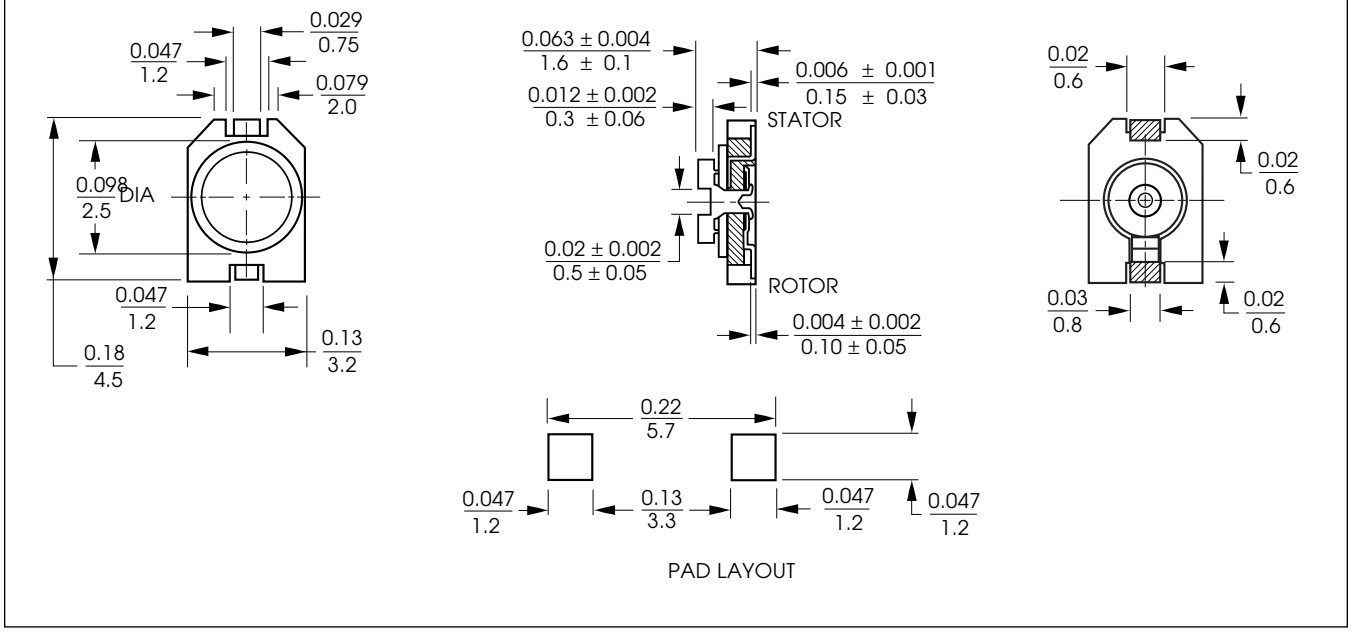
Operating Temperature Range: –25°C to +85°C
Voltage Rating: 100 VDC
Dielectric Withstanding Voltage: 220 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 25 to 100 g-cm (0.35 to 1.39 oz-in)



3.2 x 4.5 x 1.7mm Models

Capacitance Range (pF)		TCC (ppm/°C)	Q min (1 MHz)	Color Code or Mark	Model No.
min	max				
1.7	3.0	NP0 ± 300	300	Brown	GKYB3R066
2.5	6.0	NP0 ± 300	500	Blue	GKYB6R066
3.5	10.0	N750 ± 300	500	White	GKYB10066
5.5	20.0	N1200 ± 500	300	Red	GKYB20066
7.5	30.0	N1200 ± 500	300	Green	GKYB30066

Carrier and reel specifications on page 11.



All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.04 / 0.1.

SURFTRIM® SURFACE MOUNT

GKY WASHABLE SERIES

FEATURES

- Designed for reflow soldering.
- Carrier and reel packaging.
- Sealed for washability

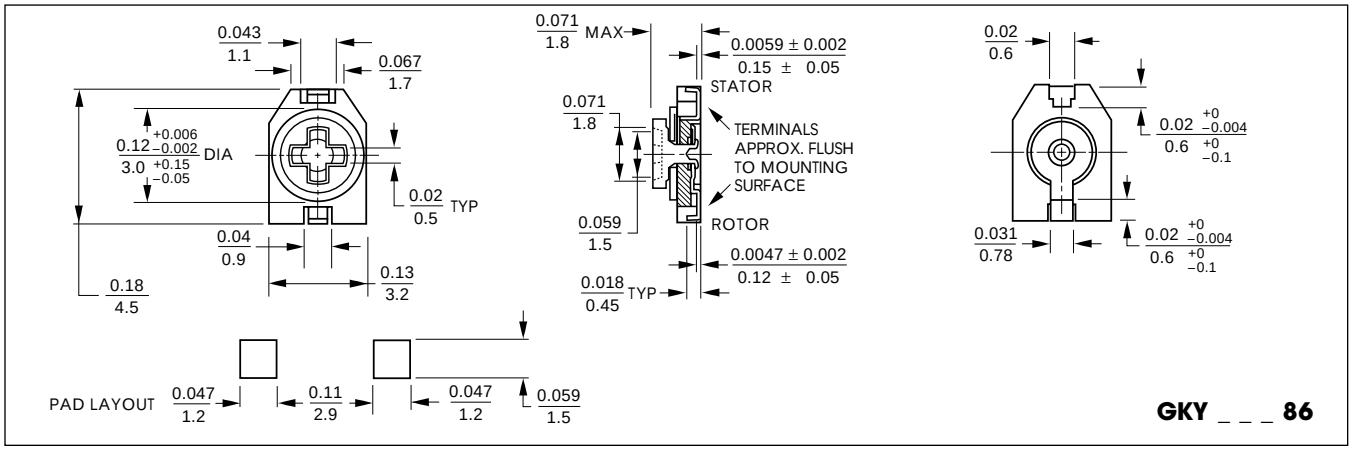
SPECIFICATIONS

Operating Temperature Range: –40°C to +85°C
Voltage Rating: 25 VDC
Dielectric Withstanding Voltage: 75 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 10 to 150 g-cm (0.14 to 2.08 oz-in)

3.2 x 4.5 x 1.8 mm Models

Capacitance (pF)		TCC (ppm / °C)	Q min (1 MHz)	Carrier and Reel Pack Model No.
min	max			
1.0	3.0	0 ± 500	300	GKY3R086
2.5	10.0	0 ± 300	300	GKY10086
4.5	20.0	N750 ± 400	300	GKY20086
4.5	30.0	N750 ± 500	300	GKY30086
4.5	40.0	N750 ± 500	300	GKY40086
4.5	50.0	N750 ± 500	300	GKY50086

Carrier and reel specifications on page 11.



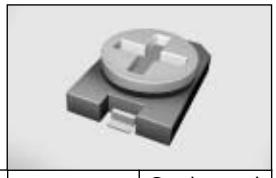
GKY STANDARD SERIES

FEATURES

- Designed for reflow soldering.
- Available in carrier and reel packaging.

SPECIFICATIONS

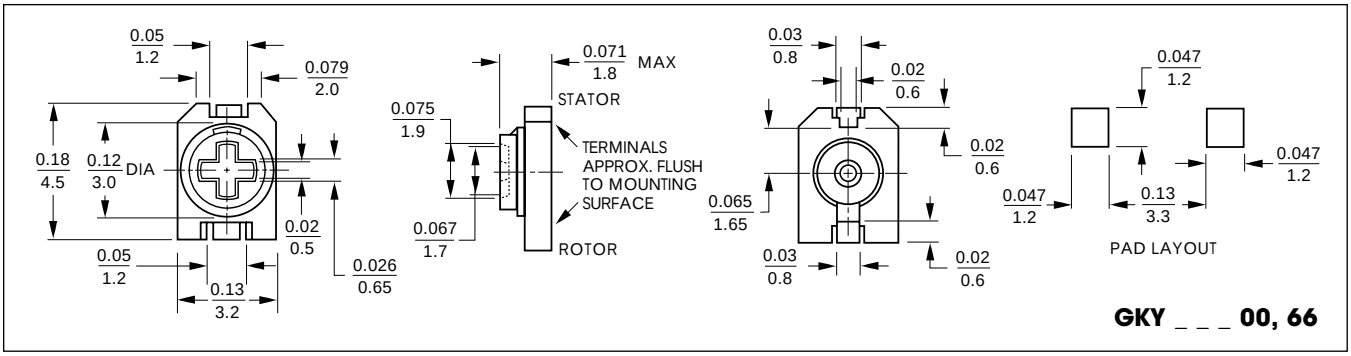
Operating
Temperature Range: –25°C to +85°C
Voltage Rating: 100 VDC
Dielectric Withstanding Voltage: 220 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 10 to 150 g-cm (0.14 to 2.08 oz-in)



3.2 x 4.5 x 1.8 mm Models

Capacitance (pF)		TCC (ppm / °C)	Q min (1 MHz)	Color Code	Bulk Pack Model No.	Carrier and Reel Pack Model No.
min	max					
1.7	3.0	0 ± 300	500	Brown	GKY3R000	GKY3R066
2.5	6.0	0 ± 300	500	Blue	GKY6R000	GKY6R066
3.0	10.0	N400 ± 400	500	White	GKY10000	GKY10066
5.0	20.0	N900 ± 400	300	Red	GKY20000	GKY20066
6.0	30.0	N1200 ± 500	300	Green	GKY30000	GKY30066

Carrier and reel specifications on page 11.



All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.

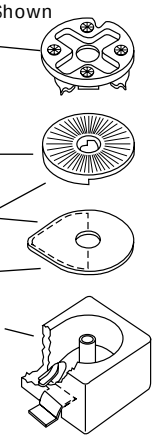
SURFTRIM® SURFACE MOUNT
Sealed Construction

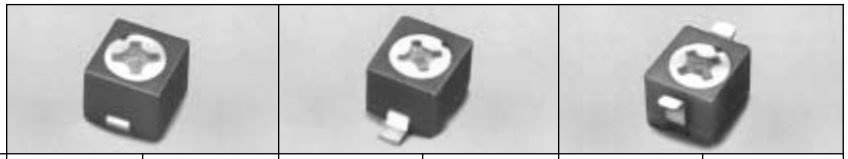
FEATURES
- Process seal provides protection against contaminants (flux, solvents, etc.) during production.
- Designed for flow and reflow soldering.
- Available in carrier and reel packaging.

SPECIFICATIONS
Operating Temperature Range: –25°C to +85°C
Voltage Rating: 100 VDC
Dielectric Withstanding Voltage: 220 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 15 to 100 g-cm (0.2 to 1.39 oz-in)

CONSTRUCTION DETAILS OF 4 x 4.5 mm GKG MODELS
Model GKG _ _ _ _ 27 Shown

- Special "drive assembly" with pointed spring fingers to engage rotor upper surface contour. Spring fingers also provide proper tension for smooth torque and low resistance.
- Special rotor with die-formed "drive" contour on upper surface.
- Flat-lapped and lubricated surfaces join for reliable capacitance settings.
- Special ceramic stator insert with metalized electrode.
- Solid one-piece housing with integrally molded terminals and contact areas. Central tubular column is spun-out into a flare after assembly to maintain built-in spring tension.



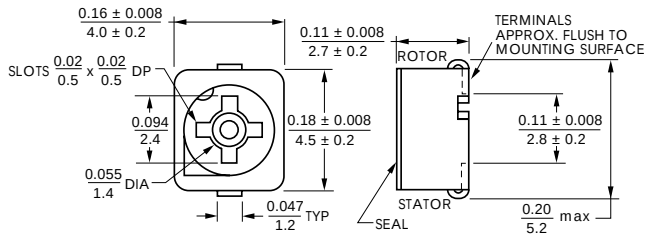


4 x 4.5 x 2.7 mm Models

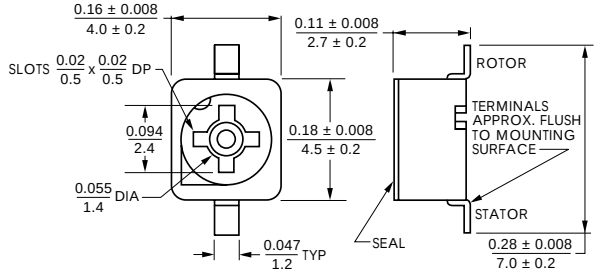
Capacitance (pF)		TCC	Q min	Color	Bulk Pack	Carrier and Reel Pack	Bulk Pack	Carrier and Reel Pack	Bulk Pack	Carrier and Reel Pack
*min	max	(ppm/°C)	(1 MHz)	Code	Model No.	Model No.	Model No.	Model No.	Model No.	Model No.
1.4	3.0	0 ± 200	300**	†Red Dot	GKG3R026	GKG3R066	GKG3R027	GKG3R067	GKG3R028	GKG3R068
2.0	6.0	0 ± 200	500**	Blue	GKG6R026	GKG6R066	GKG6R027	GKG6R067	GKG6R028	GKG6R068
3.0	10.0	0 ± 300	500**	White	GKG10026	GKG10066	GKG10027	GKG10067	GKG10028	GKG10068
4.5	20.0	N900 ± 300	500**	Red	GKG20026	GKG20066	GKG20027	GKG20067	GKG20028	GKG20068
6.5	30.0	N1100 ± 450	300	Green	GKG30026	GKG30066	GKG30027	GKG30067	GKG30028	GKG30068
15.0	50.0	N1700 ± 500	300	Orange	GKG50H26	GKG50H66	GKG50H27	GKG50H67	GKG50H28	GKG50H68

† Marking on bottom of capacitor.
* Re-rated in 1994 for lower min capacitance.
** Q at 10 MHz

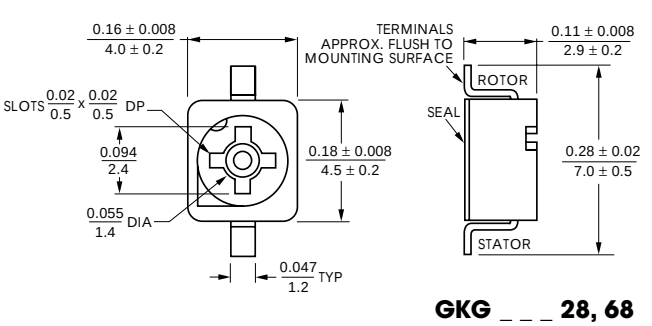
Available without seal — consult factory.
Carrier and reel specifications on page 11.
Add –07 to Model No. for 700/reel, –25 for 2500/reel.



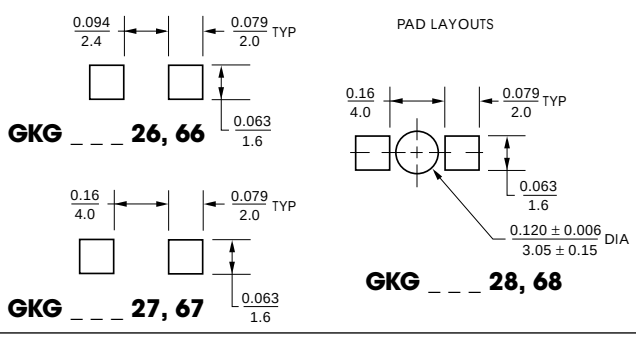
GKG _ _ _ 26, 66



GKG _ _ _ 27, 67



GKG _ _ _ 28, 68



All dimensions are in/mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004/0.1.

PLASTIC ENCASED TYPE

Available With or Without Adjust Cavity Seal

FEATURES

- Very low cost due to automated production and solderless touch contact construction.
- Wide selection of capacitance ranges.
- Color coded housings.
- Easy blind tuning (2 slots at 90° angle in adjust cavity — accepts cross-slotted tool).
- Process seal on adjust screw access face (optional) provides protection against contaminants (flux, cleaning agents, etc.) during production.

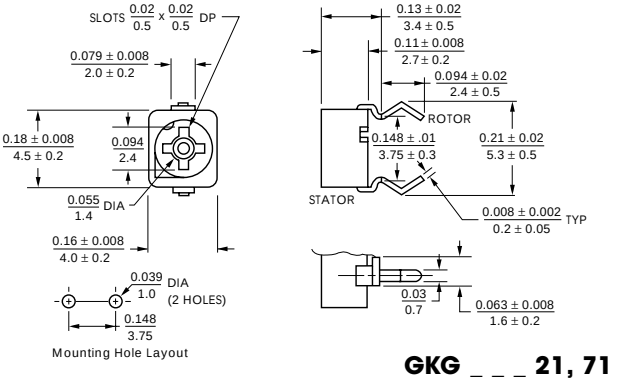
SPECIFICATIONS

Operating Temperature Range: –25°C to +85°C
Voltage Rating: 100 VDC
Dielectric Withstanding Voltage: 220 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 10 to 100 g-cm (0.14 to 1.39 oz-in)

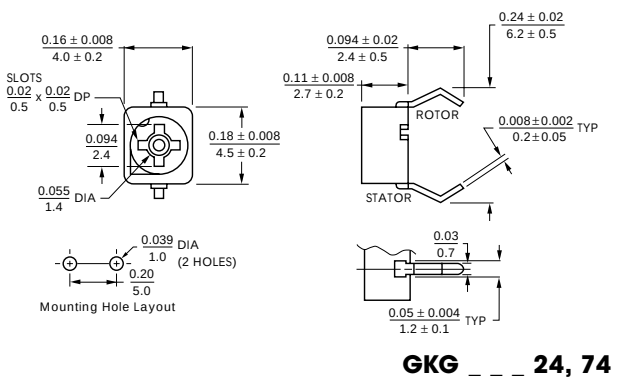
4 x 4.5 mm Models

Capacitance (pF)		TCC	Q min		Color	Top Mount[3] Spring Lead Model No.		Top Mount[3] Spring Lead Model No.		Top Mount[4] Ammo Pack Model No.
[1]min	max	(ppm / °C)	1 MHz	10 MHz	Code	Unsealed	Sealed	Unsealed	Sealed	Unsealed
1.4	3.0	0 ± 200	300	300	[2]Red Dot	GKG3R021	GKG3R071	GKG3R024	GKG3R074	GKG3R025
2.0	6.0	0 ± 200	500	300	Blue	GKG6R021	GKG6R071	GKG6R024	GKG6R074	GKG6R025
3.0	10.0	0 ± 300	500	300	White	GKG10021	GKG10071	GKG10024	GKG10074	GKG10025
4.5	20.0	N900 ± 350	500	300	Red	GKG20021	GKG20071	GKG20024	GKG20074	GKG20025
6.5	30.0	N1100 ± 450	300	300	Green	GKG30021	GKG30071	GKG30024	GKG30074	GKG30025
15.0	50.0	N1700 ± 500	300	N.A.	Orange	GKG50021	GKG50071	GKG50024	GKG50074	GKG50025

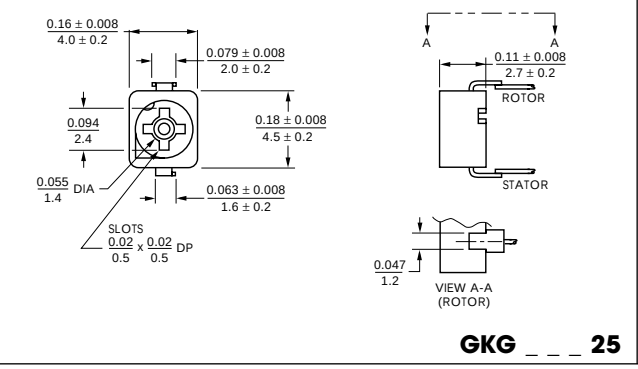
[1]Re-rated in 1993.
[2]Marking on bottom of capacitor.
[3]Magazine pack (120 pieces) for auto insertion available — consult factory for pricing.
[4]Ammo pack contains 1000 pcs.



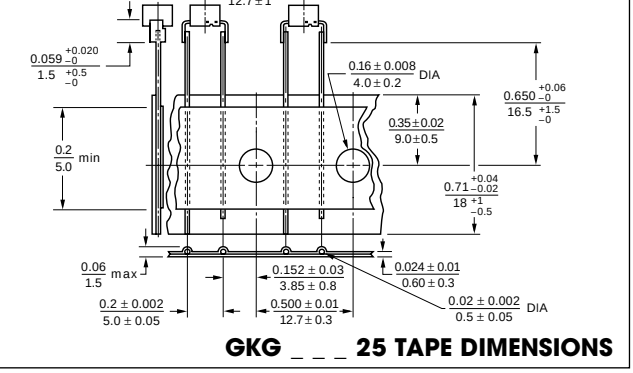
GKG _ _ _ 21, 71



GKG _ _ _ 24, 74



GKG _ _ _ 25



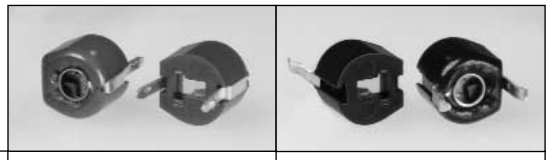
GKG _ _ _ 25 TAPE DIMENSIONS

All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.

PLASTIC ENCASED TYPE
GKG SERIES

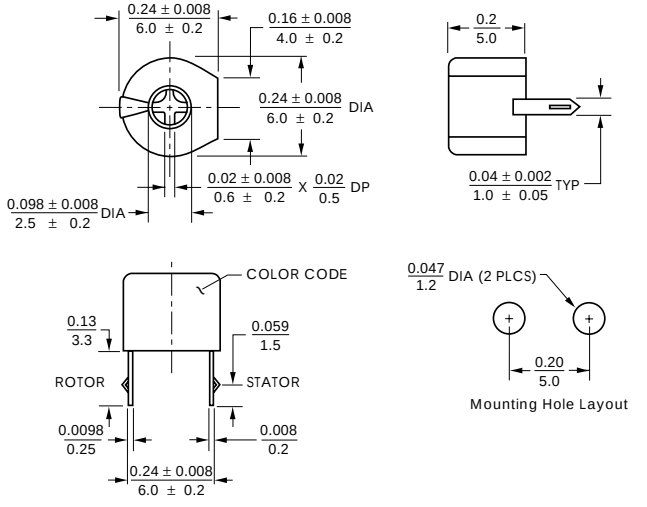
FEATURES
- Very low cost.
- Wide selection of capacitance ranges.
- Suitable for printed circuit production methods using “spring leads” or “straight leads”.

SPECIFICATIONS
Operating Temperature Range: –25°C to +85°C
Voltage Rating: 100 VDC
Dielectric Withstanding Voltage: 220 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 15 to 150 g-cm (0.21 to 2.1 oz-in)

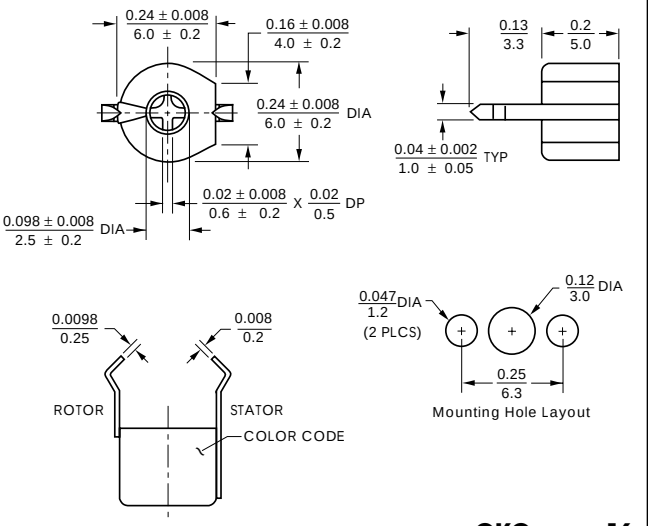


6 mm Economy Models

Capacitance (pF) min	Capacitance (pF) max	TCC (ppm / °C)	Q min (1 MHz)	Color Code	Top Adjust Model No.	Bottom Adjust Model No.
1.0	3.0	NPO ± 250	300	Black	GKG3R015	GKG3R016
2.0	5.0	NPO ± 250	300	Blue	GKG5R015	GKG5R016
3.0	10.0	NPO ± 250	300	White	GKG10015	GKG10016
5.0	20.0	N750 ± 250	300	Red	GKG20015	GKG20016
6.5	30.0	N1000 ± 500	200	Green	GKG30015	GKG30016
7.0	40.0	N2200 ± 800	200	Yellow	GKG40015	GKG40016
10.0	50.0	N2200 ± 800	200	Brown	GKG50015	GKG50016
12.0	60.0	N2200 ± 800	200	Brown	GKG60015	GKG60016
15.0	70.0	N2200 ± 800	200	Brown	GKG70015	GKG70016
18.0	90.0	N2200 ± 800	150	Brown	GKG90015	GKG90016



GKG _ _ _ 15



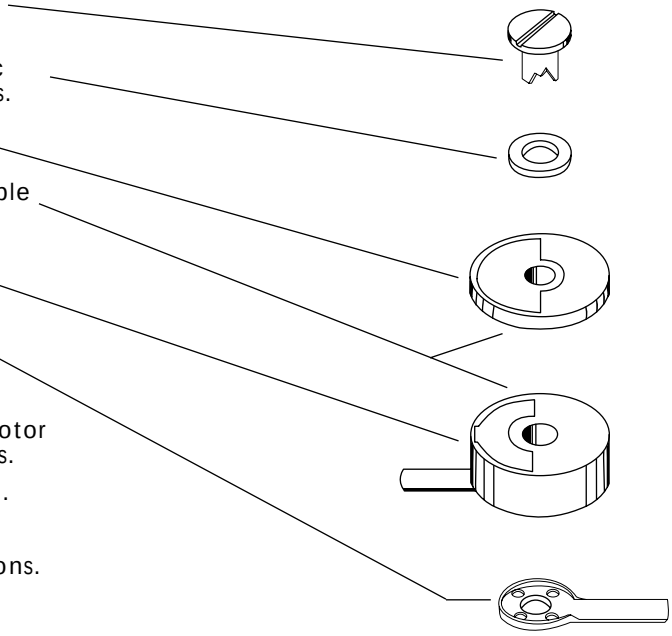
GKG _ _ _ 16

All dimensions are in / mm.
Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1; except slot tolerance is ± 0.008 / 0.2.

RUGGED 5 mm
GKU SERIES

FEATURES

- Proven rugged axle design prevents electrode shifting, maximizes stability.
- Plastic washer between adjust shaft and ceramic rotor to absorb tuning and environmental stresses.
- Special ceramic dielectric rotor with metalized electrode.
- Flat-lapped and lubricated surfaces join for reliable capacity settings.
- Solid one-piece stator electrode and terminal, recessed and integral with base. Cannot shift. Improves stability and resistance to humidity.
- Combination spring/contact/terminal maintains proper tension for smooth torque and low resistance.
- Soldered connection between adjust shaft and rotor electrode eliminates contact resistance problems.
- Compact form factor conserves mounting space.
- Straight line capacitance curve.
- Low cost for industrial and commercial applications.



SPECIFICATIONS

Operating Temperature Range: –55°C to +125°C

Voltage Rating: 250 VDC at 85°C
125 VDC at 125°C

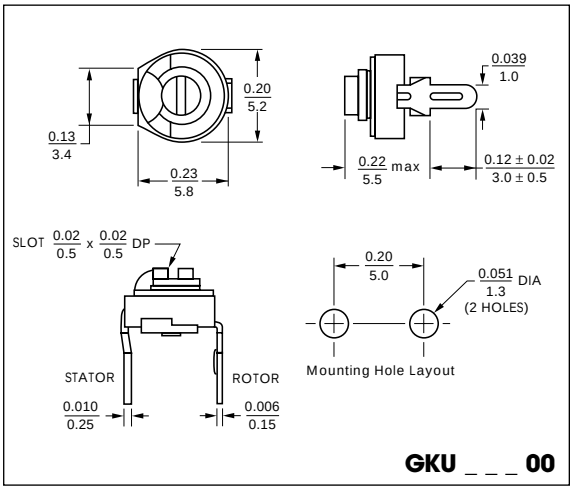
Dielectric
Withstanding Voltage: 500 VDC at 85°C
250 VDC at 125°C

Insulation Resistance: 10^4 Megohms min

Torque: 30 to 140 g-cm (0.42 to 1.94 oz-in)

5 mm Rugged Models

Capacitance Range (pF) min	Capacitance Range (pF) max	TCC (ppm / °C)	Q min (10 MHz)	Color Code or Mark	Model No.
1.5	† 5.5	0 ± 250	300	Black	GKU4R000
2.0	† 8.0	N100 ± 200	300	Red	GKU6R000
2.8	† 12.0	N600 ± 300	300	None	GKU10000
3.3	†† 20.5	N800 ± 300	300	Blue	GKU18000
3.8	† 28.5	N1350 ± 650	200	Purple	GKU25000
4.5	30.0	N1350 ± 650	200	Orange	GKU30000
5.0	40.0	N1600 ± 800	200	Brown	GKU40000
6.0	50.0	N1300 ± 500	150 (1MHz)	Green	GKU50000
7.0	60.0	N1300 ± 500	150 (1MHz)	Pink	GKU60000
15.0	90.0	N1500 ± 800	100 (1MHz)	None	GKU90000



† Re-rated in 1992 †† Re-rated in 1986

All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.

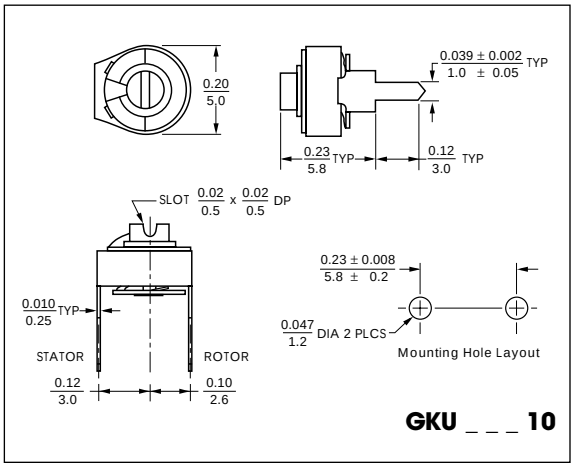
ECONOMY 5 mm
GKU SERIES

FEATURES
- Economical for consumer and industrial applications.
- Rotor soldered to tuning axle for stability.
- For lead-through-hole connection to printed circuit boards.

SPECIFICATIONS
Operating Temperature Range: –25°C to +85°C
Voltage Rating: 250 VDC
Dielectric Withstanding Voltages: 500 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 35 to 200 g-cm (0.49 to 2.8 oz-in)

5 mm Economy Models

Capacitance Range (pF)				
min	max	TCC (ppm / °C)	Q min (1 MHz)	Model No.
1.0	3.0	0 ± 250	300	GKU3R010
2.0	6.0	0 ± 250	300	GKU6R010
3.0	10.0	N750 ± 250	300	GKU10010
4.8	20.0	N750 ± 250	300	GKU20010
5.5	30.0	N1000 ± 250	200	GKU30010
6.8	40.0	N2200 ± 800	200	GKU40010
9.8	50.0	N2200 ± 800	200	GKU50010
12.0	60.0	N2200 ± 800	200	GKU60010
14.0	70.0	N2200 ± 800	200	GKU70010



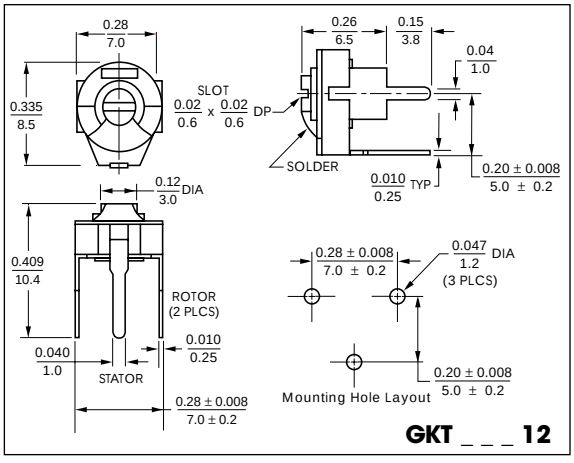
ECONOMY 7 mm
GKT SERIES

FEATURES
- Economical for consumer and industrial applications.
- Rotor soldered to tuning axle for stability.
- For lead-through-hole connection to printed circuit boards.
- Three hole mounting pattern.

SPECIFICATIONS
Operating Temperature Range: –25°C to +85°C
Voltage Rating: 250 VDC
Dielectric Withstanding Voltages: 500 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 32 to 200 g-cm (0.45 to 2.8 oz-in)

7 mm Economy Models

Capacitance Range (pF)				
min	max	TCC (ppm / °C)	Q min (1 MHz)	Model No.
2.0	5.0	0 ± 200	300	GKT5R012
2.5	10.0	0 ± 200	300	GKT10012
3.0	20.0	N470 ± 200	300	GKT20012
4.5	30.0	N550 ± 800	300	GKT30012
6.0	50.0	N1400 ± 800	200	GKT50012
8.5	63.0	N2200 ± 250	200	GKT60012
10.5	81.0	N2200 ± 250	200	GKT80012
12.0	90.0	N2200 ± 250	200	GKT90012



All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.

THIN 2 mm & 3 mm TYPES

FEATURES

- Very small size — for hybrid circuit applications.
- Straight line capacitance curve.
- Choice of mounting styles.

SPECIFICATIONS

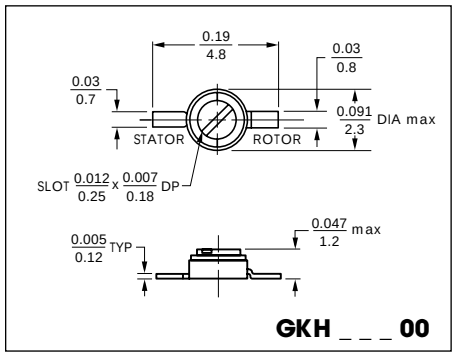
Operating Temperature Range: –25°C to +85°C
Voltage Rating: 25 VDC
Dielectric Withstanding Voltages: 75 VDC
Insulation Resistance: 10^4 Megohms min
Torque: 10 to 75 g-cm (0.14 to 1.0 oz-in)
Terminal Plating: Silver

MINIATURE SERIES

2.0 x 1.2 mm Models

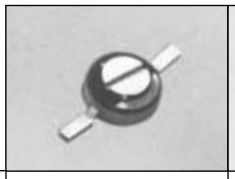
Capacitance (pF) min*	Capacitance (pF) max	TCC (ppm / °C)	Q min (1 MHz)	Model No.
5.0	25.0	N1200 ± 800	100	GKH25000

*Re-rated in 1996

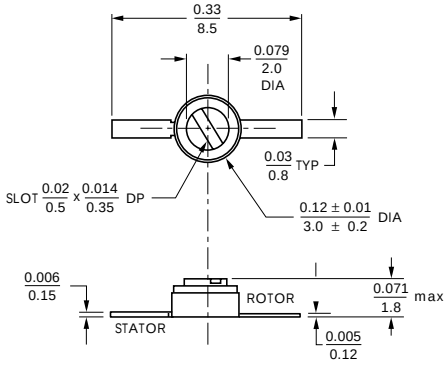


GKH _ _ _ 00

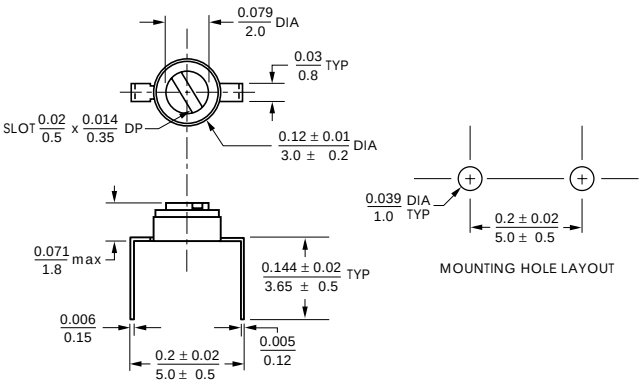
3.0 x 1.8 mm Models



Capacitance (pF) min	Capacitance (pF) max	TCC (ppm / °C)	Q min (1 MHz)	Model No.	Model No.
1.0	3.0	0 ± 300	200	GKX3R010	GKX3R011
1.5	5.0	0 ± 300	200	GKX5R010	GKX5R011
2.5	10.0	0 ± 300	200	GKX10010	GKX10011
5.0	20.0	N750 ± 500	200	GKX20010	GKX20011
5.0	30.0	N750 ± 500	200	GKX30010	GKX30011
5.0	35.0	N750 ± 500	200	GKX35010	GKX35011
6.0	40.0	N750 ± 500	200	GKX40010	GKX40011



GKX _ _ _ 10



GKX _ _ _ 11

All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.

CARRIER AND REEL SPECIFICATIONS

CARRIER

Product Line \ Dimension / Tolerance		A ±0.004 / 0.1	B ±0.004 / 0.1	C ±0.01 / 0.3	D ±0.004 / 0.1	E ±0.004 / 0.1	F ±0.004 / 0.1	G ±0.004 / 0.1	H ±0.004 / 0.1	K ±0.008 / 0.2	L ±0.002 / 0.05	M +0.004 / 0.1 − 0	N ±0.004 / 0.1	P ±0.004 / 0.1
GKG_ _ _ 66	Fig. 2	0.18 / 4.5	0.21 / 5.4	0.47 / 12	0.22 / 5.5	0.069 / 1.75	0.31 / 8.0	0.08 / 2.0	0.2 / 4	0.13 / 3.2	0.01 / 0.3	0.059 / 1.5	—	—
GKG_ _ _ 67, 68	Fig. 1	0.18 / 4.5	0.30 / 7.5	0.47 / 12	0.22 / 5.5	0.069 / 1.75	0.31 / 8.0	0.08 / 2.0	0.2 / 4	0.13 / 3.2	0.01 / 0.3	0.059 / 1.5	0.08 / 2.0	0.2 / 5
GKRP_ _ _ 66	Fig. 2	0.11 / 2.7	0.13 / 3.2	0.47 / 12	0.22 / 5.5	0.069 / 1.75	0.16 / 4.0	0.08 / 2.0	0.2 / 4	0.075 / 1.9	0.01 / 0.3	0.059 / 1.5	—	—
GKY_ _ _ 66, GKYA	Fig. 2	0.14 / 3.6	0.19 / 4.9	0.47 / 12	0.22 / 5.5	0.069 / 1.75	0.31 / 8.0	0.08 / 2.0	0.2 / 4	0.091 / 2.3	0.01 / 0.3	0.059 / 1.5	—	—
GKY_ _ _ 86	Fig. 2	0.132 / 3.35	0.185 / 4.70	0.47 / 12	0.22 / 5.5	0.069 / 1.75	0.31 / 8.0	0.08 / 2.0	0.2 / 4	0.091 / 2.4	0.01 / 0.3	0.059 / 1.5	—	—

All dimensions are in/ mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.
GKG and GKY_ _ _66 series capacitors are positioned in compartments (blisters) with the stator terminal closer to the "M" holes. To get the parts with the rotor terminal closer to the "M" holes, add an "A" suffix to the model number.
GKRP and GKY_ _ _86 series capacitors are positioned in compartments (blisters) with the rotor terminal closer to the "M" holes. To get the parts with the stator terminal closer to the "M" holes, add an "A" suffix to the model number.

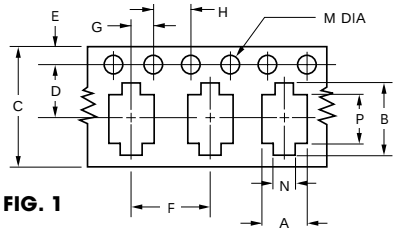


FIG. 1

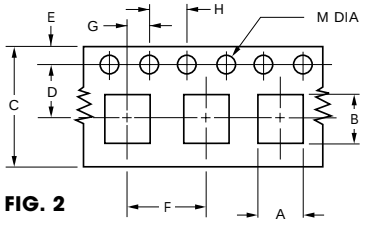
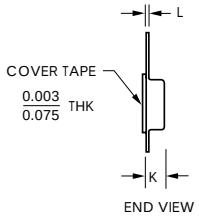
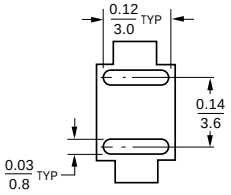


FIG. 2

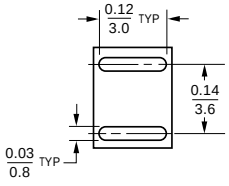


END VIEW

Embossment Details



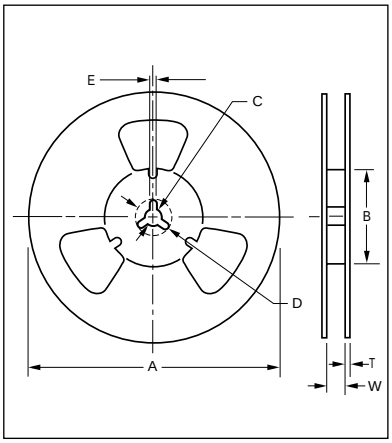
GKG _ _ _ 67, 68



GKG _ _ _ 66

REEL

Product Line \ Dimension / Tolerance	Quantity Per Reel	A ±0.1 / 3	B ±0.1 / 3	C ±0.04 / 1	D ±0.08 / 2	E ±0.04 / 1	T ±0.02 / 0.5	W ±0.08 / 2
GKG_ _ _ 66-07, 67-07, 68-07	700	7.09 / 180	2.4 / 60	0.51 / 13	0.91 / 23	0.08 / 2	0.043 / 1.1	0.531 / 13.5
GKG_ _ _ 66-25, 67-25, 68-25	2500	13.0 / 330	3.1 / 80	0.51 / 13	0.91 / 23	0.098 / 2.5	0.079 / 2.0	0.531 / 13.5
GKRP_ _ _ 66	2000	7.09 / 180	2.4 / 60	0.51 / 13	0.83 / 21	0.08 / 2	0.047 / 1.2	0.512 / 13.0
GKY_ _ _ 66, GKYA	1000	7.09 / 180	2.4 / 60	0.51 / 13	0.91 / 23	0.08 / 2	0.043 / 1.1	0.531 / 13.5
GKY_ _ _ 86	1000	7.09 / 180	2.4 / 60	0.51 / 13	0.83 / 21	0.08 / 2	0.047 / 1.2	0.512 / 13.0



All dimensions are in / mm. Unless otherwise specified, the tolerance on dimensions is ± 0.004 / 0.1.

SPECIFICATION NOTES

1. Parts are 100% tested for capacitance range, dielectric withstanding voltage, insulation resistance, and torque.
2. Capacitance range specified is that which is guaranteed, and is measured at 1 MHz and 25°C.
3. For soldering SURFTRIM® surface mounting models, pre-heat at 140°C ±10°C for 2 minutes maximum, and reflow solder at 240°C ±5°C for 20 seconds maximum.
4. For soldering printed circuit board mounting models, solder at 260°C ±10°C for 5 seconds maximum, except 3 seconds maximum for Miniature Models (page 10).
5. Q factor is measured at maximum rated capacitance and at room temperature. Frequency of measurement is as listed for each model.
6. Dielectric strength is measured at maximum rated capacitance and room temperature, with test voltage as listed for each model applied for 5 seconds.
7. Insulation resistance is measured at maximum rated capacitance and room temperature and at rated voltage, unless otherwise specified.
8. Temperature coefficient of capacitance (TCC) is measured at 100 kHz or 1 MHz, over a temperature range of –20°C to +70°C with capacitor set at maximum rated capacitance.
9. Axial load during tuning should not exceed 250 grams.
10. Capacitors should not be operated outside of rated capacitance range and working voltage.
11. Angular orientation of adjusting slot is random.

APPLICATION NOTES

Soldering and Cleaning of Ceramic Trimmer Capacitors

Soldering temperatures and times are specified in Notes 3 and 4 above. If using an iron for manual soldering (for prototyping or repairs, for example) use an appropriate size and temperature so that the high temperature exposure of the trimmer is less than 3 seconds.

We strongly recommend the use of water soluble fluxes for soldering, followed by cleaning in water containing detergents, and then a clear water rinse.

Some operations still use Freon or similar fluorinated or chlorinated hydrocarbon solvents. These solvents have a tendency to remove the lubricant, which in turn makes for bumpy adjustment, and will degrade the tuning torque, adjustment life, and other mechanical specifications.

In general, the minimum exposure to cleaning solutions is recommended. The gentlest would be the detergent and water rinses at fairly low temperatures. When chlorinated or fluorinated hydrocarbons are used, the boards should never be plunged into the solvent solution, but rather maintained in the vapor area of the defluxing equipment, and for the minimum possible time. Most desirable would be to clean only the bottom of the printed circuit board, as with board scrubbers.

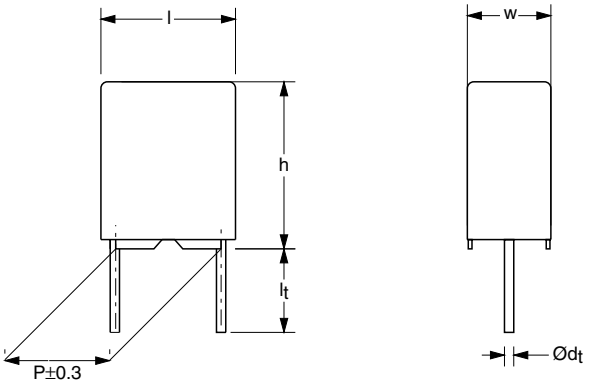
The unsealed GKG models are usually specified for consumer applications where cleaning after soldering is normally not required. Should cleaning be required, the method to use would be to clean the bottom of the board, as with board scrubbers. If a solvent is used when cleaning the GKG series, sealed versions should be specified to prevent the solvent from being trapped in the housing and degrading performance.

Other precautions for using ceramic trimmer capacitors include:

- Beware of excessive handling with bare hands as, “finger oil” and dirt can bring down Q and insulation resistance values.
- Terminals should not be cut or reformed, as this could cause deformation of the spring or breaking of the rotor.

Sprague-Goodman Electronics, Inc.
1700 SHAMES DRIVE, WESTBURY, NY 11590
TEL: 516-334-8700 • FAX: 516-334-8771
E-MAIL: info@spraguegoodman.com
WEBSITE: http://www.spraguegoodman.com

Metallized Polypropylene Film Capacitors
MKP Radial Potted Type



Dimensions in mm

APPLICATIONS

Low losses due to low contact resistance and low loss dielectric result in applications where high frequency occur or high stability is preferred. Their small dimensions make them suitable for circuits with high packaging density.

MARKING

C-value; rated voltage; tolerance; code for manufacturer; year and week of manufacture; manufacturers type designation

DIELECTRIC

Polypropylene film

ELECTRODES

Vacuum deposited aluminum

ENCAPSULATION

Flame retardant plastic case and epoxy resin (UL-class 94 V-0)

CONSTRUCTION

Wound mono construction

LEADS

Tinned wire

CAPACITANCE RANGE (E24 SERIES)

0.001 to 1.2 µF

FEATURES

5, 10 and 15 mm lead pitch. Supplied loose in box, in ammopack and taped on reel. Intermediate values are available of the E96 series

Lead (Pb)-free product

RoHS-compliant product

Pb-free

e3

RoHS COMPLIANT

CAPACITANCE TOLERANCE

± 5 %; ± 2 %

RATED (DC) VOLTAGE

63 V; 160 V; 250 V; 400 V; 630 V

RATED (AC) VOLTAGE

25 V; 63 V;100 V; 125 V; 160 V

RATED PEAK-TO-PEAK VOLTAGE

70 V; 180 V; 280 V; 350 V; 450 V

CLIMATIC CATEGORY

55/085/56

RATED TEMPERATURE (DC)

85 °C

RATED TEMPERATURE (AC)

85 °C

MAXIMUM APPLICATION TEMPERATURE

85 °C

REFERENCE SPECIFICATIONS

IEC 60384-16

PERFORMANCE GRADE

Grade 1 (long life)

STABILITY GRADE

Grade 1

DETAIL SPECIFICATION

For more detailed data and test requirements contact: filmcaps.roeselare@vishay.com

COMPOSITION OF CATALOG NUMBER

TYPE AND PITCHES	
416	5.0/10.0/15.0 mm
417	5.0/10.0/15.0 mm
418	5.0/10.0/15.0 mm
419	5.0/10.0/15.0 mm
420	5.0/10.0/15.0 mm

CAPACITANCE (numerically)

MULTIPLIER (nF)	
0.01	2
0.1	3
1	4

Example:
1004 = 100 x 1 = 100 nF

2222	4..	XX	XX	X
BFC2*	4..	XX	XX	X

* Use this partnumber for those with access to the Vishay's SAP system and Partners website within the Americas

TYPE	PACKAGING	PITCH (mm)	LEAD CONFIGURATION	PREFERRED TYPES					
				C-TOL	63 V	160 V	250 V	400 V	630 V
416	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %	1				
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %	7				
417	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %		1			
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %		7			
418	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %			1		
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %			7		
419	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %				1	
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %				7	
420	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 2 %					1
	Loose in box	15	lead length 3.5 ± 0.3 mm	± 2 %					7
					ON REQUEST				
416	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %	0				
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %	3				
				± 2 %	4				
		15	lead length 3.5 ± 0.3 mm	± 5 %	6				
417	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %		0			
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %		3			
				± 2 %		4			
		15	lead length 3.5 ± 0.3 mm	± 5 %		6			
418	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %			0		
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %			3		
				± 2 %			4		
		15	lead length 3.5 ± 0.3 mm	± 5 %			6		
419	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %				0	
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %				3	
				± 2 %				4	
		15	lead length 3.5 ± 0.3 mm	± 5 %				6	
420	Taped; see note	5/10/15	H = 18.5 mm; P_0 = 12.7 mm	± 5 %					0
	Loose in box	5/10	lead length 4.0 + 1.0/– 0.5 mm	± 5 %					3
				± 2 %					4
		15	lead length 3.5 ± 0.3 mm	± 5 %					6

Note:
Pitch = 5 and 10 mm: taped on ammopack
Pitch = 15 mm: taped on reel with diameter = 356 mm

SPECIFIC REFERENCE DATA

DESCRIPTION	VALUE				
Tangent of loss angle:	at 10 kHz			at 100 kHz	
$C \leq 0.0091\ \mu F$	$\leq 5 \times 10^{-4}$			$\leq 10 \times 10^{-4}$	
$0.0091\ \mu F < C \leq 0.027\ \mu F$	$\leq 5 \times 10^{-4}$			$\leq 15 \times 10^{-4}$	
$0.027\ \mu F < C \leq 0.075\ \mu F$	$\leq 5 \times 10^{-4}$			$\leq 20 \times 10^{-4}$	
$0.075\ \mu F < C \leq 0.11\ \mu F$	$\leq 5 \times 10^{-4}$			$\leq 25 \times 10^{-4}$	
$0.11\ \mu F < C \leq 0.18\ \mu F$	$\leq 10 \times 10^{-4}$			$\leq 30 \times 10^{-4}$	
$0.18\ \mu F < C \leq 0.27\ \mu F$	$\leq 10 \times 10^{-4}$			$\leq 35 \times 10^{-4}$	
$0.27\ \mu F < C \leq 0.39\ \mu F$	$\leq 10 \times 10^{-4}$			$\leq 40 \times 10^{-4}$	
$0.39\ \mu F < C \leq 0.56\ \mu F$	$\leq 10 \times 10^{-4}$			$\leq 45 \times 10^{-4}$	
$0.56\ \mu F < C \leq 0.75\ \mu F$	$\leq 10 \times 10^{-4}$			$\leq 50 \times 10^{-4}$	
$0.75\ \mu F < C \leq 1.1\ \mu F$	$\leq 10 \times 10^{-4}$			$\leq 60 \times 10^{-4}$	
Rated voltage pulse slope $(dU/dt)_R$:	at 63 V (DC)	at 100 V (DC)	at 250 V (DC)	at 400 V (DC)	at 630 V (DC)
P = 5 mm	50 V/µs	50 V/µs	50 V/µs	50 V/µs	50 V/µs
P = 10 mm	20 V/µs	20 V/µs	20 V/µs	20 V/µs	50 V/µs
P = 15 mm	50 V/µs	50 V/µs	50 V/µs	50 V/µs	50 V/µs
R between leads, for C ≤ 0.33 µF:					
at 50 V; 1 minute	> 100000 MΩ				
at 100 V; 1 minute		> 100000 MΩ	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ
RC between leads, for C > 0.33 µF at 10 V; 1 minute	> 30000 s	>30000 s	>30000 s	>30000 s	
R between interconnecting leads and casing; 50 V; 1 minute	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ	> 100000 MΩ
Withstanding (DC) voltage (cut off current 10 mA); rise time 100 V/s	100 V; 1 minute	260 V; 1 minute	400 V; 1 minute	640 V; 1 minute	1000 V; 1 minute
Withstanding (DC) voltage between leads and case	2840 V; 1 minute	2840 V; 1 minute	2840 V; 1 minute	2840 V; 1 minute	1260 V; 1 minute

U_{Rdc} = 63 V; U_{Rac} = 25 V; U_{p-p} = 70 V

C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 416 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		lt = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		lt = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.036	4.5 × 9.0 × 7.2	0.45	13603	1000	43603	2000				
0.039			13903		43903					
0.043			14303		44303					
0.047			14703		44703					
0.051	6.0 × 11.0 × 7.2	0.60	15103	750	45103	1500				
0.056			15603		45603					
0.062			16203		46203					
0.068			16803		46803					
0.075			17503		47503					
0.082			18203		48203					
0.091			19103		49103					
0.1			11004		41004					
0.11			11104		41104					
0.12			11204		41204					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.13	5.0 × 11.0 × 12.5	0.85	11304	600	41304	1000				
0.15			11504		41504					
0.16	6.0 × 12.0 × 12.5	1.10	11604	500	41604	750				
0.18			11804		41804					
0.20			12004		42004					
0.22			12204		42204					
0.24			12404		42404					
0.27			12704		42704					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.3	6.0 × 12.0 × 17.5	1.4					13004	900	73004	1000
0.33							13304		73304	
0.36							13604		73604	
0.39							13904		73904	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.43	7.0 × 13.5 × 17.5	1.9					14304	800	74304	750
0.47							14704		74704	
0.51							15104		75104	
0.56							15604		75604	
0.62	8.5 × 15.0 × 17.5	2.6					16204	650	76204	750
0.68							16804		76804	
0.75							17504		77504	
0.82							18204		78204	
0.91	10.0 × 16.5 × 17.5	3.1					19104	600	79104	500
1.0							11005		71005	
1.1							11105		71105	

U_{Rdc} = 160 V; U_{Rac} = 63 V; U_{p-p} = 180 V

C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 417 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		lt = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		lt = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.024	4.5 × 9.0 × 7.2	0.45	12403	1000	42403	2000				
0.027			12703		42703					
0.03			13003		43003					
0.033			13303		43303					
0.036	6.0 × 11.0 × 7.2	0.60	13603	750	43603	1500				
0.039			13903		43903					
0.043			14303		44303					
0.047			14703		44703					
0.051			15103		45103					
0.056			15603		45603					
0.062			16203		46203					
0.068			16803		46803					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.075	4.0 × 10.0 × 12.5	0.60	17503	750	47503	1000				
0.082			18203		48203					
0.091			19103		49103					
0.1			11004		41004					
0.11	5.0 × 11.0 × 12.5	0.85	11104	600	41104	1000				
0.12			11204		41204					
0.13			11304		41304					
0.15			11504		41504					
0.16	6.0 × 12.0 × 12.5	1.10	11604	500	41604	750				
0.18			11804		41804					
0.20			12004		42004					
0.22			12204		42204					
0.24			12404		42404					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.27	5.0 × 11.0 × 17.5	1.2					12704	1100	72704	1250
0.3	6.0 × 12.0 × 17.5	1.4					13004	900	73004	1000
0.33							13304		73304	
0.36							13604		73604	
0.39							13904		73904	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.43	7.0 × 13.5 × 17.5	1.9					14304	800	74304	750
0.47							14704		74704	
0.51							15104		75104	
0.56							15604		75604	
0.62	8.5 × 15.0 × 17.5	2.6					16204	650	76204	750
0.68							16804		76804	
0.75							17504		77504	
0.82							18204		78204	
0.91	10.0 × 16.5 × 17.5	3.1					19104	600	79104	500
1.0							11005		71005	
1.1							11105		71105	

U_{Rdc} = 250 V; U_{Rac} = 25 V; U_{p-p} = 70 V

C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 418 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		lt = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		lt = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.01	3.5 × 8.0 × 7.2	0.35	11003	1500	41003	3000				
0.011			11103		41103					
0.012			11203		41203					
0.013			11303		41303					
0.015			11503		41503					
0.016	4.5 × 9.0 × 7.2	0.45	11603	1000	41603	2000				
0.018			11803		41803					
0.02			12003		42003					
0.022			12203		42203					
0.024			12403		42403					
0.027	6.0 × 11.0 × 7.2	0.60	12703	750	42703	1500				
0.03			13003		43003					
0.033			13303		43303					
0.036			13603		43603					
0.039			13903		43903					
0.043			14303		44303					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.047	4.0 × 10.0 × 12.5	0.60	14703	750	44703	1000				
0.051			15103		45103					
0.056			15603		45603					
0.062			16203		46203					
0.068			16803		46803					
0.075	5.0 × 11.0 × 12.5	0.85	17503	600	47503	1000				
0.082			18203		48203					
0.091			19103		49103					
0.1	6.0 × 12.0 × 12.5	1.10	11004	500	41004	750				
0.11			11104		41104					
0.12			11204		41204					
0.13			11304		41304					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.15	5.0 × 11.0 × 17.5	1.2					11504	1100	71504	1250
0.16							11604		71604	
0.18	6.0 × 12.0 × 17.5	1.4					11804	900	71804	1000
0.2							12004		72004	
0.22							12204		72204	
0.24							12404		72404	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.27	7.0 × 13.5 × 17.5	1.9					12704	800	72704	750
0.3							13004		73004	
0.33							13304		73304	
0.36							13604		73604	
0.39	8.5 × 15.0 × 17.5	2.6					13904	650	73904	750
0.43							14304		74304	
0.47							14704		74704	
0.51							15104		75104	
0.56	10.0 × 16.5 × 17.5	3.1					15604	600	75604	500
0.62							16204		76204	
0.68							16804		76804	

U_{Rdc} = 400 V; U_{Rac} = 125 V; U_{p-p} = 350 V

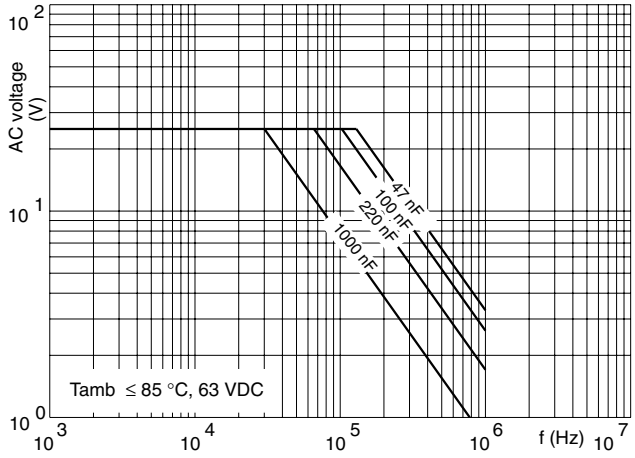
C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 419 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		lt = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		lt = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.001	3.5 × 8.0 × 7.2	0.35	11002	1500	41002	3000				
0.0011			11102		41102					
0.0012			11202		41202					
0.0013			11302		41302					
0.0015			11502		41502					
0.0016			11602		41602					
0.0018			11802		41802					
0.002			12002		42002					
0.0022			12202		42202					
0.0024			12402		42402					
0.0027			12702		42702					
0.003			13002		43002					
0.0033			13302		43302					
0.0036			13602		43602					
0.0039			13902		43902					
0.0043	4.5 × 9.0 × 7.2	0.45	14302	1000	44302	2000				
0.0047			14702		44702					
0.0051			15102		45102					
0.0056			15602		45602					
0.0062			16202		46202					
0.0068			16802		46802					
0.0075			17502		47502					
0.0082			18202		48202					
0.0091			19102		49102					
0.01			11003		41003					
0.011			11103		41103					
0.012			11203		41203					
0.013	6.0 × 11.0 × 7.2	0.60	11303	750	41303	1500				
0.015			11503		41503					
0.016			11603		41603					
0.018			11803		41803					
0.02			12003		42003					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.022	4.0 × 10.0 × 12.5	0.60	12203	750	42203	1000				
0.024			12403		42403					
0.027			12703		42703					
0.03			13003		43003					
0.033			13303		43303					
0.036	5.0 × 11.0 × 12.5	0.85	13603	600	43603	1000				
0.039			13903		43903					
0.043			14303		44303					

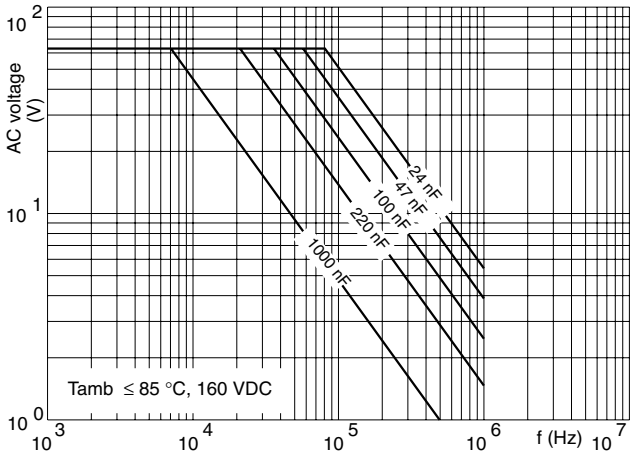
C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 419 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		lt = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		lt = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
0.047	6.0 × 12.0 × 12.5	1.10	14703	500	44703	750				
0.051			15103		45103					
0.056			15603		45603					
0.062			16203		46203					
0.068			16803		46803					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.075	5.0 × 11.0 × 17.5	1.2					17503	1100	77503	1250
0.082							18203		78203	
0.091	6.0 × 12.0 × 17.5	1.4					19103	900	79103	1000
0.1							11004		71004	
0.11							11104		71104	
0.12							11204		71204	
0.13							11304		71304	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.15	7.0 × 13.5 × 17.5	1.9					11504	800	71504	750
0.16							11604		71604	
0.18							11804		71804	
0.2	8.5 × 15.0 × 17.5	2.6					12004	650	72004	750
0.22							12204		72204	
0.24							12404		72404	
0.27							12704		72704	
0.3	10.0 × 16.5 × 17.5	3.1					13004	600	73004	500
0.33							13304		73304	
0.36							13604		73604	

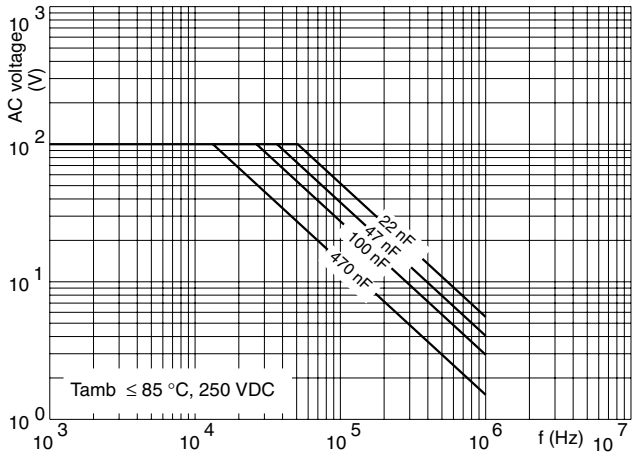
U_{Rdc} = 630 V; U_{Rac} = 160 V; U_{p-p} = 450 V

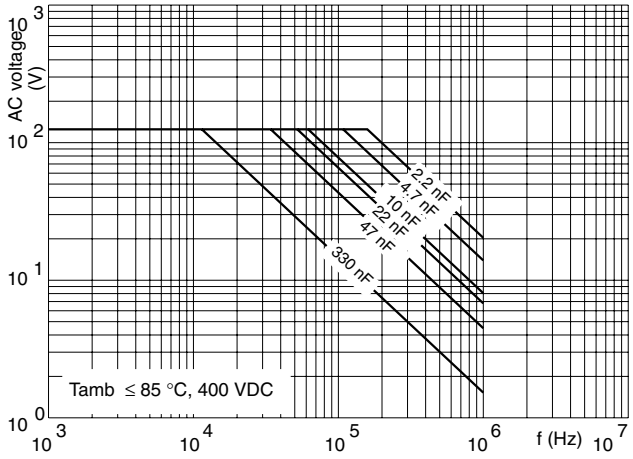
C (E 24) (µF)	DIMENSIONS w × h × l (mm)	MASS (g)	CATALOG NUMBER 2222 420 ..... AND PACKAGING							
			AMMOPACK		LOOSE IN BOX		REEL		LOOSE IN BOX	
			H = 18.5 mm; P_0 = 12.7 mm		lt = 4.0 + 1.0/– 0.5 mm		H = 18.5 mm; P_0 = 12.7 mm		lt = 3.5 ± 0.3 mm	
			C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %		C-tol = ± 2 %	
			last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ	last 5 digits of catalog number	SPQ
Pitch = 5.0 ± 0.3 mm; d_t = 0.50 ± 0.05 mm										
0.0015	3.5 × 8.0 × 7.2	0.35	11502	1500	41502	3000				
0.0016			11602		41602					
0.0018			11802		41802					
0.002			12002		42002					
0.0022			12202		42202					
0.0024			12402		42402					
0.0027			12702		42702					
0.003	4.5 × 9.0 × 7.2	0.45	13002	1000	43002	2000				
0.0033			13302		43302					
0.0036			13602		43602					
0.0039			13902		43902					
0.0043	6.0 × 11.0 × 7.2	0.60	14302	750	44302	1500				
0.0047			14702		44702					
0.0051			15102		45102					
0.0056			15602		45602					
0.0062			16202		46202					
0.0068			16802		46802					
Pitch = 10.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.01	4.0 × 10.0 × 12.5	0.60	11003	750	41003	1000				
0.011			11103		41103					
0.012			11203		41203					
0.013			11303		41303					
0.015			11503		41503					
0.016			11603		41603					
0.018	5.0 × 11.0 × 12.5	0.85	11803	600	41803	1000				
0.02			12003		42003					
0.022			12203		42203					
0.024			12403		42403					
0.027	6.0 × 12.0 × 12.5	1.10	12703	500	42703	750				
0.03			13003		43003					
0.033			13303		43303					
0.036			13603		43603					
0.039			13903		43903					
0.043			14303		44303					
0.047			14703		44703					
Pitch = 15.0 ± 0.4 mm; d_t = 0.60 ± 0.06 mm										
0.051	6.0 × 12.0 × 17.5	1.4					15103	900	75103	1000
0.056							15603		75603	
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm										
0.062	7.0 × 13.5 × 17.5	1.9					16203	800	76203	750
0.068							16803		76803	
0.075							17503		77503	
0.082							18203		78203	
0.091	8.5 × 15.0 × 17.5	2.6					19103	650	79103	750
0.1							11004		71004	
0.11							11104		71104	
0.12							11204		71204	
0.13	10.0 × 16.5 × 17.5	3.1					11304	600	71304	500
0.15							11504		71504	
0.16							11604		71604	

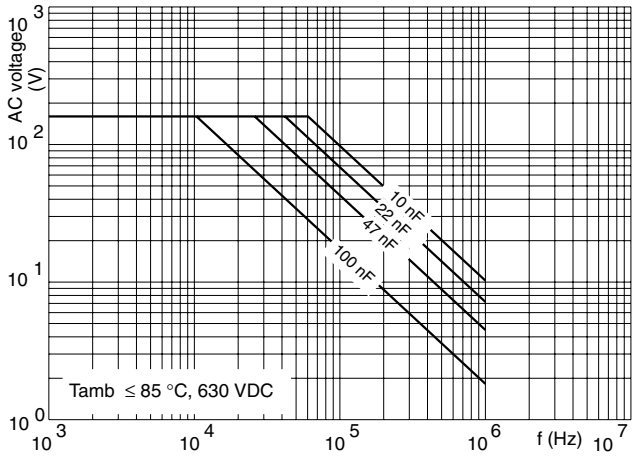
MAXIMUM RMS VOLTAGE (SINEWAVE) AS A FUNCTION OF FREQUENCY



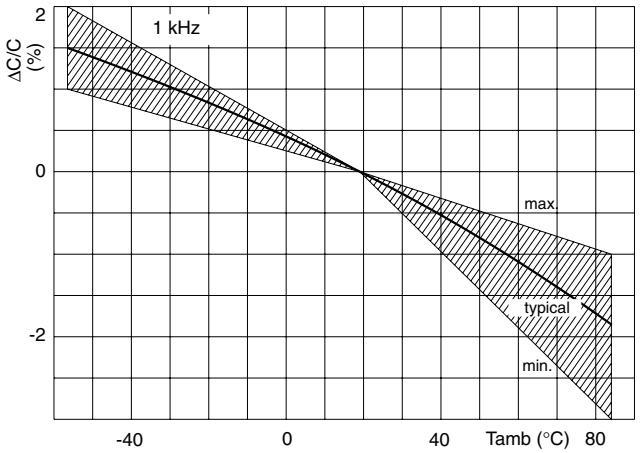




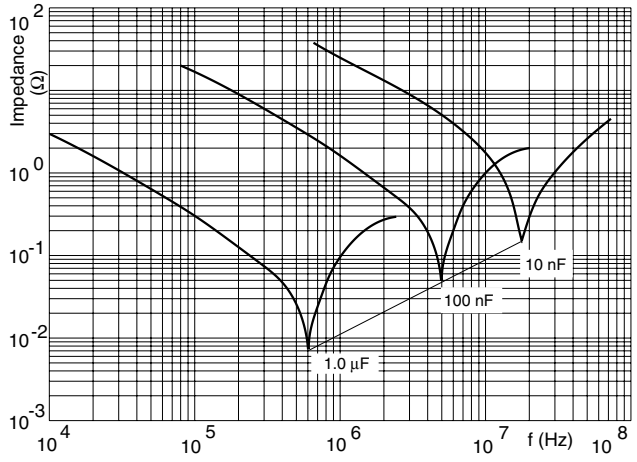




CAPACITANCE



IMPEDANCE



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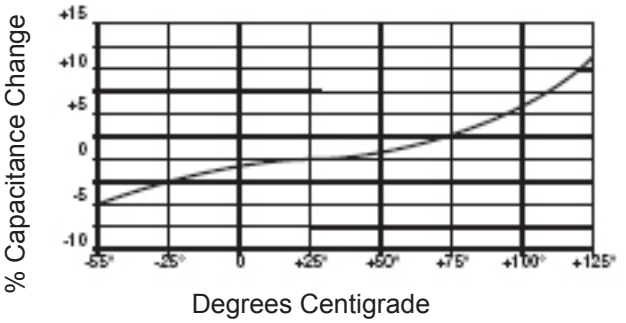
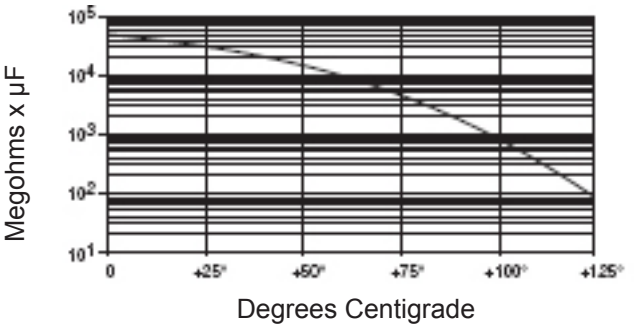
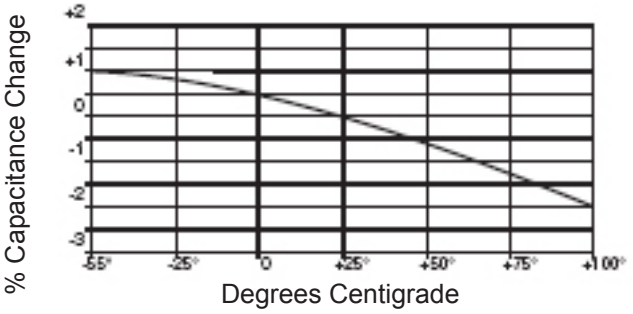
Capacitance Change vs. Temperature Insulation Resistance vs. Temperature

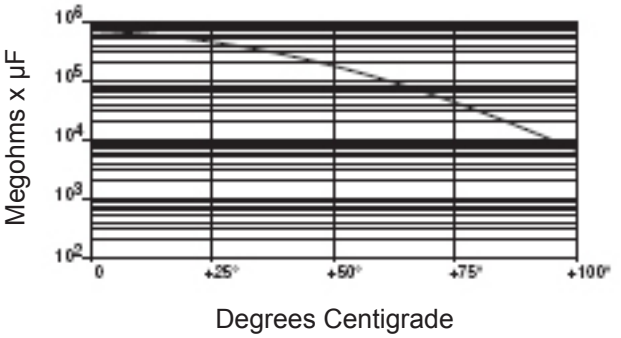
Polyester Typical Characteristics at 1 kHz



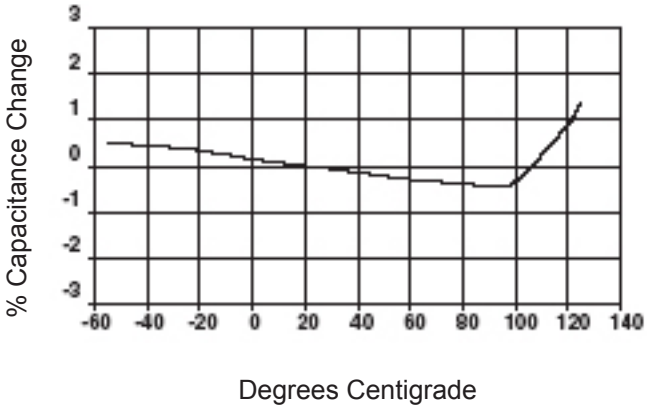


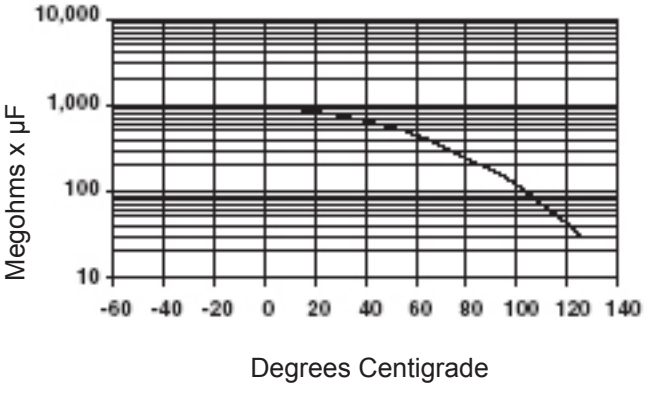
Polypropylene Typical Characteristics at 1 kHz





Polyphenylene Sulfide Typical Characteristics at 1 kHz

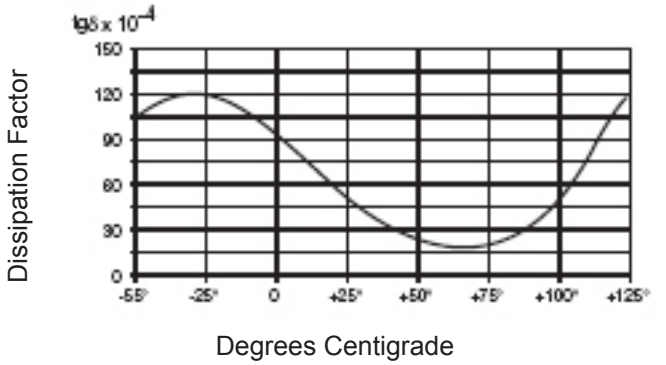


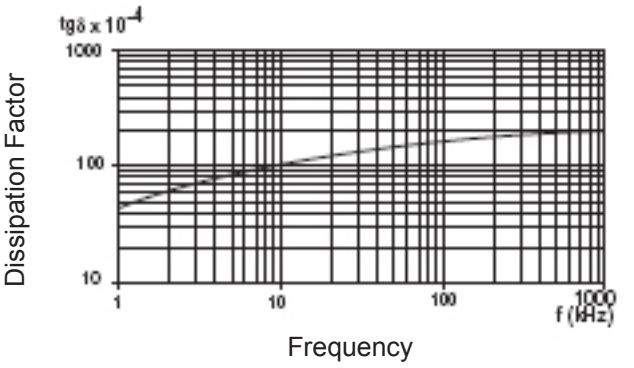


Dissipation Factor vs. Temperature

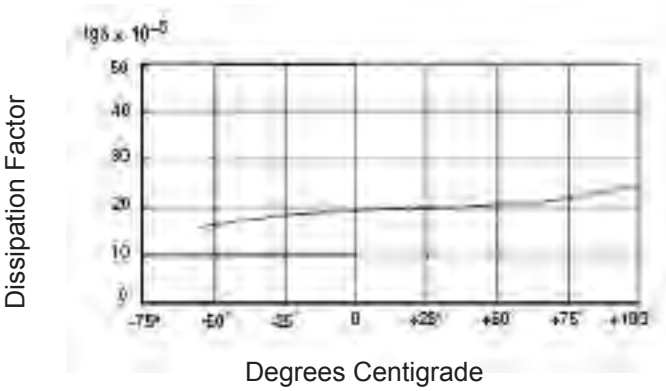
Dissipation Factor vs. Frequency

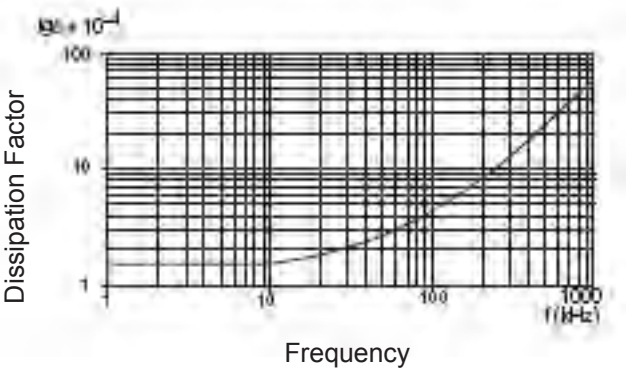
Polyester Typical Characteristics



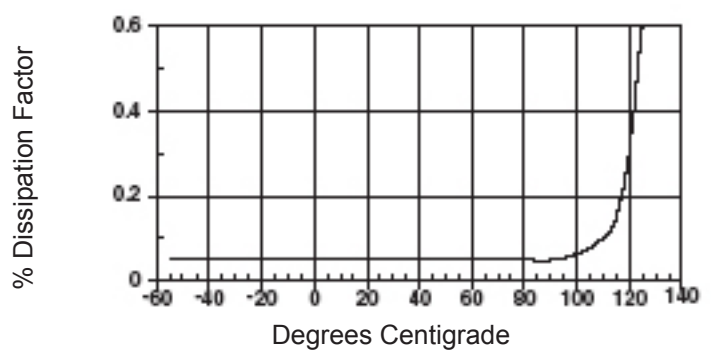


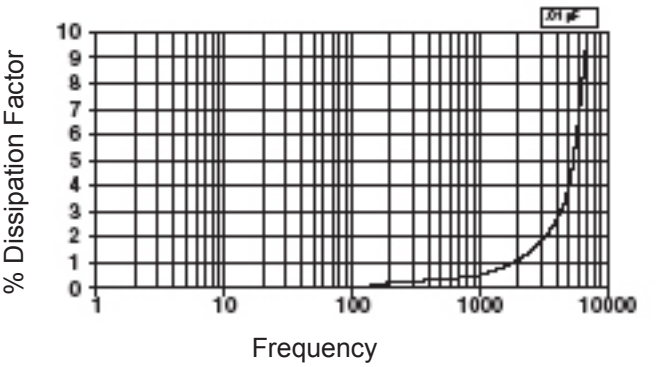
Polypropylene Typical Characteristics





Polyphenylene Sulfide Typical Characteristics





Capacitance is within tolerance when measured at 1 kHz ±20 Hz (120 Hz for polyester if C >1 µF) and 25 ºC ±5 °C. Standard tolerance is ±10%.

Dissipation Factor or tan σ is the ratio of the capacitor's ESR to its reactance. It's no more than specified when measured at 1 kHz ±20 Hz (120 Hz for polyester if C>1 µF) and 25 ±5 °C.

Insulation Resistance changes from a minimum resistance capacitance product (MΩ•µF) to a minimum resistance (MΩ) for rated capacitances above 0.25 to 0.5 µF, depending on the capacitor type. It is no less than the lesser of the RC product or the R specified, when measured at 100 Vdc after 2 minutes and at 25 ±5 °C.

Rated Voltage is the maximum continuous voltage for actual use up to the rated maximum operating temperature.

Dielectric Strength is the maximum peak voltage that the capacitor is rated to withstand at room temperature. Test by applying the specified multiple of rated voltage for one minute through a current limiting resistance of 100 Ω per volt. As an illustration, to test a Type DPM capacitor rated 250 Vdc and 175% dielectric strength, apply 438 Vdc through a 43.8 kΩ or higher value resistor.

Life Test: Subject capacitors to rated maximum temperature ±3 °C with the specified multiple of rated voltage applied for 500 or 1,000 (+72, -2) hours as specified. There will be no visual damage and the capacitance will not have changed more than ±5%. Insulation resistance will not decrease to less than 50% of initial limit. Dissipation factor will not increase to more than initial limit.

Pulse Capability is peak-current Capability. The ability of the capacitor to withstand current transients is set largely by the integrity of the lead connections and is indicated by the dV/dt rating, the maximum permitted rate of change of voltage in V/µs. The peak current rating in amps is the rated capacitance in µF times the dV/dt rating:

$$Ipk = C(dV/dt)$$

Marking includes part number, capacitance in µF, tolerance in %, manufacturer and rated voltage in Vdc and Vac. Small units may include only Type, CD, capacitance in pF and a tolerance code. Example: "DLMCD" and "682K" means Type DLM, 6800 pF ("2" is the number of zeroes) and 10%.

When used, tolerance codes are:

F = ± 1%
G = ± 2%
H = ± 6%
I = ± 3%
J = ± 5%
K = ±10%
M = ±20%

Metallized vs. Film/Foil Construction. Here's how to choose. For a metallized film capacitor, the capacitor plates are aluminum sprayed onto the dielectric film by thin-film vacuum deposition. Compared to making the capacitor with separate foil and film sheets, metallizing enables smaller size, lighter weight, lower cost per microfarad and self-healing, but it also engenders lower current capability. Smaller size and cost is especially striking in high capacitance ratings.

Self healing refers to an internal short circuit from an overvoltage transient or a fault in the film which clears in microseconds by vaporizing the aluminum metallizing at the fault site. There is a glitch in the applied voltage, but the capacitor suffers no permanent damage save a negligible reduction in capacitance. The advantages make CDE metallized film capacitors the correct high-value

choice for all applications except four:

• low capacitance, less than .01 µF, where size difference is not significant and the film/foil material cost is less,

• high continuous current as in a resonant circuit,

• high-transient current as in a snubber circuit, and

• low noise where self clearing is a problem with its attendant, albeit rare, volts of noise.

Polyester Dielectric: Just as metallized is usually the CDE construction of choice, so too, polyester is usually the dielectric film material of choice. Of the three CDE dielectrics, polyester has the highest dielectric constant and delivers the lowest cost, smallest size capacitors with the bonus of being able to operate to 125 °C at half rated voltage. However, with a DF hovering at 1% at higher temperatures, power dissipation prevents its choice for high current or high-frequency AC voltage applications, and with about a 5% capacitance change from –55 °C to 0 °C and from 50 °C to 125 °C, polyester is not the choice for precision capacitance at temperature extremes. But notice that capacitance changes only ±1% from 0 °C to 50 °C.

Polypropylene Dielectric with its low dissipation factor empowers CDE capacitors for high-current DC, high-voltage AC and high-frequency AC applications. And its high insulation resistance and low dielectric absorption are a fit for precision DC capacitors. It would displace polyester in many applications except its low dielectric constant and unavailability of thin-gauge films produces larger case sizes and prices. A slight handicap — its maximum operating temperature is 105 °C.

Polypropylene fits many of the applications polyester misses. It even complements polyester in wide temperature applications: capacitance decreases with temperature at about the same rate as capacitance increases for polyester capacitors, so a polypropylene capacitor in parallel with a polyester spawns a temperature-compensated capacitor.

Polyphenylene Sulfide is for precision capacitance and wide temperature applications. Able to operate from –55 °C to 125 °C and hold capacitance change to less than 1% over all but the extremes of the range, polyphenylene sulfide is the preferred precision-capacitor dielectric and is the dielectric film in FCP chip capacitors.

AC Voltage Operation:
You can use all CDE film capacitors with either AC or DC voltages or a combination of the two. The rules for successful application are: 1) don't exceed the dielectric's voltage capability; 2) keep the capacitor cool, and 3) don't operate with corona. As a practical matter, here's how you do those three rules.

Limit the voltage peaks to the rated DC voltage. Limit the current peaks to the rated capacitance times the dV/dt rating. For high-frequency operation limit the power dissipated so that the case-temperature rise is no more than 15 °C and at high temperatures the case temperature no greater than the maximum operating temperature. The maximum high frequency sine wave voltage for a 15 °C rise may be calculated using the following formulas:

Round cases:

$$V_{RMS} = \sqrt{\frac{11(.5\pi D^2 + \pi DL)}{2\pi f C \bullet DF(\%)}}$$

Oval cases:

$$V_{RMS} = \sqrt{\frac{21(TH + TL + HL)}{2\pi f C \bullet DF(\%)}}$$

D, T, H, and L are dimensions taken from the ratings dimensions chart.

DF is dissipation factor in percent at operating frequency taken from the DF vs. Frequency charts which appear two pages back.

And for rule 3, limit the applied voltage to the maximum AC rating listed for each type to avoid corona.

Corona is partial breakdown of the dielectric by sparking across air voids in the insulation system. It occurs with the application of AC voltage because the effective "capacitance" of the voids is lower than the surrounding dielectric material. Like low-value capacitors connected in series with high-value ones, the voids get higher voltage gradients and they break down. Corona is to be avoided because the sparking tends to carbonize the dielectric which converts it to conductive material and eventually a carbon track can short the capacitor.

Comparison of Dielectrics

Dielectric	Best Tolerance	Change –25 to 85 °C	Change/ Year	Typical DF	Typical DA*	IR	Size 1 µF/100 V
Polyester, Metallized	±5%	+5%	0.40%	0.50%	0.3%	30 GΩ	0.09 in³
Polypropylene, Metallized	±5%	–3%	0.10%	0.10%	0.1%	100 GΩ	0.13 in³
Polyphenylene Sulfide (PPS), Metallized	±2%	±0.5%	<1%	0.20%	0.08%	3 GΩ	0.09 in³
Polyester, Film/Foil	±5%	+5%	0.40%	0.50%	0.35%	100 GΩ	0.40 in³
Polypropylene, Film/Foil	±5%	–3%	0.20%	0.05%	0.1%	200 GΩ	0.71 in³

* Dielectric absorption — a measure of energy stored in the dielectric. Needs to be low for sample-and-hold circuit applications to avoid voltage rebound

Metallized Film Capacitor Lifetime Evaluation and Failure Mode Analysis

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Abstract
One of the main concerns for power electronic engineers regarding capacitors is to predict their remaining lifetime in order to anticipate costly failures or system unavailability. This may be achieved using a Weibull statistical law combined with acceleration factors for the temperature, the voltage, and the humidity. This paper discusses the different capacitor failure modes and their effects and consequences.

Keywords
Metallized film capacitor; failure mode; lifetime.

1 Capacitor technologies

The following different power capacitor technologies are used in inverters:

- Electrolytic capacitors characterized by very big capacitance per volume unit, but with low rated voltages and very important power losses due to the ionic conductivity. In particular, the bigger the capacitance density, the lower the rated voltage.
- Film foil capacitors made of dielectric films between two plain aluminium foils. These capacitors can sustain very high currents.
- Metallized film capacitors, which are made with dielectric films with a metallic coating on the surface. With this technology the electric-field stress may be much bigger than with film capacitors thanks to the metallization self-healing capability.

Today the dielectric films that are used are mainly polypropylene (PP) or polyethylene terephthalate (PET). Formerly, paper (PA) was used in film foil technology—either pure paper or mixed with polypropylene (DM). In special applications, where high temperatures are required, polyethylene naphthalene (PEN) up to 125°C or polyphenylene sulfide (PPS) up to 150°C are used.

PET presents the following advantages over PP: a dielectric constant 50% bigger (ε = 3.3 versus 2.2), which means 50% more capacitance in the same volume, a better mechanical resistance (which means a higher endurance to self-healing), and the possibility of manipulating thinner films, consequently leading to a smaller capacitance and a higher exploitation temperature (+10°C). The negative point is that the loss factor is ten times larger, which means a ten-fold increase in temperature elevation for the same rated power. The nominal electrical field is about the same.

The capacitive elements must be dried to remove moisture, which would cause accelerated aging and bigger losses if left in the capacitor. In the case of power capacitors, the dried elements are either impregnated with vegetable oil or with gas (SF_6, N_2, etc.).

The dielectric films are either wound or stacked before being inserted in a plastic or metallic container. The best winding machines are required to produce active wound elements of reliable quality in the case of oil-free capacitors. One way of overcoming the difficulty of controlling the space ratio between the gas and the film in the winding curves is to wind the film on a large-diameter wheel and to cut the film layers to obtain a stack.

The plastic containers are not completely moisture tight—there is always some residual permeability in polymers. In the case of metallized films, this may lead to electrode corrosion when the capacitors are submitted to environmental conditions of high humidity.

The electric-field stess in metallized film capacitors may be much larger than in film foil capacitors. This is obtained thanks to the ability of the electrodes to self-heal. If a breakdown occurs in the polymer, the current will increase through the defect and on the electrode near the defect. Close to the defect the current density will be big enough to evaporate the 100 nm metallic layer. If the capacitor is well designed, the phenomenon will stop when the diameter is large enough to insulate the defect and small enough not to damage the film. The electrode resistance (given in ohm/square) is the key parameter to define to achieve good self-healing behaviour, with Joule losses as small as possible. A thick metallized layer will present a lower resistance, but higher energies will be involved during the self-healing process, leading to greater damage [1-5].

2 Capacitor failure modes

Most of the metallized film capacitors fail because the capacitance drops below the required tolerance. This normally occurs after the expected lifetime given by the manufacturer. The capacitance drop is generally accompanied by an increase of the loss factor.

From a general point of view, the causes of capacitor failures may occur because of bad design, bad processes, or inappropriate application conditions. During the design phase, the following causes may lead to failure: the dielectric film is too thin, insulation distances are too small, the metallization layer is too thick or too thin, or the conductor is the wrong size. During production, causes may include the following: poor mechanical tension control during the winding, bad drying (leaving too high a humidity content in the capacitor), or bad sealing. In application, the causes may be: higher voltages, EMI, lightning, higher temperature, or a high humidity environment.

The failure modes are a little more complicated to describe because different causes may lead to the same modes. Figure 1 gives a non-exhaustive summary of the possible failure modes which can occur in metallized film capacitors.

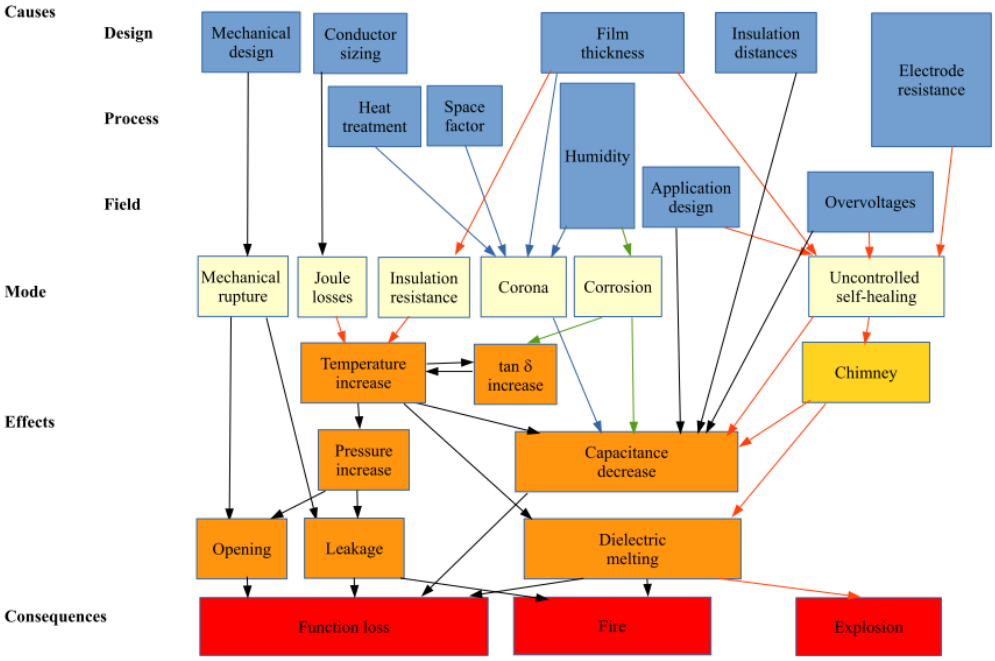

Fig. 1: Metallized film capacitor failure modes with their causes, effects, and consequences

For example, bad space factor control of the dielectric films during the winding operation will be the cause of the electrode corona demetallization, which will lead to a fast capacitance drop and to the loss of functionality of the capacitor.

A bad choice of the metallization resistance value, or poor metallization control during the film manufacturing process, leads to bad self-healing management, which may damage the dielectric film mechanically and produces heat which is transmitted locally to the next film layers. At this location the dielectric strength of the film drops and breakdown may occur. Consequently, chimneys of melted polypropylene may appear through the winding. The formed channel is conductive, inducing a drop in the insulation resistance and a leakage current that can generate enough heat to melt the polypropylene and increase the internal pressure of the capacitor. Along with bad metallization resistance, the final consequence can, in the worst case, lead to fire ignition or even a capacitor explosion.

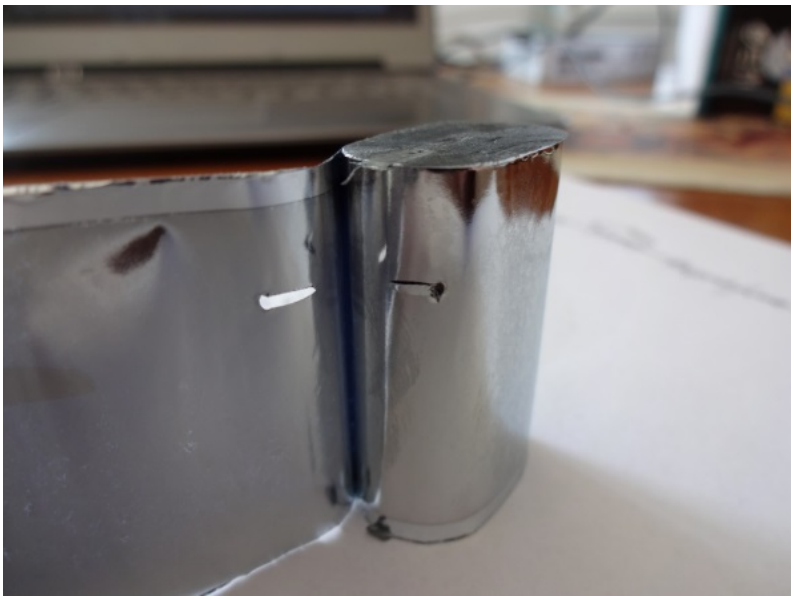

Fig. 2: Chimney through the film layers in the capacitor winding

One of the main failure modes is often due to high currents, which increase the capacitor temperature, leading to a reduction of the breakdown voltage and, in the worse cases, even melting of the capacitor. In this regard, the shape of the capacitor is very important. For high-power applications, it is important to build short elements in order to reduce the current path length and increase the number of parallel layers, and consequently reduce the heating. The current capability of a capacitor is specified through the series resistance R_s and the loss factor tan δ_s at different frequencies. The relation between the two factors, in the high-frequency domain where the effect of the insulation resistance is negligible, is given by the linear relation

$$\tan \delta_s = \frac{Z_R}{Z_i} = R_s \omega C , \tag{1}$$

where C is the capacitance, $\omega = 2\pi f$ is the frequency, Z_R is the impedance real part and Z_i the impedance imaginary part.

The presence of humidity in the capacitor, because of poor drying during the manufacturing process, or because the moisture permeability of the material was too high, or because the humidity level where the capacitors are installed was too high, may lead to three failure modes with different effects and consequences.

Fig. 3: Electrode corrosion due to the presence of moisture

The first is electrode corrosion (see Fig. 3) [6-8], where the series resistance will slowly increase over time. The effect is a loss factor increase due to the electrode thickness reduction and a heat dissipation increase. The elevation of the temperature will accelerate the capacitance loss because of the reduction of the dielectric strength with temperature, ending with the loss of functionality of the capacitor.

The second effect (see Fig. 4), today known as 'corona' [9-11], is due either to a decrease of the dielectric strength of the gas present in the capacitor in the gaps between the dielectric films or to a poor space factor control of the films. The bigger the gap, the more severe the problem. The thickness of the gap is characterized by the space factor, which is the ratio of the dielectric thickness to the total distance between the electrodes. This space factor is very difficult to control in curves of flat windings, leading manufacturers to build either round winding or stacks. Only performant winding machines can achieve good space factor control by managing the mechanical tension of the films during the winding. The consequence of this is a fast capacitance decrease due to the appearance of corona discharges on the electrode edges, i.e., the locations where the electrical field is more intense due to the point effect. In the case of segmented metallization, the corona failure mode may also propagate from the non-metallic lines which separate the active electrode metallic areas.

Fig. 4: Demetallized electrodes by corona arcing in the gas gap between the films

The third failure mode is a reduction of the insulation resistance, which is the parallel resistance of the capacitor. A decrease in insulation resistance leads to an increase in current leakage from one electrode to the other. This phenomenon is present at low frequency. It may be measured via either the

loss factor (tan δ) or the d.c. resistance R_p. The relation between the two parameters is given by the following relation (only true at very low frequencies):

$$\tan\delta_p = \frac{Z_R}{Z_i} = \frac{1}{R_p \omega C}. \quad (2)$$

This later failure mode may have a runaway behaviour. The more the insulation resistance decreases, the more heat is produced, and the more the temperature increases, which leads to a new insulation decrease. This phenomenon may end with the appearance of chimneys and melting of the dielectric.

3 Lifetime expectancy

The lifetime [12] of a capacitor is the time to failure, where failure is defined as the lack of ability of a component to fulfil its specified function. The failure modes are classified into two main categories: 'early failures' and 'wear out failures', which are reflected in the curve known as the 'bathtub' curve (Fig. 5): at the beginning of the component's existence, in its 'infancy', the failure rate is rapidly decreasing. These 'youth' failures are normally screened by routine tests performed by the manufacturer. They are due to design and process weaknesses which have not been detected by the design and process failure modes and effects analysis FMEA performed during the development. They are more probably due to production process variations or to changes in material quality. The process variations are due to tool wear, operator change, and lack of formation. This early failure mode is not taken into account by the Weibull model theory. In normal operation this failure process should not be observed in the field of applications. If it occurs, the capacitors are normally covered by manufacturer's product warranty.

Once the 'early failures' regime is past, the failure rate starts to follow a statistical prediction law which depends on several parameters that may be defined experimentally as a function of the voltage, the temperature, and the environmental humidity. It has been shown that a Weibull statistic can provide a good prediction of the capacitor lifetime expectancy.

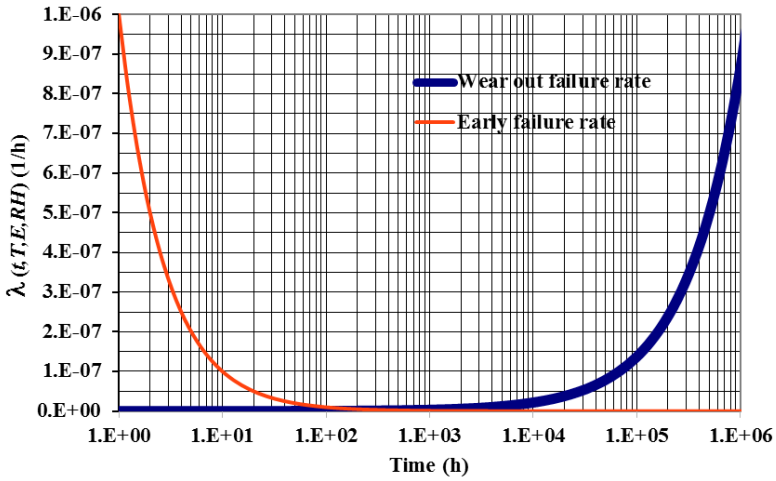

Fig. 5: Bathtub curve of the failure rate function showing the infancy or early failures occurring at the beginning of the component's life (in red) and the wear out curve (in blue) which is defined by aWeibull law with 2 parameters: the power factor p = 1.8 and the inverse of the time necessary for 63% of the sample to fail λ_0 = 1/1,500,000 h^{-1}.

The failure rate $\lambda(t)$ may be given in FIT (failure in time), which is the number of failures occurring during 10^9 h of working of one object, i.e., $3E^{-7}$ h^{-1} corresponds to 300 FIT. The Weibull failure rate is given by

$$\lambda(t) = \lambda_0 \; p\,(\lambda_0 t)^{p-1}, \tag{3}$$

where λ_0 must not be confused with $\lambda(t)$. λ_0 is a constant (independent of time, but dependent on temperature, voltage, and humidity) which corresponds to the inverse of the time necessary for 63% of the sample to fail, and $\lambda(t)$ is the inverse of the mean time to failure (MTTF). In the wear out failure region, $\lambda(t)$ increases with time. The manufacturer specifications give the maximum value of $\lambda(t)$ within the announced lifetime: for example, 150 FIT and 100,000 h of lifetime expectancy in Fig. 5. The slope parameter of the Weibull law is denoted by p.

The survivor or Weibull reliability function $R(t)$ is the probability that a capacitor has not failed or has not lost its function at time t and is still working. The survivor function is given by

$$R(t) = \mathrm{e}^{-(\lambda_0 t)^p} \; . \tag{4}$$

When multiplied by the number of capacitors N in the batch, this gives the expected number of capacitors still working after time t. There are capacitor manufacturers [13] that use a simple exponential model instead of the more complex Weibull model. Actually the exponential model corresponds to a Weibull model where $p = 1$. In this exponential model the failure rate is constant over the time $\lambda(t) = \lambda_0$. To fit this model to the actual statistical behaviour of capacitors, manufacturers limit the exponential model to a time period which they call the 'service life of the product'. After that time period the failure rate starts to increase.

Weibull statistics can also be used to predict the capacitance evolution of a metallized capacitor under electrical, thermal, and humidity stresses. In such cases, the failure definition will be, for example, 1% or 1‰ capacitance loss, depending on the available resolution of the measurement device. The capacitance will be given straightforwardly by the survivor function. The Weibull reliable life, which gives the expected lifetime of a capacitor for a given reliability level (the proportion of remaining working objects, in our case capacitance) is

$$T_{\mathrm{R}} = \frac{1}{\lambda_0}\{-\ln(R)\}^{1/p}, \tag{5}$$

where λ_0 is the failure rate for the special case when 1/e, or 36.8%, of the samples still remain.

Table 1: Capacitor lifetime expectancy factor as a function of the required capacitance minimum in an exponential model.

Reliability (%)	**Lifetime, $1/\lambda_0$ (h)**
36.8	1
50	0.693
63.2	0.500
80	0.223
90	0.105
95	0.051
98	0.020

If the manufacturer gives a capacitor failure rate of 50 FIT at 40°C and $U_n/2$ for an exponential model, it means that the lifetime expectancy for a capacitance drop tolerance of 10% will be 2.1×10^6 h in these conditions.

4 Aging acceleration factors

The speed of capacitance drop depends on the temperature, the voltage, and the humidity. The increases in these parameters are considered as aging acceleration factors. These factors are determined experimentally based on the following theories.

4.1 Temperature

It has been shown [14] that capacitor aging as a function of the temperature follows an Arrhenius law, in other words an exponential law

$$t(T) = t_{T_n} \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T} - \frac{1}{T_n}\right)\right), \tag{6}$$

where t_{T_n} is the expected lifetime at a reference temperature, 70°C or 85°C for example, k_B is the Boltzmann constant, and E_a is an activation energy. A relatively good fit of Epcos/Vishay factors (see Fig. 6) may be obtained with a ratio E_a/k_B = 7000 K [15]. Between 40°C and 70°C there is an acceleration factor of 7.1 with the parameters considered.

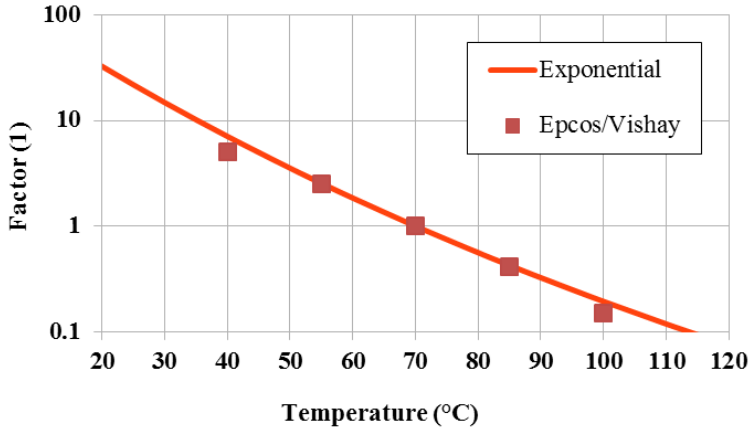

Fig. 6: Temperature acceleration factor

4.2 Voltage

Regarding voltage dependency, authors use either an inverse power law

$$t = t_{U_n}\left(\frac{U}{U_n}\right)^{-n} \tag{7}$$

or an exponential law

$$t = t_{U_n} \exp\left(-\alpha \frac{(U - U_n)}{U_n}\right), \tag{8}$$

where t_{U_n} is the expected lifetime at the nominal voltage or reference voltage and t/t_{U_n} is the voltage acceleration factor.

A careful examination shows that these laws do not differ much when considered between 0.7 and 1.3U_n. To sketch Fig. 7, n and α have been both set to 3.5.

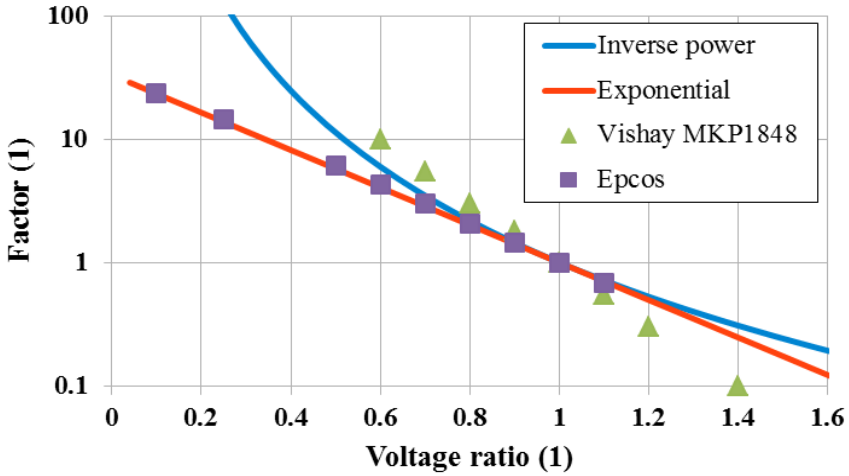

Fig. 7: Acceleration factor of the aging as a function of the voltage level. In this diagram the inverse power law and the exponential law are both parameterized with a factor 3.5. The Vishay data would fit better with an exponential law with factor 5 [16, 17].

Between $U_n/2$ and U_n there is an acceleration factor of approximatively 5 (Epcos) to 10 (inverse power) with the parameters considered. The discrepancy between the values may be attributed to the different technologies produced by the different manufacturers. It is interesting to note that the Vishay display on p. 6 of Ref. [18] has almost the same accelerating factors as Epcos.

4.3 Humidity

Humidity is a concern for capacitors contained in plastic because moisture can permeate through this type of material. Once inside the capacitor, the moisture has several effects: first, it decreases the electrical strength of the gas in the case of oil-free capacitors, leading to corona demetallization of the electrode, and secondly it corrodes the electrode. When moisture is present in the dielectric film, the loss factor is increased, because of the presence of water dipoles, and the insulation resistance is reduced, leading to current leakage and generation of heat. The lifetime as a function of the humidity level can be estimated using the following relation [19]:

$$t(RH) = t_{H_n}\left(\frac{RH_n}{RH}\right)^m, \tag{9}$$

where t_{H_n} is the expected lifetime at a reference humidity level.

4.4 Capacitor lifetime expectancy calculation

To design and size a capacitor correctly engineers must work through two steps. First, they must determine the law parameters: E_a for the temperature, n for the voltage, and m for the humidity. This is basically achieved by defining a plan of the experiment with three different temperatures, voltages, and humidity levels. The second step is the calculation of the lifetime expectancy as a function of the customer specifications. For example, for a solar inverter, half of the time there is no voltage and the temperature is 20°C, 20% of the time the voltage is maximum and the temperature reaches 90°C, and 30% of the time the voltage is 80% of the maximum and the temperature is 60°C. Each stress condition must be converted to a reference condition value. The sum of the contributions will determine the lifetime expectation.

Table 2: Lifetime expectancy with indicative data

Duration (%)	**Voltage (U_n)**	**Temperature (°C)**	**Converted aging weight @ reference conditions(%)**
50	0	20	5
30	0.8	60	25
20	1	90	70

In most applications, in the first step the required dielectric thickness is calculated at the reference temperature for the specified voltage distribution. In the second step the temperature distribution is used to adapt the dielectric thickness to the temperature profile requirement. In the section 'Power cap sizing' of the site http://www.garmanage.com [20], there is a tool which allows the user to calculate the lifetime expectancy with ten different stresses.

Taking again the example of a failure rate of 50 FIT in an exponential model, which gives a lifetime expectancy of 2.1×10^6 h at 40°C and $U_n/2$, it may be calculated by multiplication of Eqs. (7), (8), and (9)

$$t(T,U,RH) = t_{T_n,U_n,RH_n} \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T}-\frac{1}{T_n}\right)\right)\left(\frac{U}{U_n}\right)^{-n}\left(\frac{RH_n}{RH}\right)^{m} \tag{10}$$

that the lifetime at 70°C and U_n may be estimated to be approximatively equal to 60,000 (h) or nearly 7 years.

5 Technology qualification

The next thing to do is to evaluate the confidence level that, in operation, a given number of capacitors k in a batch of N capacitors are fulfilling the defined condition (for example, a proportion $p > 90\%$ of remaining capacitance after 100,000 h of operation).

The confidence level is given by a binomial law (failed/not failed) and will improve with the number of capacitors which pass the tests. The reverse question is: how many pieces have to be tested to get a given confidence level? The simple relation

$$n = \frac{\log(1-\mathrm{CL})}{\log(p)} \tag{11}$$

yields the number of pieces which must tested without failure to get a confidence level CL. For example, in an accelerated test at 70°C and $1.4U_n$, $n = 16$ pieces must be tested, and none must fail during a 2000 h test, to get a confidence level of CL = 80%; in other words, 80% of all the capacitors will have a remaining capacitance greater than $p = 90\%$ in these conditions. Considering the acceleration factors, the test will state that 80% of all the capacitors will have more than 90% of their capacitance after 60,000 h of operation at U_n and 40°C.

In order to introduce the new technology of oil-impregnated metallized film with an electrical field rated at 200 V/μm, the company Montena Components (today called Maxwell Technologies), in collaboration with the French railways company (SNCF), ran comparative accelerated tests during the 1990s, alongside the tests defined by the IEC 61071 standard [21]. The TGV high speed train input filter capacitor bank has a nominal voltage of 1800 V d.c. and a capacitance of 8 mF. The requested lifetime is 20 yr with a capacitance tolerance ±10%. The bank is built with four 2 mF capacitors.

The volume and weight of the capacitors vary inversely with the square of the electrical field. The first generation was operated at 150 V/μm, and each capacitor had a mass of 44 kg. In a TGV in normal commercial use, a bank at 200 V/μm (four capacitors of mass 22 kg with film thickness of 9 μm) was mounted in one of the tractors, and a bank at 240 V/μm (four capacitors of mass 17 kg with film thickness of 7.4 μm) was mounted on the other side of the train. The voltage and climatic conditions were therefore the same for the two batteries.

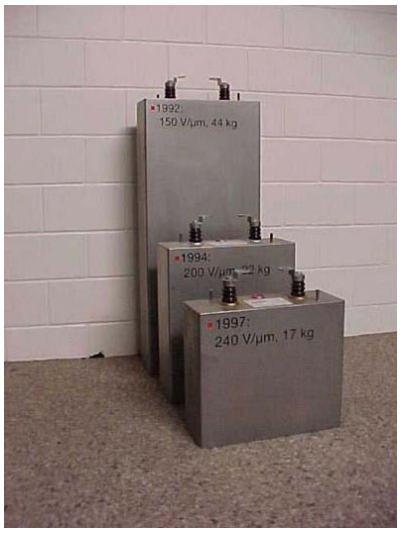

Fig. 8: A 2 mF 1800 V d.c. capacitor for input filters of TGV application. The sizes correspond to 150, 200, and 240 V/μm in the dielectric.

In parallel with the field experiment, a 2 mF capacitor, made with 9 µm thick film, has been tested in an oven at 70°C in the manufacturer's laboratory at 2500 V d.c., a voltage which corresponds to an electrical field of 280 V/μm. The capacitors in the TGV have been measured before the test and after 6 months and one, two, and four years, the capacitors in the laboratory have been measured weekly at the beginning and monthly at the end of the test.

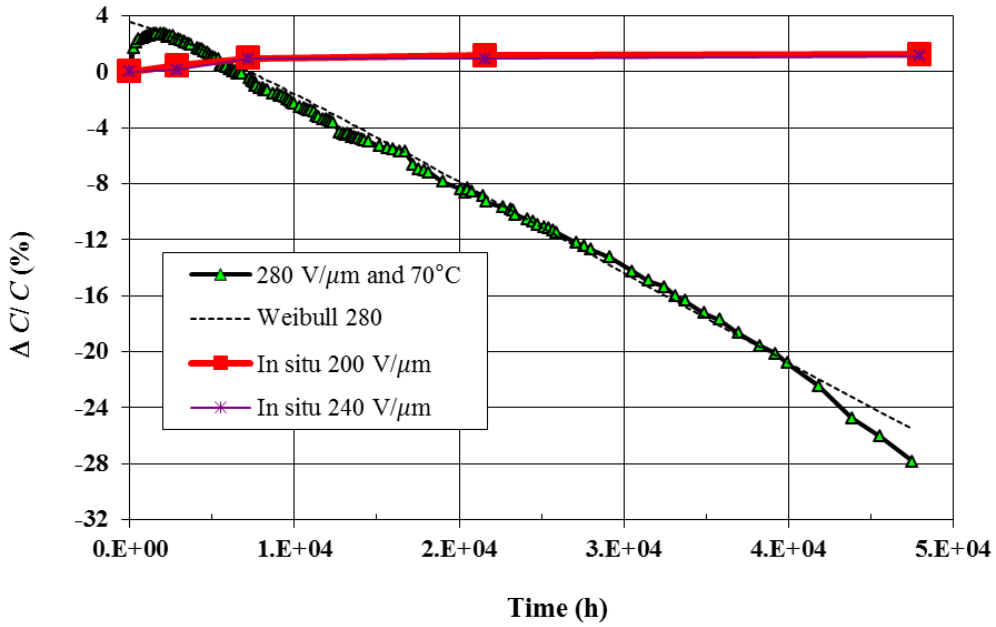

Fig. 9: Capacitance loss as a function of time for 280 V/µm laboratory test at 70°C and TGV in situ tests at 200 and 240 V/mm film [22].

At the beginning of the stress application a slight capacitance increase is observed because of the electrostatic compression of the films. It is also interesting to note that during four years the two capacitor batteries mounted in the TGV in commercial use are still in the compression phase.

The capacitance loss of a metallized film capacitor may be fitted by a Weibull law. In the case of an electrical field of 280 V/μm and an oven temperature of 70°C, a good fit is obtained with $p = 1.2$ and $\lambda_0 = 1/120{,}000\ \mathrm{h}^{-1}$. The 10% capacitance loss has been reached after 20,000 h at 70°C and 280 V/μm; tan δ was smaller than $70\mathrm{E}^{-4}$, whereas it was $30\mathrm{E}^{-4}$ at the beginning.

With a very rough estimation of mean temperature of 35°C inside the TGV tractor, a temperature acceleration factor of 10 between 35 and 70°C and a voltage acceleration factor of 10 between 200 and 280 V/μm, one may expect a lifetime of 2,000,000 h to reach 10% capacitance loss at 35°C and 200 V/μm. With an acceleration factor of 3 between 240 and 280 V/μm, the expected lifetime at 240 V/μm would be 'only' 600,000 h.

6 Conclusion

Capacitors often represent a small part of the cost of an installation. Their failure however may have huge physical and financial consequences. A typical example is a small capacitor of cost 1p connected in series in the electronic control of a freezer which leads to almost all these devices having to be scrapped when they fail. When capacitors have to be used in highly reliable applications, they should be tested in advance.

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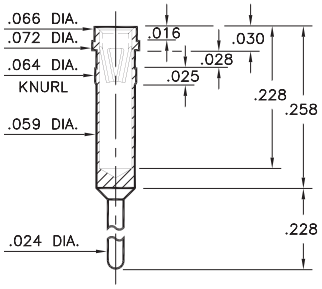
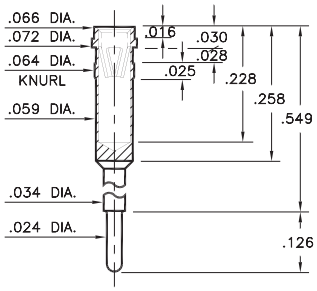
PIN RECEPTACLES

FOR .025" - .037" DIAMETER PINS AND .025" SQUARE PINS

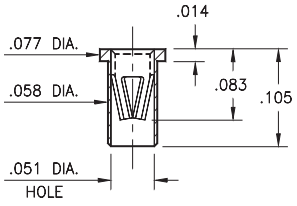
1305
1305-0-15-XX-47-XX-04-0
Press-fit in .061 mounting hole



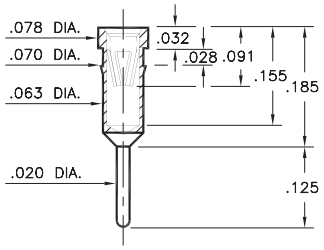
1306
1306-0-15-XX-47-XX-04-0
Press-fit in .061 mounting hole



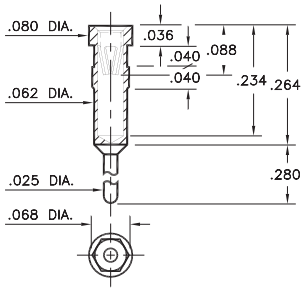
7305
7305-0-15-XX-47-XX-10-0
Solder mount in .060 min. mounting hole
Also available on 8mm wide carrier tape:
6,000 parts per 13" reel
See page 194.12 for Tape & Reel details



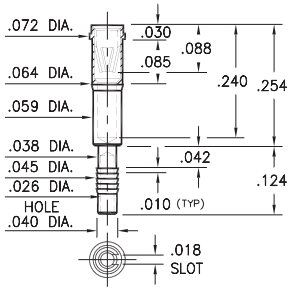
0400
0400-0-15-XX-47-XX-04-0
Press-fit in .067 mounting hole



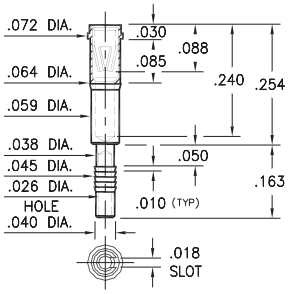
0335
0335-0-15-XX-47-XX-04-0
Hex press-fit in .064 plated through-hole



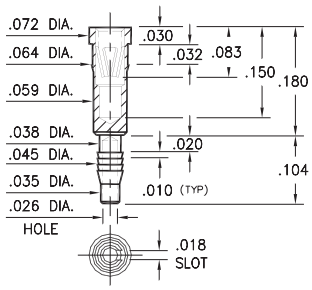
4614
4614-0-31-XX-47-XX-04-0
Compliant press-fit in .040 ± .003 plated hole. For .060" →.100" thick board



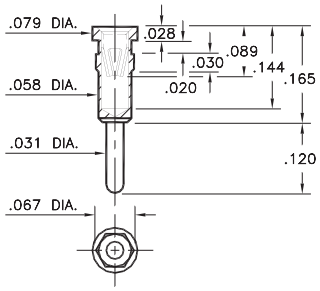
4615
4615-0-31-XX-47-XX-04-0
Compliant press-fit in .040 ± .003 plated hole. For .090" →.130" thick board



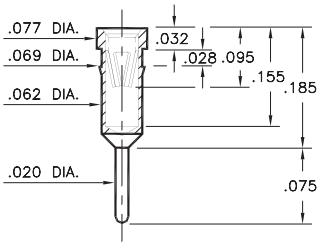
7614
7614-0-31-XX-47-XX-04-0
Compliant press-fit in .040 ± .003 plated hole. For .060" →.100" thick board



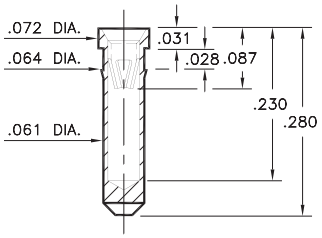
8401
8401-0-15-XX-47-XX-04-0
Hex press-fit in .063 plated through-hole



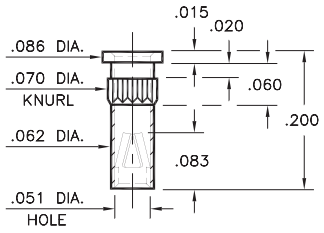
2400
2400-0-15-XX-47-XX-04-0
Press-fit in .066 mounting hole



6857
6857-0-15-XX-47-XX-10-0
Press-fit in .062 mounting hole



9393
9393-0-15-XX-47-XX-10-0
Press-fit in .067 mounting hole



SPECIFICATIONS:

Shell Material: Brass Alloy 360, 1/2 Hard

Contact Material: Beryllium Copper Alloy 172, HT

Dimensions: Inches

Tolerances On: Lengths: ± .005
Diameters: ± .002
Angles: ± 2°

RoHS-2 2011/65/EU

ORDER CODE: XXXX - X - XX - XX - 47 - XX - XX - 0

BASIC PART #

SPECIFY SHELL FINISH:
- **01** 200 µ" TIN/LEAD OVER NICKEL
- **80** 200 µ" TIN OVER NICKEL (RoHS)
- **15** 10 µ" GOLD OVER NICKEL (RoHS)

SPECIFY CONTACT FINISH:
- **01** 200 µ" TIN/LEAD OVER NICKEL
- **80** 200 µ" TIN OVER NICKEL (RoHS)
- **27** 30 µ" GOLD OVER NICKEL (RoHS)

SELECT CONTACT:
#47 CONTACT (DATA ON PAGE 256)
(For alternate contact choices, see group D on page 248)

PART NUMBER CODING

___C___S__N-M71RC

INSULATOR / CONTACT MATERIAL

PR = PBT / BRASS
OPERATING TEMPERATURE: -40° C TO +105° C.
PROCESSING TEMP: 245°C ±5°C FOR 3~5 SECS MAX.

NR = NYLON 6T / BRASS
OPERATING TEMPERATURE: -40° C TO +105° C.
PROCESSING TEMP: 230°C FOR 60 SECS MAX.
(260°C FOR 10 SECS MAX.)

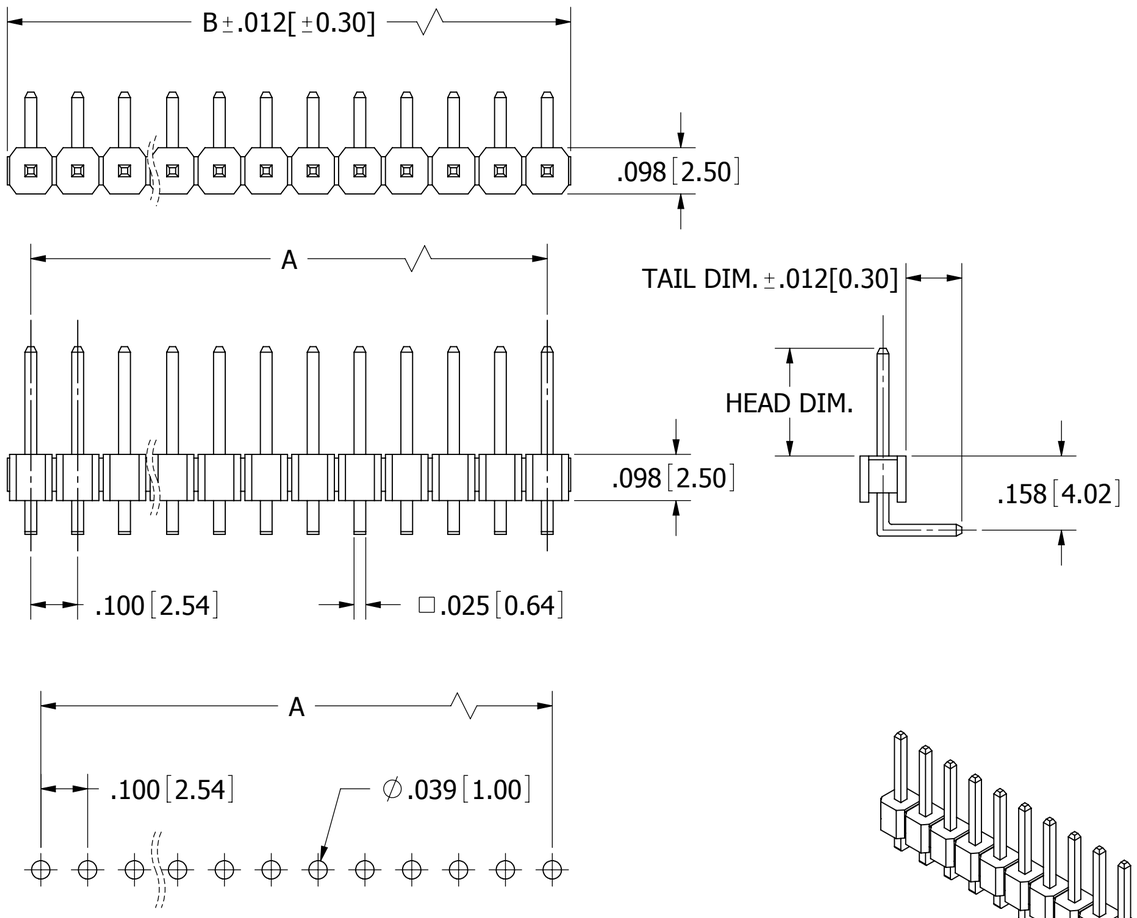
TERMINATION TYPE

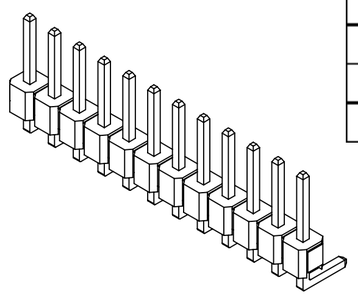
NUMBER OF POSITIONS
(CONTACTS PER ROW, 002 THRU 040)

PLATING
(ALL PLATINGS HAVE .000030"~.000050" MIN NICKEL UNDERPLATE)

	CONTACT SURFACE	TERMINATION
B	.000010" GOLD	.000100" PURE TIN, MATTE
C	.000030" GOLD	.000100" PURE TIN, MATTE
E	TIN OVERALL	
P	GOLD FLASH OVERALL	

REVISIONS				
REV.	ECO. NO	DESCRIPTION	DATE	BY
A	2268	INITIAL RELEASE	03/21/2011	LH
B	2422	ADD 'P' PLATING OPTION	08/08/2011	GC





RECOMMENDED PCB LAYOUT

TERMINATION TYPE				
CODE	HEAD DIM		TAIL DIM	
	INCH	MM	INCH	MM
BA	0.230	5.84	0.120	3.05
BB	0.230	5.84	0.220	5.59
BC	0.230	5.84	0.320	8.13
BD	0.230	5.84	0.420	10.67
BE	0.230	5.84	0.520	13.21
BF	0.230	5.84	0.620	15.75
BG	0.230	5.84	0.720	18.29
BH	0.230	5.84	0.820	20.83
BI	0.230	5.84	0.920	23.37
BJ	0.230	5.84	1.020	25.91
GA	0.318	8.08	0.120	3.05
GB	0.318	8.08	0.220	5.59
GC	0.318	8.08	0.320	8.13
GD	0.318	8.08	0.420	10.67
GE	0.318	8.08	0.620	15.75
GF	0.318	8.08	0.820	20.83
DA	0.120	3.05	0.140	3.56

PART NUMBER	A		B	
	INCH	MM	INCH	MM
___C002S__N-M71RC	0.100	2.54	0.200	5.08
___C003S__N-M71RC	0.200	5.08	0.300	7.62
___C004S__N-M71RC	0.300	7.62	0.400	10.16
___C005S__N-M71RC	0.400	10.16	0.500	12.70
___C006S__N-M71RC	0.500	12.70	0.600	15.24
___C007S__N-M71RC	0.600	15.24	0.700	17.78
___C008S__N-M71RC	0.700	17.78	0.800	20.32
___C009S__N-M71RC	0.800	20.32	0.900	22.86
___C010S__N-M71RC	0.900	22.86	1.000	25.40
___C011S__N-M71RC	1.000	25.40	1.100	27.94
___C012S__N-M71RC	1.100	27.94	1.200	30.48
___C013S__N-M71RC	1.200	30.48	1.300	33.02
___C014S__N-M71RC	1.300	33.02	1.400	35.56
___C015S__N-M71RC	1.400	35.56	1.500	38.10
___C016S__N-M71RC	1.500	38.10	1.600	40.64
___C017S__N-M71RC	1.600	40.64	1.700	43.18
___C018S__N-M71RC	1.700	43.18	1.800	45.72
___C019S__N-M71RC	1.800	45.72	1.900	48.26
___C020S__N-M71RC	1.900	48.26	2.000	50.80
___C021S__N-M71RC	2.000	50.80	2.100	53.34
___C022S__N-M71RC	2.100	53.34	2.200	55.88
___C023S__N-M71RC	2.200	55.88	2.300	58.42
___C024S__N-M71RC	2.300	58.42	2.400	60.96
___C025S__N-M71RC	2.400	60.96	2.500	63.50
___C026S__N-M71RC	2.500	63.50	2.600	66.04
___C027S__N-M71RC	2.600	66.04	2.700	68.58
___C028S__N-M71RC	2.700	68.58	2.800	71.12
___C029S__N-M71RC	2.800	71.12	2.900	73.66
___C030S__N-M71RC	2.900	73.66	3.000	76.20
___C031S__N-M71RC	3.000	76.20	3.100	78.74
___C032S__N-M71RC	3.100	78.74	3.200	81.28
___C033S__N-M71RC	3.200	81.28	3.300	83.82
___C034S__N-M71RC	3.300	83.82	3.400	86.36
___C035S__N-M71RC	3.400	86.36	3.500	88.90
___C036S__N-M71RC	3.500	88.90	3.600	91.44
___C037S__N-M71RC	3.600	91.44	3.700	93.98
___C038S__N-M71RC	3.700	93.98	3.800	96.52
___C039S__N-M71RC	3.800	96.52	3.900	99.06
___C040S__N-M71RC	3.900	99.06	4.000	101.60

NOTES:
1. INSULATOR MATERIAL: SEE PART NUMBER CODING, UL 94V-0, BLACK.
2. CONTACT MATERIAL: SEE PART NUMBER CODING.
3. CONTACT PLATING: SEE PART NUMBER CODING.
4. CURRENT RATING: 3 AMPS PER CONTACT.
5. INSULATOR RESISTANCE: 5000 MEGOHMS MIN.
6. CONTACT RESISTANCE: 20 MILLIOHMS MAX.
7. DIELECTRIC WITHSTANDING: 1000 VAC.
8. OPERATING TEMPERATURE: SEE PART NUMBER CODING.
9. *PROCESSING TEMP.: SEE PART NUMBER CODING.

*INDICATED TEMPERATURE AND TIME IS FOR COMPONENT INSULATOR. HIGHER PROCESSING TEMPERATURES MAY BE USED, PROVIDED HEAT IS APPLIED FROM BACK SIDE OF PCB, AND INSULATOR DOES NOT EXCEED INDICATED TEMPERATURE AND TIME.

Pb
RoHS COMPLIANT

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES [MM]

TOLERANCES: ANGULAR:
.XX=± .012 [.30]
.XXX=± .008 [.20]
.XXXX=± .0040 [.100]

INTERPRET DIMENSIONS AND TOLERANCING PER: ASME Y14.5M-2009

DRAWN	DATE	NAME
	03/21/2011	LH

SULLINS CONNECTOR SOLUTIONS

TITLE: HEADER MALE .100"[2.54mm]PITCH, RA

PART NUMBER: _R_C___S__N-M71RC

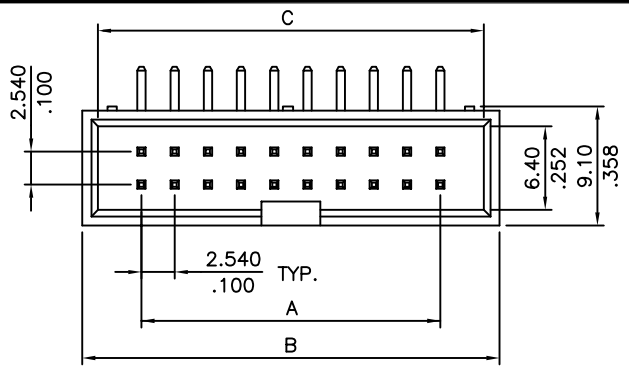
SIZE	CAGE CODE	DWG. NO.	REV
C	54453	11637	B

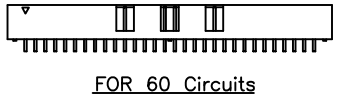
SCALE: 4:1 SHEET 1 OF 1

FILE NAME: Z:\ECO PENDING\2422, TAIWAN HEADER 100 CC ADD P PLATING\11637, _R_C___S__N-M71RC PRINT: 8/26/2011

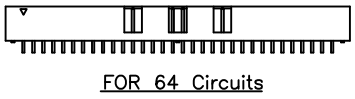
SIGN	DATE	DESCRIPTION	APPROVER

THIS IS CAD DRAWING, DO NOT REVISE MANUALLY!!!

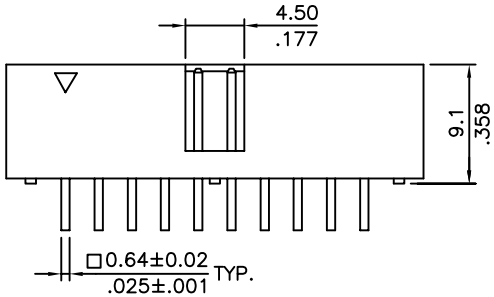


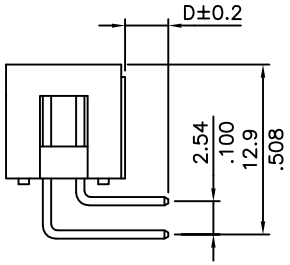


FOR 60 Circuits

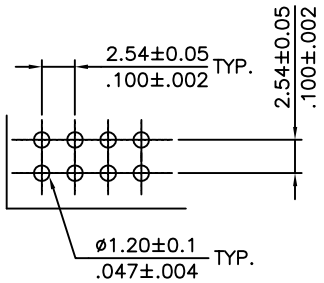


FOR 64 Circuits





A = 2.54 * No. of Spaces
B = A + 10.16
C = A + 7.86
* Available circuits: 06, 08,10,14,16,20,24,
26,30,34,40,44,50,60,64



Recommended P.C. Board Layout

Material

- Insulator: Glass Filled Polyester
- Flammability: UL94V-0
- Color: Black
- Contacts: Brass
- Plating termination: 1.2u" Au min, 50u" Ni

Ratings

- Current: 3A
- Voltage: 250V AC(r.m.s.)
- Contact Resistance: <20mΩ
- Insulation Resistance: >1,000MΩ
- Dielectric Withstanding Voltage: 1500V AC for one minute
- Operating Temperature: -40°C ±105°C
- Solderability: 245°C ± 5°C for 3±0.5 seconds

RoHS Compliant

PLATING
1= Full Gold Flash/Nickel (STD)
5 = 120u" Tin over 50u" Nickel
7 = Selective 15u" Gold/Nickel
8 = Selective 30u" Gold/Nickel
NON-STD may require MOQ

PART NUMBER:
302-RXXX
Number of circuits

Dim. D
3.10 - leave blank (standard)
2.80 - add 2.8 to end of p/n
may require MOQ

ON-SHORE TECHNOLOGY, INC.

TITLE	302 Series - Dual Row Right Angle Box Header					
PART NO.	302-RXXX			DWG NO.	302-RXXX.DWG	
APPROVED	CHECKED	DESIGNED	DRAWN		4050	Tolerance
	Marvin 2003.06.16	Marvin 2003.06.16	Marvin 2003.06.16	SHEET: 01/01	UNIT: mm/inches SCALE: NONE REV.: B	X. ±0.30/.012 X.X ±0.20/.008 X.XX ±0.10/.004 X° ±1°

LOC	DIST
E	B

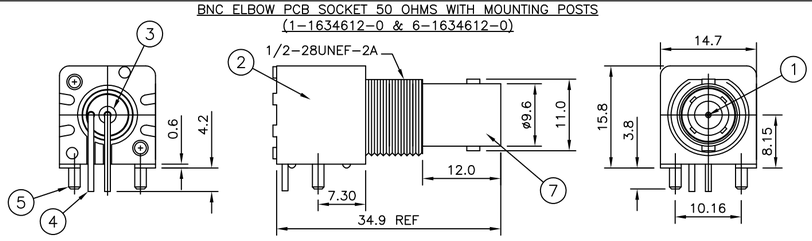
REVISIONS

P	LTR	DESCRIPTION	DATE	DWN	APVD
	C1	REVISED PER ECO-11-005033	31MAR11	RK	HMR
	D	ECO-12-014680	20Aug2012	TITAN	MARTIN
	E	ECO-12-018113	27DEC2012	TITAN	MARTIN

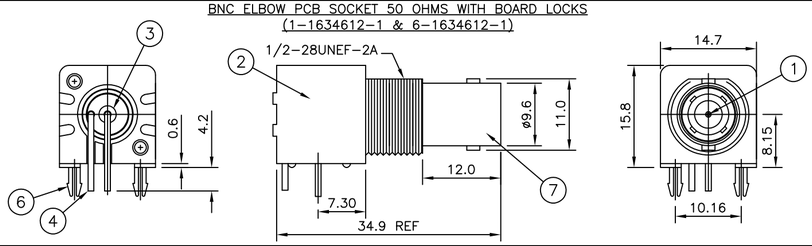
NOTES:

1. SINGLE PACK IN ACCORDANCE WITH AMP SPEC 107-3275
2. 50 TRAY PACK IN ACCORDANCE WITH AMP SPEC 107-3275
3. Au PLATING OVER Ni PLATING OVER Cu PLATING
4. Ni PLATING OVER Cu PLATING
5. TIN PLATING
6. RECOMMENDED SELF-TAPPING SCREW 221108-4
7. RECOMMENDED MOUNT NUT 1-1634816-0
8. RECOMMENDED LOCKWASHER 1-1634817-0
9. FOR TECHNICAL DATA REFER TO YOUR LOCAL TE CONNECTIVITY SALES OFFICE
10. ALL DIMENSIONS ARE NOMINAL FOR REFERENCE ONLY UNLESS OTHERWISE STATED

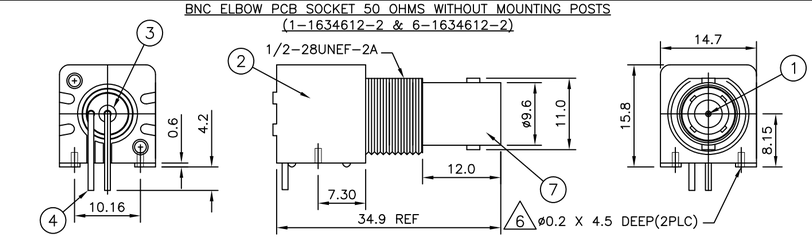
BNC ELBOW PCB SOCKET 50 OHMS WITH MOUNTING POSTS
(1-1634612-0 & 6-1634612-0)



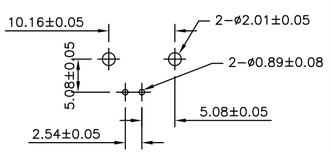
BNC ELBOW PCB SOCKET 50 OHMS WITH BOARD LOCKS
(1-1634612-1 & 6-1634612-1)



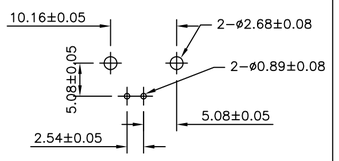
BNC ELBOW PCB SOCKET 50 OHMS WITHOUT MOUNTING POSTS
(1-1634612-2 & 6-1634612-2)



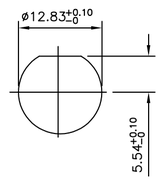
RECOMMENDED PCB LAYOUT
WITH MOUNTING POSTS OR BOARD LOCKS



RECOMMENDED PCB LAYOUT
WITHOUT MOUNTING POSTS



RECOMMENDED MOUNTING HOLE
MAX PANEL THICKNESS: 5.5mm



	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete			
	1	1	1	1	1	1	ZINC DIECAST 4	BODY 7
	–	–	2	2	–	–	BRASS 5	BOARD LOCK 6
	–	–	–	–	2	2	BRASS 5	MOUNTING POST 5
	1	1	1	1	1	1	BRASS 5	SOLDER TAIL 4
	1	1	1	1	1	1	PE-606	INSULATOR 3
	1	1	1	1	1	1	PBT BLACK	HOUSING 2
	1	1	1	1	1	1	BRASS 3	CONTACT 1
	6--2	1--2	6--1	1--1	6--0	1--0	MATERIAL	DESCRIPTION ITEM
	2	1	2	1	2	1		
	QUANTITY PER ASSY						PARTS LIST	

THIS DRAWING IS A CONTROLLED DOCUMENT.

DIMENSIONS: mm

TOLERANCES UNLESS OTHERWISE SPECIFIED:
0 PLC ± 0.5
1 PLC ± 0.3
2 PLC ± 0.2
3 PLC ± –
4 PLC ± –
ANGLES ± –

MATERIAL SEE TABLE

FINISH SEE TABLE

DWN 14 Feb 09 RITA ZUO
CHK 14 Feb 09 ANSON MA
APVD 14 Feb 09 BOB ZHAO
PRODUCT SPEC 108-112000
APPLICATION SPEC —
WEIGHT –

TE Connectivity

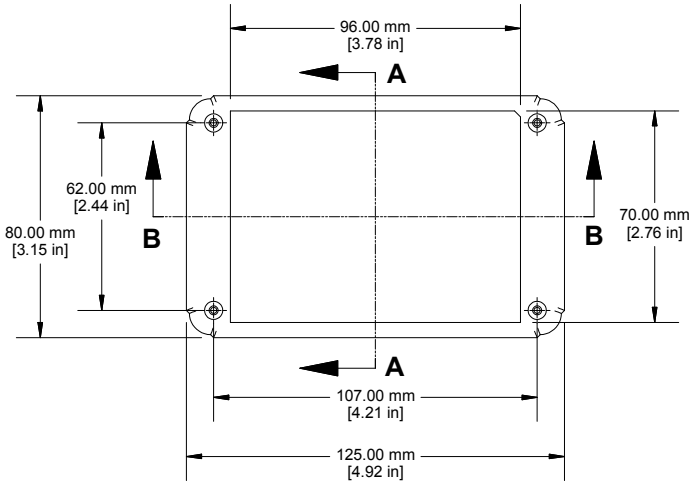
NAME BNC HIGH PROFILE R/A INSULATED PCB SOCKET 50 OHM BLACK
–

SIZE	CAGE CODE	DRAWING NO	RESTRICTED TO
A2	00779	C-1634612	—

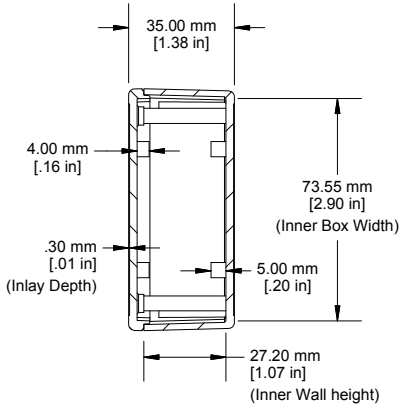
CUSTOMER DRAWING | SCALE NTS | SHEET 1 OF 1 | REV E

1634612

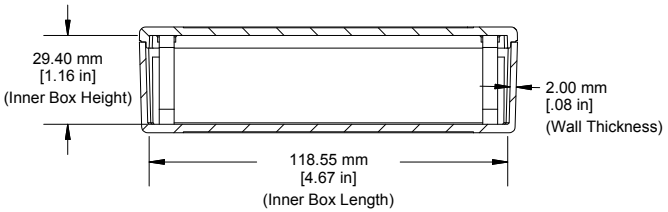
Assembly - Top View



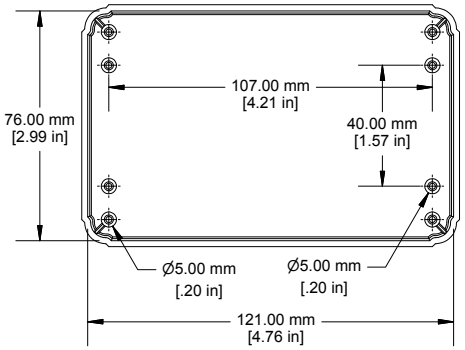
SECTION A-A
End View of Assembly



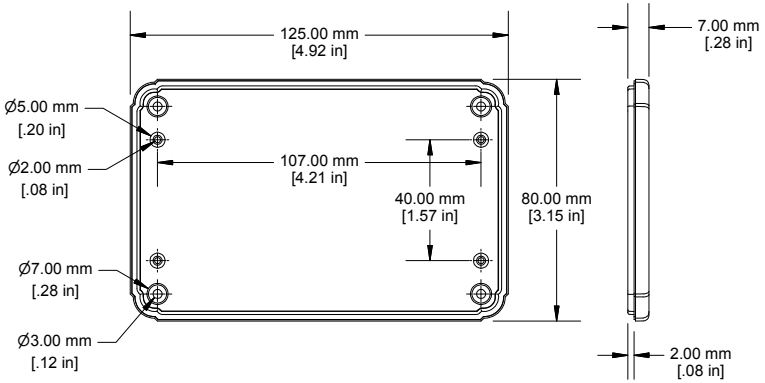
SECTION B-B
Side View of Assembly



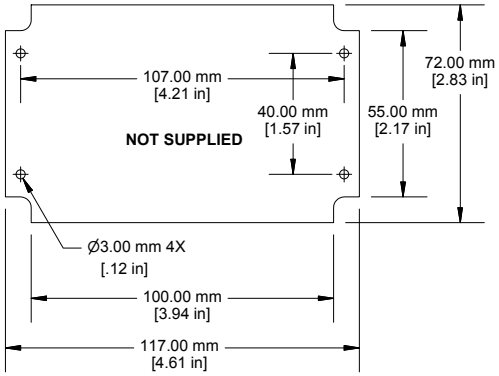
Box - Inside View



Lid - Inside View



Inner Panel



Enclosures can be Factory Modified (Milling, Drilling, Printing etc.)
Contact Factory mjm@hammondmfg.com for quotes
Solid models of this enclosure available in STEP or IGES.

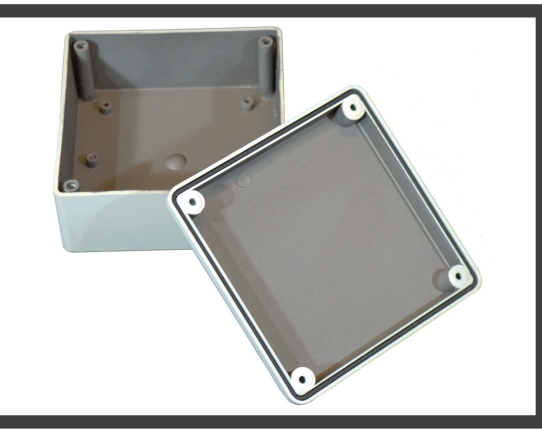
RL6215
Material: ABS (UL94-HB), Light Gray color
Lid Screws: M2.6 x 18
Circuit Board Screws, 4 Supplied (M2.6 self tap)
Suggested Lid Screw Torque: 30 ozf-in (21 cN-m)

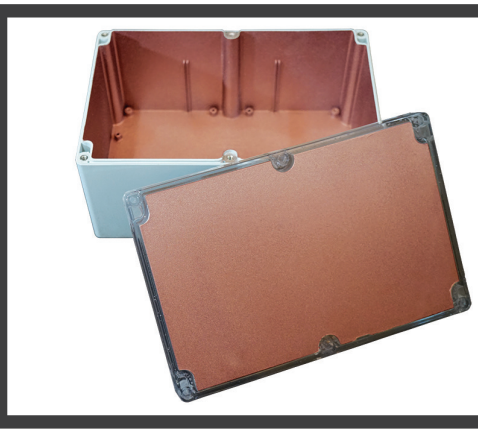
HAMMOND MANUFACTURING™

RL6215

www.hammondmfg.com

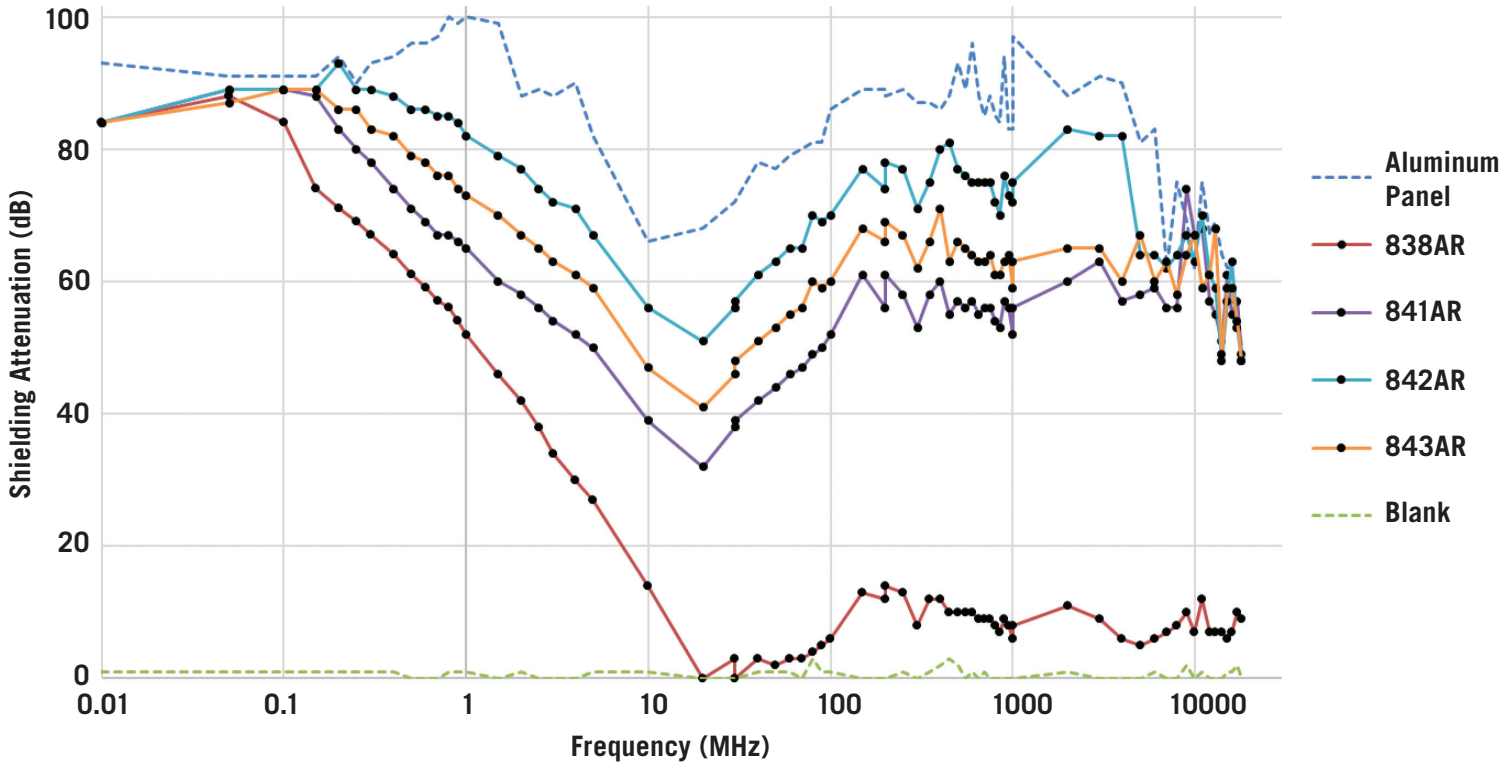
EMI/RFI Shielding — Acrylic Conductive Coatings





- *Provides effective EMI/RFI shielding*
- *Easy to use, solvent based system - available in liquid or aerosol*
- *Smooth, durable, and abrasion resistant*
- *Strong adhesion to most plastics*
- *Does not contain xylene or toluene*
- *Available in four pigments: carbon, nickel, silver coated copper, or silver*

Acrylic Conductive Coating Shielding Effectiveness



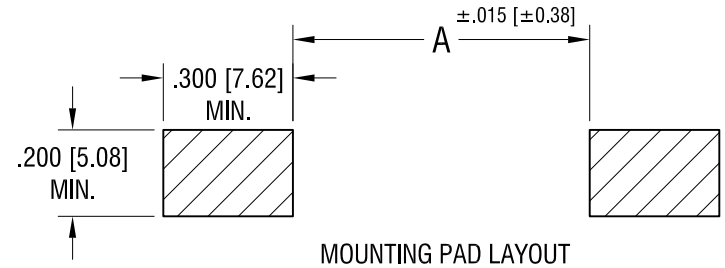
Acrylic Conductive Coating Comparison Chart

Uncured Working Properties	838AR	841AR	843AR	842AR
Conductive Filler	C (carbon)	Ni (nickel)	Ag/Cu (silver coated copper)	Ag (silver)
Format	Liquid	Liquid	Liquid	Liquid
Color	Black	Dark grey	Light metallic brown	Metallic silver
Solids Percentage	15%	57%	31%	61%
Density @ 25 °C [77 °F]	0.85 g/mL	1.7 g/mL	1.1 g/mL	1.7 g/mL
Viscosity @ 25 °C [77 °F]	154 cP	1 460 cP	<30 cP	873 cP
VOC Content	47%	14%	17%	12%
Shelf Life	2 y	2 y	2 y	2 y
Coverage & Application Properties				
Ready to Spray	No	No	Yes	No
Theoretical HVLP Spray Coverage	≤25 300 cm^2/L	≤29 600 cm^2/L	≤15 000 cm^2/L	≤59 600 cm^2/L
Re-coat Time	3 min	3 min	3 min	3 min
Drying Time @ 25 °C [77 °F]	24 h	24 h	24 h	24 h
Drying Time @ 65 °C [149 °F]	30 min	30 min	30 min	30 min
Cured Properties	**838AR**	**841AR**	**843AR**	**842AR**
Electrical Properties				
Volume Resistivity	0.33 Ω·cm	0.0040 Ω·cm	0.00030 Ω·cm	0.00011 Ω·cm
Volume Conductivity	3.1 S/cm	250 S/cm	3 300 S/cm	9 337 S/cm
Surface Resistance @ 1 coat	170 Ω/sq	0.52 Ω/sq	0.071 Ω/sq	<0.01 Ω/sq [a]
Surface Resistance @ 2 coats	60 Ω/sq	0.38 Ω/sq	0.018 Ω/sq	<0.01 Ω/sq [a]
Attenuation from 0.01 to 18 000 MHz	23 dB ± 25 dB	59 dB ± 12 dB	65 dB ± 11 dB	73 dB ± 11 dB
Salt Fog Test @ 35 °C [95 °F], 96 h [b]	Before: 70 Ω/sq After: 70 Ω/sq	Before: 0.38 Ω/sq After: 0.51 Ω/sq	Before: 0.08 Ω/sq After: 3.3 Ω/sq	Before: <0.01 Ω/sq After: 0.05 Ω/sq
Thermal Properties				
Constant Service Temperature	-40 to 120 °C [-40 to 248 °F]	-40 to 120 °C [-40 to 248 °F]	-40 to 120 °C [-40 to 248 °F]	-40 to 120 °C [-40 to 248 °F]
Intermittent Temperature Limits	-50 to 125 °C [-58 to 257 °F]	-50 to 125 °C [-58 to 257 °F]	-50 to 125 °C [-58 to 257 °F]	-50 to 125 °C [-58 to 257 °F]
Mechanical Properties				
Adhesion [b]	5B	5B	5B	5B
Pencil Hardness [b]	H, hard	3H, hard	F, medium	3H, hard
Magnetic Properties				
Magnetic Class	Diamagnetic (non-magnetic)	Ferromagnetic (magnetic)	Diamagnetic (non-magnetic)	Diamagnetic (non-magnetic)
Relative Permeability	<1.0	≥100	<1.0	<1.0

Values for conductive coatings in aerosol format will vary slightly. Please see product's TDS for exact values.
a) Readings less than 0.01 Ω/sq are below the detection limit of the test apparatus b) Tested on acrylonitrile butadiene styrene (ABS)

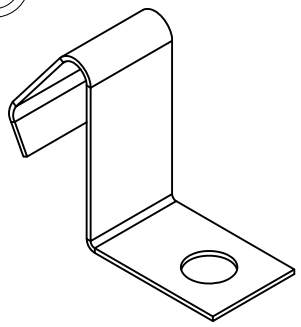
Applications and Uses: • Electronic enclosures • Sensors • Controllers • Receivers • Test equipment • Scientific equipment • Grounding • Medical equipment • Shielding repair • Communication devices • Satellite dishes and radar systems • Antennas • Aerospace • Electric vehicles • Network gear • Military equipment • Cellphones, laptops, PDAs • GPSs, navigation systems • TVs, monitors, displays • Consumer electronics • Prototyping and circuit repair • RC vehicles • Electric guitars and other amplified instruments • Conductive undercoat for electroplating

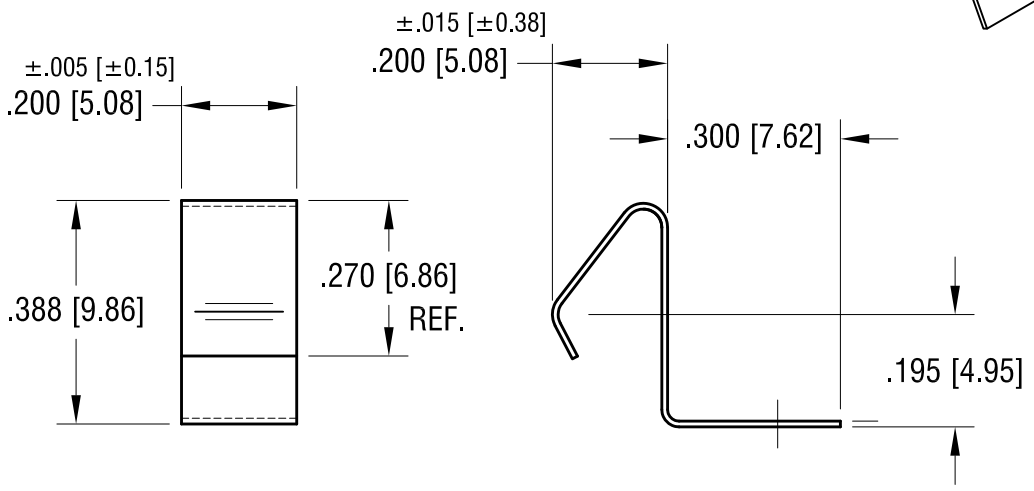
Total Ground™ Carbon Conductive Coating (838AR) *Provides effective for low frequency shielding, musical instruments, and grounding.*
Super Shield™ Nickel Conductive Coating (841AR) *Suitable for most device level shielding applications with excellent corrosion resistance.*
Super Shield™ Silver Coated Copper Conductive Coating (843AR) *Provides superior shielding at higher frequencies.*
Super Shield™ Silver Conductive Coating (842AR) *Offers the best shielding and corrosion resistance. It is also the best choice for board level shielding and can be applied very thin.*

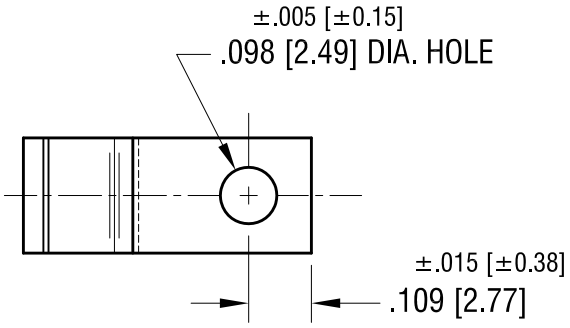


MOUNTING PAD LAYOUT

FOR BATTERY SIZE:	'A' DIM.
AAA	1.959 [49.76]
AAAA	1.864 [47.35]







NOTE:

1. HEAT TREAT TO SPRING TEMPER.

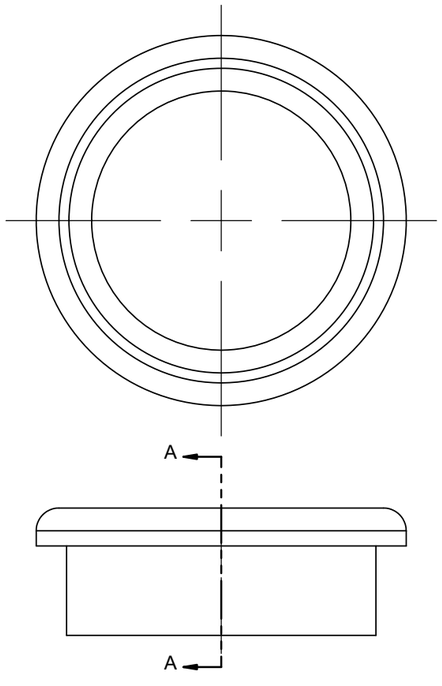
DATE	DESCRIPTION	REV.

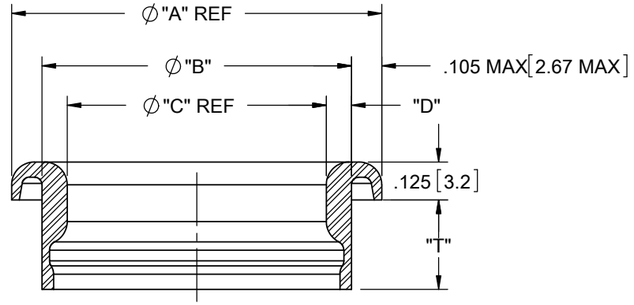
KEYSTONE ELECTRONICS CORP.

www.keyelco.com ● NEW HYDE PARK, NY 11040● Tel (516) 328-7500

PART NAME: BATTERY CONTACT, SURFACE MOUNT			
MATERIAL: .010 [0.25] TH'K ANNEALED SPRING STEEL			
FINISH: MATTE TIN PLATE	DRN BY: NT	DATE: 7.28.09	
	APP'D: LN	SCALE: 3X	
TOLERANCES INCH [MM] DECIMAL ± .010 [± 0.25] ANGULAR ± 1° UNLESS OTHERWISE SPECIFIED	CODE: C	DWG NO.: 5330	

REF MILITARY STANDARD	PART NO.	HOLE DIAMETER +.010/-.005 [+0.25/-0.13]	"T" ±.005 [±0.13]	NAS 1368 PANEL THICKNESS RANGE	MAX RECOMMENDED PANEL THICKNESS	"A" REF	"B"	"C" REF	"D"
NAS1368N4A	GFA-N4A	.375 [9.5]	.235 [5.97]	.025-.080 [0.64-2.03]	.030 [0.76]	.567 [14.4]	.367±.003 [9.3]	.251 [6.4]	.058 [1.47]
NAS1368N4B	GFA-N4B		.295 [7.49]	.081-.140 [2.06-3.56]	.100 [2.54]				
NAS1368N6A	GFA-N6A	.500 [12.7]	.235 [5.97]	.025-.080 [0.64-2.03]	.030 [0.76]	.692 [17.6]	.492±.003 [12.5]	.376 [9.55]	
NAS1368N6B	GFA-N6B		.295 [7.49]	.081-.140 [2.06-3.56]	.090 [2.29]				
NAS1368N6C	GFA-N6C		.360 [9.1]	.141-.200 [3.58-5.08]	.160 [4.06]				
NAS1368N8A	GFA-N8A	.625 [15.9]	.235 [5.97]	.025-.080 [0.64-2.03]	.030 [0.76]	.815 [20.7]	.615±.005 [15.6]	.499 [12.7]	
NAS1368N8B	GFA-N8B		.295 [7.49]	.081-.140 [2.06-3.56]	.090 [2.29]				
NAS1368N10A	GFA-N10A	.781 [19.8]	.235 [5.97]	.025-.080 [0.64-2.03]	.030 [0.76]	.971 [24.7]	.771±.005 [19.6]	.605 [15.4]	.083 [2.11]
NAS1368N10B	GFA-N10B		.295 [7.49]	.081-.140 [2.06-3.56]	.080 [2.03]				
NAS1368N10D	GFA-N10D		.420 [10.7]	.201-.250 [5.1-6.35]	.210 [5.33]				
NAS1368N12A	GFA-N12A	.906 [23]	.235 [5.97]	.025-.080 [0.64-2.03]	.020 [0.51]	1.096 [27.8]	.896±.005 [22.8]	.730 [18.5]	
NAS1368N12B	GFA-N12B		.295 [7.49]	.081-.140 [2.06-3.56]	.070 [1.78]				
NAS1368N14A	GFA-N14A	1.031 [26.2]	.235 [5.97]	.025-.080 [0.64-2.03]	.020 [0.51]	1.221 [31]	1.021±.005 [25.9]	.855 [21.7]	
NAS1368N14B	GFA-N14B		.295 [7.49]	.081-.140 [2.06-3.56]	.070 [1.78]				





SECTION A-A
SCALE 2 : 1

NOTES:
1. MATERIAL: NYLON 6/6 UL 94 V-2 (RMS-01)
2. COLOR: GREEN
3. ALTERNATE UNITS [ ] FOR REFERENCE ONLY

REV.	DESCRIPTION	ENGR.	DATE
C	ADDED COLUMN FOR MILITARY STANDARD CO 200736	DK	11/17/2011
B	ADDED COLUMN FOR MAX PANEL THICKNESS, CO 200702	DK	08/29/11
A	RELEASED FOR PRODUCTION	DK	03.16.11

TITLE:	FLIP GROMMET			UNITS= IN [MM]	
CREATED USING SOLIDWORKS	FILE #: GFA		DWN: DK	APP: MB	FINAL
TOLERANCES UNLESS NOTED .XX=±.010 .XXX=±.005 FRAC.=±1/64 ANG.=±1°	SHEET: 1 OF 1	SHEET SIZE: B	DT: 01/10/11	CHKD: DZ	PART # SEE TABLE
	RE: --	RICHCO, INC.	RICHCO, INC. WWW.RICHCO-INC.COM		PRINT TYPE CA